

## Preliminary Technical Data

### ADuM140D/ADuM140E/ADuM141D/ADuM141E/ ADuM142D/ADuM142E

#### FEATURES

**High common-mode transient immunity: 100 kV/μs**  
**High robustness to radiated and conducted noise**  
**Low propagation delay: 13 ns maximum for 5 V operation,  
15 ns maximum for 1.8 V operation**

**150 Mbps maximum data rate**  
**Safety and regulatory approvals (pending)**

UL recognition

3750 V rms for 1 minute per UL 1577

CSA component acceptance notice 5A

VDE certificate of conformity

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12

$V_{IORM} = 848$  V peak

CQC Certification per GB4943.1-2011

**Backward compatibility**

ADuM14xE1 pin compatible with ADuM140x

**Low dynamic power consumption**

**1.8 V to 5 V level translation**

**High temperature operation: 125°C**

**Failsafe high or low options**

**16-lead, RoHS-compliant, SOIC package**

#### APPLICATIONS

**General-purpose multichannel isolation**

**SPI interface/data converter isolation**

**Industrial field bus isolation**

#### GENERAL DESCRIPTION

The ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E<sup>1</sup> are quad-channel digital isolators based on Analog Devices, Inc., *iCoupler*® technology, of which, only the ADuM140D and ADuM140E are released products. Combining high speed, complementary metal-oxide semiconductor (CMOS) and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices and other integrated couplers. The maximum propagation delay is 13 ns with a pulse width distortion of less than 3 ns at 5 V operation. Channel matching is tight at 3.0 ns maximum.

The ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E data channels are independent and

#### FUNCTIONAL BLOCK DIAGRAMS

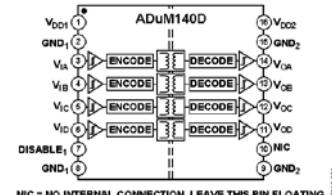


Figure 1. ADuM140D Functional Block Diagram

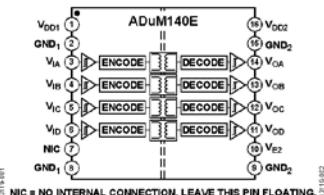


Figure 2. ADuM140E Functional Block Diagram

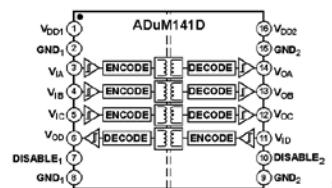


Figure 3. ADuM141D Functional Block Diagram

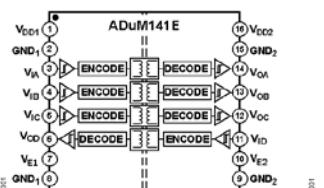


Figure 4. ADuM141E Functional Block Diagram

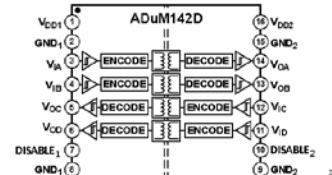


Figure 5. ADuM142D Functional Block Diagram

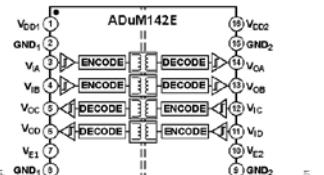


Figure 6. ADuM142E Functional Block Diagram

are available in a variety of configurations with a withstand voltage rating of 3.75 kV rms. The devices operate with the supply voltage on either side ranging from 1.8 V to 5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier.

Unlike other optocoupler alternatives, dc correctness is ensured in the absence of input logic transitions. Two different fail-safe options are available, in which the outputs transition to a predetermined state when the input power supply is not applied or the inputs are disabled. The ADuM14xE1 are pin compatible with the ADuM140x.

<sup>1</sup> Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

Rev. P.RA

Document Feedback

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## REVISION HISTORY

6/15—Revision PrA: Preliminary Version

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 5\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range of  $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within pulse width distortion (PWD) limit
Data Rate		150			Mbps	Within PWD limit
Propagation Delay	$t_{PHL}, t_{PLH}$	4.8	7.2	13	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.5	3	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			1.5		$\text{ps}/^\circ\text{C}$	
Propagation Delay Skew	$t_{PSK}$			6.1	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	$t_{PSKCD}$		0.5	3.0	ns	
Opposing Direction	$t_{PSKOD}$		0.5	3.0	ns	
Jitter			490		$\text{ps p-p}$	See the Jitter Measurement section
			TBD		$\text{ps rms}$	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold						
Logic High	$V_{IH}$	0.7 $\times$			V	
Logic Low	$V_{IL}$		0.3 $\times$		V	
Output Voltage						
Logic High	$V_{OH}$	$V_{DDx} - 0.1$	$V_{DDx}$		V	$I_{Ox^1} = -20\text{ }\mu\text{A}, V_{Ix} = V_{IxH^2}$
Logic Low	$V_{OL}$	$V_{DDx} - 0.4$	$V_{DDx} - 0.2$		V	$I_{Ox^1} = -4\text{ mA}, V_{Ix} = V_{IxL^2}$
Input Current per Channel	$I_I$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{Ix} \leq V_{DDx}$
$V_{E2}$ Enable Input Pull-Up Current	$I_{PU}$	-10	-3		$\mu\text{A}$	$V_{E2} = 0\text{ V}$
DISABLE <sub>1</sub> Input Pull-Down Current	$I_{PD}$		9	15	$\mu\text{A}$	$\text{DISABLE}_1 = V_{DDx}$
Tristate Output Current per Channel	$I_{Oz}$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{Ox} \leq V_{DDx}$
Quiescent Supply Current						
ADuM140D/ADuM140E						
$I_{DD1(Q)}$			TBD	TBD	mA	$V_I^4 = 0\text{ (E0, D0), 1 (E1, D1)^5}$
$I_{DD2(Q)}$			TBD	TBD	mA	$V_I^4 = 0\text{ (E0, D0), 1 (E1, D1)^5}$
$I_{DD1(Q)}$			TBD	TBD	mA	$V_I^4 = 1\text{ (E0, D0), 0 (E1, D1)^5}$
$I_{DD2(Q)}$			TBD	TBD	mA	$V_I^4 = 1\text{ (E0, D0), 0 (E1, D1)^5}$
ADuM141D/ADuM141E						
$I_{DD1(Q)}$			TBD	TBD	mA	
$I_{DD2(Q)}$			TBD	TBD	mA	
$I_{DD1(Q)}$			TBD	TBD	mA	
$I_{DD2(Q)}$			TBD	TBD	mA	
ADuM142D/ADuM142E						
$I_{DD1(Q)}$			TBD	TBD	mA	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Dynamic Supply Current	$I_{DD2(Q)}$		TBD	TBD	mA	
	$I_{DD1(Q)}$		TBD	TBD	mA	
	$I_{DD2(Q)}$		TBD	TBD	mA	
Dynamic Input	$I_{DD1(D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO(D)}$		0.02		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive $V_{DDX}$ Threshold	$V_{DDxUV+}$		1.6		V	
Negative $V_{DDX}$ Threshold	$V_{DDxUV-}$		1.5		V	
$V_{DDX}$ Hysteresis	$V_{DDxUVH}$		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	$t_R/t_F$		2.5		ns	10% to 90%
Common-Mode Transient Immunity <sup>6</sup>	$ CM_{H }$	75	100		kV/ $\mu$ s	$V_{IX} = V_{DDX}$ , $V_{CM} = 1000$ V, transient magnitude = 800 V
	$ CM_L $	75	100		kV/ $\mu$ s	$V_{IX} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V

<sup>1</sup>  $I_{ox}$  is the Channel x output current, where x = A, B, C, or D.

<sup>2</sup>  $V_{IXH}$  is the input side logic high.

<sup>3</sup>  $V_{IXL}$  is the input side logic low.

<sup>4</sup>  $V_I$  is the voltage input.

<sup>5</sup> E0 is the ADuM14xE0 model, D0 is the ADuM14xD0 model, E1 is the ADuM14xE1 model, and D1 is the ADuM14xD1 model.

<sup>6</sup>  $|CM_{H|}$  is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output ( $V_O$ ) > 0.8  $V_{DDX}$ .  $|CM_L|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O$  > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

**Table 2. Total Supply Current vs. Data Throughput**

Parameter	Symbol	1 Mbps			25 Mbps			100 Mbps			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SUPPLY CURRENT											
ADuM140D											
Supply Current Side 1	$I_{DD1}$		6.8	10		7.8	12		11.8	17.4	mA
Supply Current Side 2	$I_{DD2}$		2.1	3.7		3.9	5.7		9.2	13	mA
ADuM141D											
Supply Current Side 1	$I_{DD1}$		TBD	TBD		TBD	TBD		TBD	TBD	mA
Supply Current Side 2	$I_{DD2}$		TBD	TBD		TBD	TBD		TBD	TBD	mA
ADuM142D											
Supply Current Side 1	$I_{DD1}$		4.3	7.7		6.0	9.3		10.3	14.2	mA
Supply Current Side 2	$I_{DD2}$		5.3	8.7		6.7	10.1		11.0	14.9	mA

### ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 3.3$  V. Minimum/maximum specifications apply over the entire recommended operation range:  $3.0$  V  $\leq V_{DD1} \leq 3.6$  V,  $3.0$  V  $\leq V_{DD2} \leq 3.6$  V, and  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15$  pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

**Table 3.**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate		150			Mbps	Within PWD limit

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Propagation Delay	$t_{PHL}, t_{PLH}$	4.8	6.8	14	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	3	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	$t_{PSK}$			7.5	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	$t_{PSKCD}$		0.7	3.0	ns	
Opposing Direction	$t_{PSKOD}$		0.7	3.0	ns	
Jitter			580		ps p-p	See the Jitter Measurement section
				TBD	ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold						
Logic High	$V_{IH}$	$0.7 \times V_{DDx}$			V	
Logic Low	$V_{IL}$		$0.3 \times V_{DDx}$		V	
Output Voltage						
Logic High	$V_{OH}$	$V_{DDx} - 0.1$	$V_{DDx}$		V	$I_{ox^1} = -20 \mu A, V_{lx} = V_{lxH^2}$
		$V_{DDx} - 0.4$	$V_{DDx} - 0.2$		V	$I_{ox^1} = -2 mA, V_{lx} = V_{lxH^2}$
Logic Low	$V_{OL}$	0.0	0.1		V	$I_{ox^1} = 20 \mu A, V_{lx} = V_{lxL^3}$
		0.2	0.4		V	$I_{ox^1} = 2 mA, V_{lx} = V_{lxL^3}$
Input Current per Channel	$I_I$	-10	+0.01	+10	μA	$0 V \leq V_{lx} \leq V_{DDx}$
$V_{E2}$ Enable Input Pull-Up Current	$I_{PU}$	-10	-3		μA	$V_{E2} = 0 V$
DISABLE <sub>1</sub> Input Pull-Down Current	$I_{PD}$	9	15		μA	$DISABLE_1 = V_{DDx}$
Tristate Output Current per Channel	$I_{OZ}$	-10	+0.01	+10	μA	$0 V \leq V_{ox} \leq V_{DDx}$
Quiescent Supply Current						
ADuM140D/ADuM140E	$I_{DD1 (Q)}$ $I_{DD2 (Q)}$		TBD	TBD	mA	$V_I^4 = 0 (E0, D0), 1 (E1, D1)^5$
	$I_{DD1 (Q)}$ $I_{DD2 (Q)}$		TBD	TBD	mA	$V_I^4 = 0 (E0, D0), 1 (E1, D1)^5$
	$I_{DD1 (Q)}$ $I_{DD2 (Q)}$		TBD	TBD	mA	$V_I^4 = 1 (E0, D0), 0 (E1, D1)^5$
	$I_{DD1 (Q)}$ $I_{DD2 (Q)}$		TBD	TBD	mA	$V_I^4 = 1 (E0, D0), 0 (E1, D1)^5$
ADuM141D/ADuM141E	$I_{DD1 (Q)}$ $I_{DD2 (Q)}$		TBD	TBD	mA	
	$I_{DD1 (Q)}$ $I_{DD2 (Q)}$		TBD	TBD	mA	
	$I_{DD1 (Q)}$ $I_{DD2 (Q)}$		TBD	TBD	mA	
	$I_{DD1 (Q)}$ $I_{DD2 (Q)}$		TBD	TBD	mA	
ADuM142D/ADuM142E	$I_{DD1 (Q)}$ $I_{DD2 (Q)}$		TBD	TBD	mA	
	$I_{DD1 (Q)}$ $I_{DD2 (Q)}$		TBD	TBD	mA	
	$I_{DD1 (Q)}$ $I_{DD2 (Q)}$		TBD	TBD	mA	
	$I_{DD1 (Q)}$ $I_{DD2 (Q)}$		TBD	TBD	mA	
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive $V_{DDx}$ Threshold	$V_{DDxUV+}$		1.6		V	
Negative $V_{DDx}$ Threshold	$V_{DDxUV-}$		1.5		V	
$V_{DDx}$ Hysteresis	$V_{DDxUVH}$		0.1		V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
AC SPECIFICATIONS						
Output Rise/Fall Time	$t_{R/F}$		2.5		ns	10% to 90%
Common-Mode Transient Immunity <sup>5</sup>	$ CM_H $	75	100		kV/ $\mu$ s	$V_{lx} = V_{DDx}$ , $V_{CM} = 1000$ V, transient magnitude = 800 V
	$ CM_L $	75	100		kV/ $\mu$ s	$V_{lx} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V

<sup>1</sup>  $I_{Ox}$  is the Channel x output current, where x = A, B, C, or D.

<sup>2</sup>  $V_{IH}$  is the input side logic high.

<sup>3</sup>  $V_{IL}$  is the input side logic low.

<sup>4</sup>  $V_i$  is the voltage input.

<sup>5</sup> E0 is the **ADuM14xE0** model, D0 is the **ADuM14xD0** model, E1 is the **ADuM14xE1** model, and D1 is the **ADuM14xD1** model.

<sup>6</sup>  $|CM_H|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output ( $V_o$ )  $> 0.8 V_{DDx}$ .  $|CM_L|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_o > 0.8$  V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

**Table 4. Total Supply Current vs. Data Throughput**

Parameter	Symbol	1 Mbps			25 Mbps			100 Mbps			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SUPPLY CURRENT											
ADuM140E/ADuM140D											
Supply Current Side 1	$I_{DD1}$		6.6	9.8		7.4	11.2		10.7	15.9	mA
Supply Current Side 2	$I_{DD2}$		2.0	3.7		3.5	5.5		8.2	11.6	mA
ADuM141E/ADuM141D											
Supply Current Side 1	$I_{DD1}$		TBD	TBD		TBD	TBD		TBD	TBD	mA
Supply Current Side 2	$I_{DD2}$		TBD	TBD		TBD	TBD		TBD	TBD	mA
ADuM142E/ADuM142D											
Supply Current Side 1	$I_{DD1}$		4.3	7.7		5.6	9.0		9.1	13	mA
Supply Current Side 2	$I_{DD2}$		5.0	8.4		6.2	9.6		9.8	13.7	mA

## ELECTRICAL CHARACTERISTICS—2.5 V OPERATION

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 2.5$  V. Minimum/maximum specifications apply over the entire recommended operation range:  $2.25$  V  $\leq V_{DD1} \leq 2.75$  V,  $2.25$  V  $\leq V_{DD2} \leq 2.75$  V,  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15$  pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

**Table 5.**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	$PW$	6.6			ns	Within PWD limit
Data Rate		150			Mbps	Within PWD limit
Propagation Delay	$t_{PHL}, t_{PLH}$	5.0	7.0	14	ns	50% input to 50% output
Pulse Width Distortion	$PWD$		0.7	3	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			1.5		ps/ $^\circ\text{C}$	
Propagation Delay Skew	$t_{PSK}$			6.8	ns	Between any two units at the same temperature, voltage, load
Channel Matching						
Codirectional	$t_{PSKCD}$		0.7	3.0	ns	
Opposing Direction	$t_{PSKOD}$		0.7	3.0	ns	
Jitter		800			ps p-p	See the Jitter Measurement section
					ps rms	See the Jitter Measurement section

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Threshold						
Logic High	$V_{IH}$	$0.7 \times V_{DDx}$			V	
Logic Low	$V_{IL}$			$0.3 \times V_{DDx}$	V	
Output Voltage						
Logic High	$V_{OH}$	$V_{DDx} - 0.1$	$V_{DDx}$		V	$I_{ox}^1 = -20 \mu A, V_{lx} = V_{lxH}^2$
		$V_{DDx} - 0.4$	$V_{DDx} - 0.2$		V	$I_{ox}^1 = -2 mA, V_{lx} = V_{lxH}^2$
Logic Low	$V_{OL}$	0.0	0.1		V	$I_{ox}^1 = 20 \mu A, V_{lx} = V_{lxL}^3$
		0.2	0.4		V	$I_{ox}^1 = 2 mA, V_{lx} = V_{lxL}^3$
Input Current per Channel	$I_I$	-10	+0.01	+10	$\mu A$	$0 V \leq V_{lx} \leq V_{DDx}$
$V_{E2}$ Enable Input Pull-Up Current	$I_{PU}$	-10	-3		$\mu A$	$V_{E2} = 0 V$
DISABLE <sub>1</sub> Input Pull-Down Current	$I_{PD}$	9		15	$\mu A$	$DISABLE_1 = V_{DDx}$
Tristate Output Current per Channel	$I_{OZ}$	-10	+0.01	+10	$\mu A$	$0 V \leq V_{Ox} \leq V_{DDx}$
Quiescent Supply Current						
ADuM140D/ADuM140E	$I_{DD1 (Q)}$	TBD		TBD	mA	$V_I^4 = 0 (E0, D0), 1 (E1, D1)^5$
	$I_{DD2 (Q)}$	TBD		TBD	mA	$V_I^4 = 0 (E0, D0), 1 (E1, D1)^5$
	$I_{DD1 (Q)}$	TBD		TBD	mA	$V_I^4 = 1 (E0, D0), 0 (E1, D1)^5$
	$I_{DD2 (Q)}$	TBD		TBD	mA	$V_I^4 = 1 (E0, D0), 0 (E1, D1)^5$
ADuM141D/ADuM141E	$I_{DD1 (Q)}$	TBD		TBD	mA	
	$I_{DD2 (Q)}$	TBD		TBD	mA	
	$I_{DD1 (Q)}$	TBD		TBD	mA	
	$I_{DD2 (Q)}$	TBD		TBD	mA	
ADuM142D/ADuM142E	$I_{DD1 (Q)}$	TBD		TBD	mA	
	$I_{DD2 (Q)}$	TBD		TBD	mA	
	$I_{DD1 (Q)}$	TBD		TBD	mA	
	$I_{DD2 (Q)}$	TBD		TBD	mA	
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$	0.01			$mA/Mbps$	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$	0.01			$mA/Mbps$	Inputs switching, 50% duty cycle
Undervoltage Lockout						
Positive $V_{DDx}$ Threshold	$V_{DDxUV+}$	1.6			V	
Negative $V_{DDx}$ Threshold	$V_{DDxUV-}$	1.5			V	
$V_{DDx}$ Hysteresis	$V_{DDxUVH}$	0.1			V	
AC SPECIFICATIONS						
Output Rise/Fall Time	$t_R/t_F$	2.5			ns	10% to 90%
Common-Mode Transient Immunity <sup>6</sup>	$ CM_H $	75	100		$kV/\mu s$	$V_{lx} = V_{DDx}, V_{CM} = 1000 V$ , transient magnitude = 800 V
	$ CM_L $	75	100		$kV/\mu s$	$V_{lx} = 0 V, V_{CM} = 1000 V$ , transient magnitude = 800 V

<sup>1</sup>  $I_{ox}$  is the Channel x output current, where x = A, B, C, or D.<sup>2</sup>  $V_{lxH}$  is the input side logic high.<sup>3</sup>  $V_{lxL}$  is the input side logic low.<sup>4</sup>  $V_I$  is the voltage input.<sup>5</sup> E0 is the ADuM14x E0 model, D0 is the ADuM14x D0 model, E1 is the ADuM14x E1 model, and D1 is the ADuM14x D1 model.<sup>6</sup>  $|CM_H|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output ( $V_o$ ) > 0.8  $V_{DDx}$ .  $|CM_L|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_o > 0.8 V$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

**Table 6. Total Supply Current vs. Data Throughput**

<b>Parameter</b>	<b>Symbol</b>	<b>1 Mbps</b>			<b>25 Mbps</b>			<b>100 Mbps</b>			<b>Unit</b>
		<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	
SUPPLY CURRENT											
ADuM140D/ADuM140E											
Supply Current Side 1	$I_{DD1}$		6.5	9.8		7.3	11.1		10.4	15.5	mA
Supply Current Side 2	$I_{DD2}$		2.0	3.6		3.3	5.2		7.3	10.2	mA
ADuM141D/ADuM141E											
Supply Current Side 1	$I_{DD1}$		TBD	TBD		TBD	TBD		TBD	TBD	mA
Supply Current Side 2	$I_{DD2}$		TBD	TBD		TBD	TBD		TBD	TBD	mA
ADuM142D/ADuM142E											
Supply Current Side 1	$I_{DD1}$		4.3	7.7		5.4	8.8		8.8	12.7	mA
Supply Current Side 2	$I_{DD2}$		5.0	8.4		6.1	9.5		9.5	13.4	mA

**ELECTRICAL CHARACTERISTICS—1.8 V OPERATION**

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 1.8\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range:  $1.7\text{ V} \leq V_{DD1} \leq 1.9\text{ V}$ ,  $1.7\text{ V} \leq V_{DD2} \leq 1.9\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

**Table 7.**

<b>Parameter</b>	<b>Symbol</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>	<b>Test Conditions/Comments</b>
<b>SWITCHING SPECIFICATIONS</b>						
Pulse Width	$PW$	6.6			ns	Within PWD limit
Data Rate		150			Mbps	Within PWD limit
Propagation Delay	$t_{PHL}, t_{PLH}$	5.8	8.7	15	ns	50% input to 50% output
Pulse Width Distortion	$PWD$		0.7	3	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			1.5		$\text{ps}/^\circ\text{C}$	
Propagation Delay Skew	$t_{PSK}$			7.0	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	$t_{PSKCD}$		0.7	3.0	ns	
Opposing Direction	$t_{PSKOD}$		0.7	3.0	ns	
Jitter			470		ps p-p	See the Jitter Measurement section
				TBD	ps rms	See the Jitter Measurement section
<b>DC SPECIFICATIONS</b>						
Input Threshold						
Logic High	$V_{IH}$	$0.7 \times V_{DDx}$			V	
Logic Low	$V_{IL}$			$0.3 \times V_{DDx}$	V	
Output Voltage						
Logic High	$V_{OH}$	$V_{DDx} - 0.1$	$V_{DDx}$		V	$I_{ox}^1 = -20\text{ }\mu\text{A}, V_{lx} = V_{lxH}^2$
		$V_{DDx} - 0.4$	$V_{DDx} - 0.2$		V	$I_{ox}^1 = -2\text{ mA}, V_{lx} = V_{lxH}^2$
Logic Low	$V_{OL}$		0.0	0.1	V	$I_{ox}^1 = 20\text{ }\mu\text{A}, V_{lx} = V_{lxL}^3$
			0.2	0.4	V	$I_{ox}^1 = 2\text{ mA}, V_{lx} = V_{lxL}^3$
Input Current per Channel	$I_I$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{lx} \leq V_{DDx}$
$V_{E2}$ Enable Input Pull-Up Current	$I_{PU}$	-10	-3		$\mu\text{A}$	$V_{E2} = 0\text{ V}$
DISABLE <sub>1</sub> Input Pull-Down Current	$I_{PD}$		9	15	$\mu\text{A}$	$\text{DISABLE}_1 = V_{DDx}$
Tristate Output Current per Channel	$I_{OZ}$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{Ox} \leq V_{DDx}$
Quiescent Supply Current						
ADuM140D/ADuM140E	$I_{DD1(Q)}$		TBD	TBD	mA	$V_I^4 = 0\text{ (E0, D0), 1 (E1, D1)}^5$
	$I_{DD2(Q)}$		TBD	TBD	mA	$V_I^4 = 0\text{ (E0, D0), 1 (E1, D1)}^5$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ADuM141D/ADuM141E	I <sub>DD1</sub> (Q)		TBD	TBD	mA	V <sub>i</sub> <sup>4</sup> = 1 (E0, D0), 0 (E1, D1) <sup>5</sup>
	I <sub>DD2</sub> (Q)		TBD	TBD	mA	V <sub>i</sub> <sup>4</sup> = 1 (E0, D0), 0 (E1, D1) <sup>5</sup>
ADuM142D/ADuM142E	I <sub>DD1</sub> (Q)		TBD	TBD	mA	
	I <sub>DD2</sub> (Q)		TBD	TBD	mA	
Dynamic Supply Current	I <sub>DD1</sub> (Q)		TBD	TBD	mA	
	I <sub>DD2</sub> (Q)		TBD	TBD	mA	
Dynamic Input	I <sub>DD1</sub> (D)		0.01		mA/Mbps	Inputs switching, 50% duty cycle
	I <sub>DD0</sub> (D)		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive V <sub>DDx</sub> Threshold	V <sub>DDxUV+</sub>		1.6		V	
Negative V <sub>DDx</sub> Threshold	V <sub>DDxUV-</sub>		1.5		V	
V <sub>DDx</sub> Hysteresis	V <sub>DDxUVH</sub>		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t <sub>R</sub> /t <sub>F</sub>		2.5		ns	10% to 90%
Common-Mode Transient Immunity <sup>6</sup>	CM <sub>H</sub>	75	100		kV/μs	V <sub>lx</sub> = V <sub>DDx</sub> , V <sub>CM</sub> = 1000 V, transient magnitude = 800 V
	CM <sub>L</sub>	75	100		kV/μs	V <sub>lx</sub> = 0 V, V <sub>CM</sub> = 1000 V, transient magnitude = 800 V

<sup>1</sup> I<sub>ox</sub> is the Channel x output current, where x = A, B, C, or D.<sup>2</sup> V<sub>lxH</sub> is the input side logic high.<sup>3</sup> V<sub>lxL</sub> is the input side logic low.<sup>4</sup> V<sub>i</sub> is the voltage input.<sup>5</sup> E0 is the ADuM14xE0 model, D0 is the ADuM14xD0 model, E1 is the ADuM14xE1 model, and D1 is the ADuM14xD1 model.<sup>6</sup> |CM<sub>H</sub>| is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V<sub>o</sub>) > 0.8 V<sub>DDx</sub>. |CM<sub>L</sub>| is the maximum common-mode voltage slew rate that can be sustained while maintaining V<sub>o</sub> > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 8. Total Supply Current vs. Data Throughput

Parameter	Symbol	1 Mbps			25 Mbps			100 Mbps			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SUPPLY CURRENT											
ADuM140E/ADuM140D											
Supply Current Side 1	I <sub>DD1</sub>		6.4	9.8		7.2	11		10.2	15.2	mA
Supply Current Side 2	I <sub>DD2</sub>		1.9	3.5		3.1	5.0		6.8	10	mA
ADuM141E/ADuM141D											
Supply Current Side 1	I <sub>DD1</sub>		TBD	TBD		TBD	TBD		TBD	TBD	mA
Supply Current Side 2	I <sub>DD2</sub>		TBD	TBD		TBD	TBD		TBD	TBD	mA
ADuM142E/ADuM142D											
Supply Current Side 1	I <sub>DD1</sub>		4.3	7.7		5.3	8.7		8.6	12.6	mA
Supply Current Side 2	I <sub>DD2</sub>		4.9	8.3		6.0	9.4		9.3	13.3	mA

**INSULATION AND SAFETY RELATED SPECIFICATIONS**

For additional information, see [www.analog.com/icouplersafety](http://www.analog.com/icouplersafety).

**Table 9.**

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3750	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	7.8	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	7.8	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.1	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		25.5	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

**PACKAGE CHARACTERISTICS**
**Table 10.**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output) <sup>1</sup>	R <sub>I-O</sub>		10 <sup>13</sup>		Ω	
Capacitance (Input to Output) <sup>1</sup>	C <sub>I-O</sub>		2.2		pF	f = 1 MHz
Input Capacitance <sup>2</sup>	C <sub>I</sub>		4.0		pF	
IC Junction to Ambient Thermal Resistance	θ <sub>JA</sub>		45		°C/W	Thermocouple located at center of package underside

<sup>1</sup> The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

<sup>2</sup> Input capacitance is from any input data pin to ground.

**REGULATORY INFORMATION**

See Table 15 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

**Table 11.**

<b>UL (Pending)</b>	<b>CSA (Pending)</b>	<b>VDE (Pending)</b>	<b>CQC (Pending)</b>
Recognized under 1577 Component Recognition Program <sup>1</sup>	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 <sup>2</sup>	Certified by CQC11-471543-2012
Single Protection, 3750 V rms Isolation Voltage	Basic insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1, Second Edition +A1+A2, 760 V rms (1075 V peak)  Reinforced insulation (2MOPP) per IEC 60601-1 Edition 3.1, 125 V rms (176 V peak) maximum  Reinforced insulation per CSA 61010-1-12 and IEC 61010-1 Third Edition (Pollution Degree 2, Material Group III, Overvoltage Category II, and Overvoltage Category III): 300 V rms (424 V peak) maximum working voltage	Reinforced insulation, 849 V peak	Basic insulation per GB4943.1-2011  Working voltage 760 V rms (1075 V peak), tropical climate, altitude $\leq$ 5000 meters
File E214100	File 205078	File 2471900-4880-0001	File (pending)

<sup>1</sup> In accordance with UL 1577, each ADuM14xD/ADuM14xE is proof tested by applying an insulation test voltage  $\geq$  4500 V rms for 1 sec.

<sup>2</sup> In accordance with DIN V VDE V 0884-10, each ADuM14xD/ADuM14xE is proof tested by applying an insulation test voltage  $\geq$  1018 V peak for 1 sec (partial discharge detection limit = 5 pC). The \* marking branded on the component designates DIN V VDE V 0884-10 approval.

**DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS**

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data. The \* marking on packages denotes DIN V VDE V 0884-10 approval.

**Table 12.**

<b>Description</b>	<b>Test Conditions/Comments</b>	<b>Symbol</b>	<b>Characteristic</b>	<b>Unit</b>
Installation Classification per DIN VDE 0110  For Rated Mains Voltage $\leq$ 150 V rms For Rated Mains Voltage $\leq$ 300 V rms For Rated Mains Voltage $\leq$ 400 V rms			I to IV I to III I to III	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V <sub>IORM</sub>	848	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$ , 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge $< 5$ pC	V <sub>pd(m)</sub>	1592	V peak
Input to Output Test Voltage, Method A  After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$ , $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge $< 5$ pC	V <sub>pd(m)</sub>	1274	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$ , $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge $< 5$ pC		1019	V peak
Highest Allowable Overvoltage		V <sub>IOTM</sub>	5300	V peak

<b>Description</b>	<b>Test Conditions/Comments</b>	<b>Symbol</b>	<b>Characteristic</b>	<b>Unit</b>
Surge Isolation Voltage	V peak = 12.8 kV, 1.2 $\mu$ s rise time, 50 $\mu$ s, 50% fall time	$V_{IOSM}$	<b>6000</b>	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 7)			
Maximum Junction Temperature		$T_S$	150	°C
Total Power Dissipation at 25°C		$P_S$	<b>2.78</b>	W
Insulation Resistance at $T_S$	$V_{IO} = 500$ V	$R_S$	$>10^9$	$\Omega$

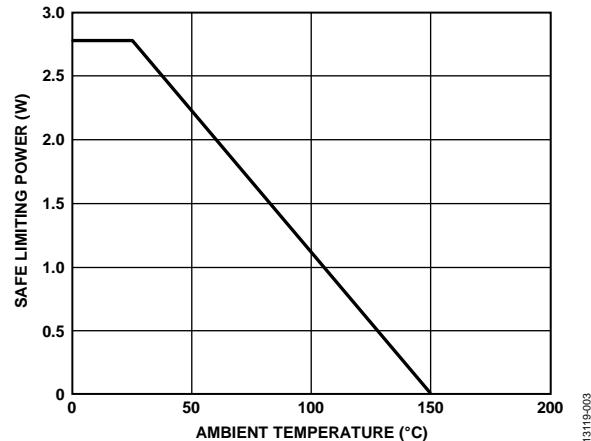


Figure 7. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-10

## RECOMMENDED OPERATING CONDITIONS

Table 13.

<b>Parameter</b>	<b>Symbol</b>	<b>Rating</b>
Operating Temperature	$T_A$	-40°C to +125°C
Supply Voltages	$V_{DD1}, V_{DD2}$	1.7 V to 5.5 V
Input Signal Rise and Fall Times		1.0 ms

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 14.

Parameter	Rating
Storage Temperature ( $T_{ST}$ ) Range	−65°C to +150°C
Ambient Operating Temperature ( $T_A$ ) Range	−40°C to +125°C
Supply Voltages ( $V_{DD1}, V_{DD2}$ )	−0.5 V to +7.0 V
Input Voltages ( $V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{E1}, V_{E2}, \text{DISABLE}_1, \text{DISABLE}_2$ )	−0.5 V to $V_{DD1} + 0.5$ V
Output Voltages ( $V_{OA}, V_{OB}, V_{OC}, V_{OD}$ )	−0.5 V to $V_{DD2} + 0.5$ V
Average Output Current per Pin <sup>3</sup>	
Side 1 Output Current ( $I_{O1}$ )	−10 mA to +10 mA
Side 2 Output Current ( $I_{O2}$ )	−10 mA to +10 mA
Common-Mode Transients <sup>4</sup>	−150 kV/μs to +150 kV/μs

<sup>1</sup>  $V_{DD1}$  is the input side supply voltage.

<sup>2</sup>  $V_{DD2}$  is the output side supply voltage.

<sup>3</sup> See Figure 7 for the maximum rated current values for various temperatures.

<sup>4</sup> Refers to the common-mode transients across the insulation barrier.

Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 15. Maximum Continuous Working Voltage<sup>1</sup>

Parameter	Rating	Constraint
AC Voltage		
Bipolar Waveform		
Basic Insulation	849 V peak	50-year minimum insulation lifetime
Reinforced Insulation	790 V peak	50-year minimum insulation lifetime
Unipolar Waveform		
Basic Insulation	1698 V peak	50-year minimum insulation lifetime
Reinforced Insulation	849 V peak	50-year minimum insulation lifetime
DC Voltage		
Basic Insulation	1118 V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
Reinforced Insulation	559 V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1

<sup>1</sup> Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.**  
Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

**Truth Tables**

Table 16. **ADuM14xD Truth Table (Positive Logic)**

<b><math>V_{lx}</math> Input<sup>1, 2</sup></b>	<b><math>V_{DISABLEx}</math> Input<sup>1, 2</sup></b>	<b><math>V_{DDI}</math> State<sup>2</sup></b>	<b><math>V_{DDO}</math> State<sup>2</sup></b>	<b>Default Low (D0), <math>V_{ox}</math> Output<sup>1, 2</sup></b>	<b>Default High (D1), <math>V_{ox}</math> Output<sup>1, 2</sup></b>	<b>Test Conditions/ Comments</b>
L	L or NC	Powered	Powered	L	L	Normal operation
H	L or NC	Powered	Powered	H	H	Normal operation
X	H	Powered	Powered	L	H	Inputs disabled, fail-safe output
X <sup>4</sup>	X <sup>4</sup>	Unpowered	Powered	L	H	Fail-safe output
X <sup>4</sup>	X <sup>4</sup>	Powered	Unpowered	Indeterminate	Indeterminate	

<sup>1</sup> H means high, L means low, X means don't care, and NC means not connected.

<sup>2</sup>  $V_{lx}$  and  $V_{ox}$  refer to the input and output signals of a given channel (A, B, C, or D).  $V_{DISABLE1}$  refers to the input disable signal on the same side as the  $V_{lx}$  inputs.  $V_{DDI}$  and  $V_{DDO}$  refer to the supply voltages on the input and output sides of the given channel, respectively.

<sup>3</sup> D0 is the **ADuM14xD0** model and D1 is the **ADuM14xD1** model.

<sup>4</sup> Input pins ( $V_{lx}$ ,  $DISABLE_1$ , and  $DISABLE_2$ ) on the same side as an unpowered supply must be in a low state to avoid powering the device through its ESD protection circuitry.

Table 17. **ADuM14xE Truth Table (Positive Logic)**

<b><math>V_{lx}</math> Input<sup>1, 2</sup></b>	<b><math>V_{Ex}</math> Input<sup>1, 2</sup></b>	<b><math>V_{DDI}</math> State<sup>2</sup></b>	<b><math>V_{DDO}</math> State<sup>2</sup></b>	<b>Default Low (E0), <math>V_{ox}</math> Output<sup>1, 2</sup></b>	<b>Default High (E1), <math>V_{ox}</math> Output<sup>1, 2</sup></b>	<b>Test Conditions/ Comments</b>
L	H or NC	Powered	Powered	L	L	Normal operation
H	H or NC	Powered	Powered	H	H	Normal operation
X	L	Powered	Powered	Z	Z	Outputs disabled
L	H or NC	Unpowered	Powered	L	H	Fail-safe output
X <sup>4</sup>	L <sup>4</sup>	Unpowered	Powered	Z	Z	Outputs disabled
X <sup>4</sup>	X <sup>4</sup>	Powered	Unpowered	Indeterminate	Indeterminate	

<sup>1</sup> H means high, L means low, X means don't care, and NC means not connected, and Z means high impedance.

<sup>2</sup>  $V_{lx}$  and  $V_{ox}$  refer to the input and output signals of a given channel (A, B, C, or D).  $V_{DISABLE1}$  refers to the input disable signal on the same side as the  $V_{lx}$  inputs.  $V_{DDI}$  and  $V_{DDO}$  refer to the supply voltages on the input and output sides of the given channel, respectively.

<sup>3</sup> E0 is the **ADuM14xE0** model and E1 is the **ADuM14xE1** model.

<sup>4</sup> Input pins ( $V_{lx}$ ,  $V_{E1}$ , and  $V_{E2}$ ) on the same side as an unpowered supply must be in a low state to avoid powering the device through its ESD protection circuitry.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

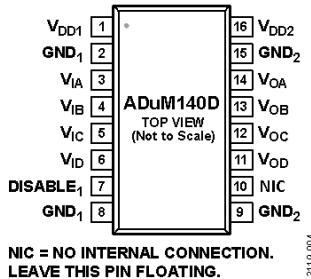


Figure 8. ADuM140D Pin Configuration

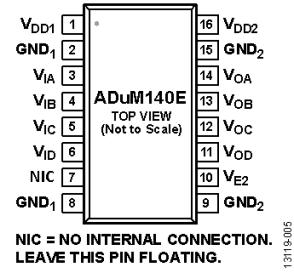


Figure 9. ADuM140E Pin Configuration

Reference the [AN-1109 Application Note](#) for specific layout guidelines.

Table 18. Pin Function Descriptions

Pin No.		Mnemonic	Description
ADuM140D	ADuM140E		
1	1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1.
2, 8	2, 8	GND <sub>1</sub>	Ground 1. Ground reference for Isolator Side 1.
3	3	V <sub>IA</sub>	Logic Input A.
4	4	V <sub>IB</sub>	Logic Input B.
5	5	V <sub>IC</sub>	Logic Input C.
6	6	V <sub>ID</sub>	Logic Input D.
7	Not applicable	DISABLE <sub>1</sub>	Input Disable 1. This pin disables the isolator inputs. Outputs take on the logic state determined by the fail-safe option.
9, 15	9, 15	GND <sub>2</sub>	Ground 2. Ground reference for Isolator Side 2.
10	7	NIC	No Internal Connection. Leave this pin floating.
Not applicable	10	V <sub>E2</sub>	Output Enable 2. Active high logic input. When V <sub>E2</sub> is high or disconnected, the V <sub>OA</sub> , V <sub>OB</sub> , V <sub>OC</sub> , and V <sub>OD</sub> outputs are enabled. When V <sub>E2</sub> is low, the V <sub>OA</sub> , V <sub>OB</sub> , V <sub>OC</sub> , and V <sub>OD</sub> outputs are disabled to the high-Z state.
11	11	V <sub>OD</sub>	Logic Output D.
12	12	V <sub>OC</sub>	Logic Output C.
13	13	V <sub>OB</sub>	Logic Output B.
14	14	V <sub>OA</sub>	Logic Output A.
16	16	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2.

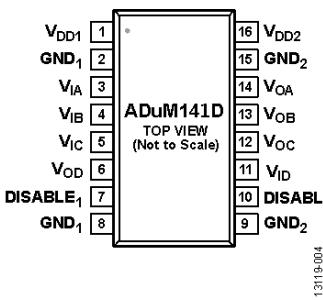


Figure 10. ADuM141D Pin Configuration

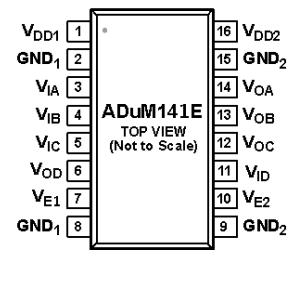


Figure 11. ADuM141E Pin Configuration

Reference the [AN-1109 Application Note](#) for specific layout guidelines.

**Table 19. Pin Function Descriptions**

Pin No.		Mnemonic	Description
ADuM141D	ADuM141E		
1	1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1.
2, 8	2, 8	GND <sub>1</sub>	Ground 1. Ground reference for Isolator Side 1.
3	3	V <sub>IA</sub>	Logic Input A.
4	4	V <sub>IB</sub>	Logic Input B.
5	5	V <sub>IC</sub>	Logic Input C.
6	6	V <sub>OD</sub>	Logic Output D.
7	Not applicable	DISABLE <sub>1</sub>	Input Disable 1. This pin disables the isolator inputs. Outputs take on the logic state determined by the fail-safe option.
Not applicable	7	V <sub>E1</sub>	Output Enable 1. Active high logic input. When V <sub>E1</sub> is high or disconnected, the V <sub>OD</sub> output is enabled. When V <sub>E1</sub> is low, the V <sub>OD</sub> output is disabled to the high-Z state.
9, 15	9, 15	GND <sub>2</sub>	Ground 2. Ground reference for Isolator Side 2.
10	Not applicable	DISABLE <sub>2</sub>	Input Disable 2. This pin disables the isolator inputs. Outputs take on the logic state determined by the fail-safe option.
Not applicable	10	V <sub>E2</sub>	Output Enable 2. Active high logic input. When V <sub>E2</sub> is high or disconnected, the V <sub>OA</sub> , V <sub>OB</sub> , and V <sub>OC</sub> outputs are enabled. When V <sub>E2</sub> is low, the V <sub>OA</sub> , V <sub>OB</sub> , and V <sub>OC</sub> outputs are disabled to the high-Z state.
11	11	V <sub>OD</sub>	Logic Output D.
12	12	V <sub>OC</sub>	Logic Output C.
13	13	V <sub>OB</sub>	Logic Output B.
14	14	V <sub>OA</sub>	Logic Output A.
16	16	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2.

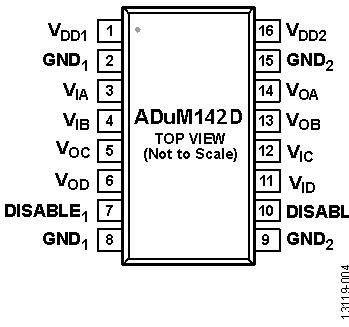


Figure 12. ADuM142D Pin Configuration

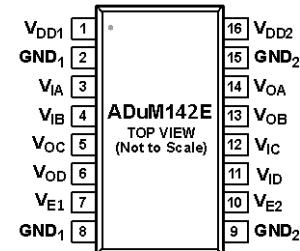


Figure 13. ADuM142E Pin Configuration

Reference the [AN-1109 Application Note](#) for specific layout guidelines.

Table 20. Pin Function Descriptions

Pin No.		Mnemonic	Description
ADuM142D	ADuM142E		
1	1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1.
2, 8	2, 8	GND <sub>1</sub>	Ground 1. Ground reference for Isolator Side 1.
3	3	V <sub>IA</sub>	Logic Input A.
4	4	V <sub>IB</sub>	Logic Input B.
5	5	V <sub>OC</sub>	Logic Output C.
6	6	V <sub>OD</sub>	Logic Output D.
7	Not applicable	DISABLE <sub>1</sub>	Input Disable 1. This pin disables the isolator inputs. Outputs take on the logic state determined by the fail-safe option.
Not applicable	7	V <sub>E1</sub>	Output Enable 1. Active high logic input. When V <sub>E1</sub> is high or disconnected, the V <sub>OD</sub> output is enabled. When V <sub>E1</sub> is low, the V <sub>OD</sub> and V <sub>OD</sub> outputs are disabled to the high-Z state.
9, 15	9, 15	GND <sub>2</sub>	Ground 2. Ground reference for Isolator Side 2.
10	Not applicable	DISABLE <sub>2</sub>	Input Disable 2. This pin disables the isolator inputs. Outputs take on the logic state determined by the fail-safe option.
Not applicable	10	V <sub>E2</sub>	Output Enable 2. Active high logic input. When V <sub>E2</sub> is high or disconnected, the V <sub>OA</sub> and V <sub>OB</sub> outputs are enabled. When V <sub>E2</sub> is low, the V <sub>OA</sub> and V <sub>OB</sub> outputs are disabled to the high-Z state.
11	11	V <sub>OD</sub>	Logic Output D.
12	12	V <sub>OC</sub>	Logic Output C.
13	13	V <sub>OB</sub>	Logic Output B.
14	14	V <sub>OA</sub>	Logic Output A.
16	16	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2.

## APPLICATIONS INFORMATION

### OVERVIEW

The [ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E](#) use a high frequency carrier to transmit data across the isolation barrier using *iCoupler* chip scale transformer coils separated by layers of polyimide isolation. Using an on-off keying (OOK) technique and the differential architecture shown in Figure 15 and Figure 16, the [ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E](#) have very low propagation delay and high speed. Internal regulators and input/output design techniques allow logic and supply voltages over a wide range from 1.7 V to 5.5 V, offering voltage translation of 1.8 V, 2.5 V, 3.3 V, and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and other techniques.

Figure 15 illustrates the waveforms for models of the [ADuM140D0/ADuM140E0/ADuM141D0/ADuM141E0/ADuM142D0/ADuM142E0](#) which have the condition of the fail-safe output state equal to low, where the carrier waveform is off when the input state is low. If the input side is off or not operating, the fail-safe output state of low ("0" in the part number) sets the output to low. For the [ADuM140D1/ADuM140E1/ADuM141D1/ADuM141E1/ADuM142D1/ADuM142E1](#) which have a fail-safe output state of high, Figure 16 illustrates the conditions where the carrier waveform is off when the input state is high. When the input side is off or not operating, the fail-safe output state of high ("1" in the part number) sets the output to high. See the Ordering Guide in the released products data sheets for the model numbers that have the fail-safe output state of low or the fail-safe output state of high.

### PCB LAYOUT

The [ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E](#) digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 14). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for  $V_{DD1}$  and between Pin 15 and Pin 16 for  $V_{DD2}$ . The recommended bypass capacitor value is between 0.01  $\mu$ F and 0.1  $\mu$ F. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 10 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 must also be considered, unless the ground pair on each package side is connected close to the package.

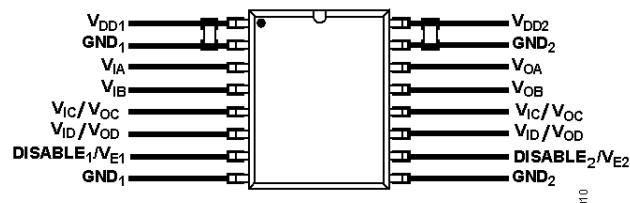


Figure 14. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the Absolute Maximum Ratings of the device, thereby leading to latch-up or permanent damage.

See the [AN-1109 Application Note](#) for board layout guidelines.

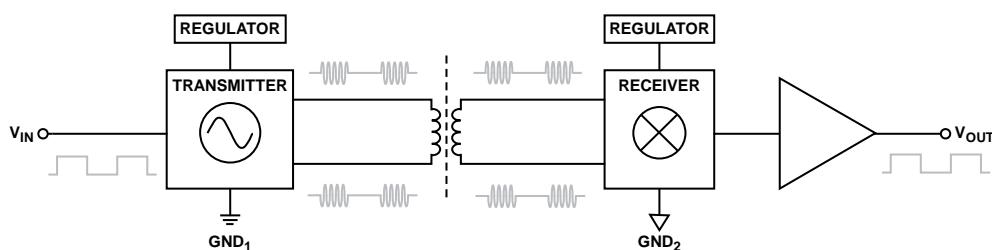


Figure 15. Operational Block Diagram of a Single Channel with a Low Fail-Safe Output State

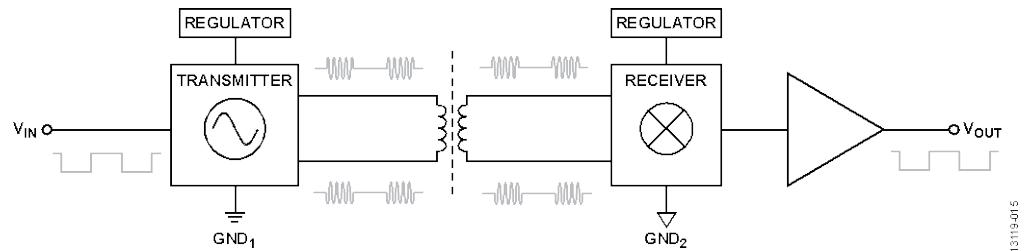


Figure 16. Operational Block Diagram of a Single Channel with a High Fail-Safe Output State

13119-015

## PROPAGATION DELAY RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a Logic 0 output may differ from the propagation delay to a Logic 1 output.

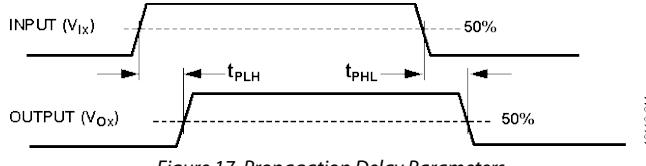


Figure 17. Propagation Delay Parameters

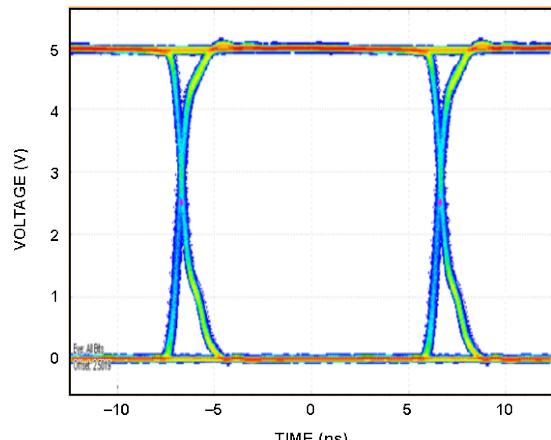
Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel matching is the maximum amount the propagation delay differs between channels within a single [ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142 D/ADuM142E](#) component.

Propagation delay skew is the maximum amount the propagation delay differs between multiple [ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM124 D/ADuM142E](#) components operating under the same conditions

## JITTER MEASUREMENT

Figure 18 shows the eye diagram for the [ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM124 D/ADuM142E](#). The measurement was taken using an Agilent 81110A pulse pattern generator at 150 Mbps with pseudorandom bit sequences (PRBS)  $2^{(n-1)}$ ,  $n = 14$ , for 5 V supplies. Jitter was measured with the Tektronix Model 5104B oscilloscope, 1 GHz, 10 GS/sec with the DPOJET jitter and eye diagram analysis tools. The result shows a typical measurement on the [ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142 D/ADuM142E](#) with 490 ps p-p jitter.

Figure 18.  
ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E  
Eye Diagram

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## INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking, and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

### Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components that allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and, therefore, can

provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group. The material group and creepage for the [ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E](#) isolators are presented in Table 9.

### **Insulation Wear Out**

The lifetime of insulation caused by wear out is determined by its thickness, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. It is the working voltage applicable to tracking that is specified in most standards.

Testing and modeling have shown that the primary driver of long-term degradation is displacement current in the polyimide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as: dc stress, which causes very little wear out because there is no displacement current, and an ac component time varying voltage stress, which causes wear out.

The ratings in certification documents are usually based on 60 Hz sinusoidal stress because this reflects isolation from line voltage. However, many practical applications have combinations of 60 Hz ac and dc across the barrier as shown in Equation 1. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as is shown in Equation 2. For insulation wear out with the polyimide materials used in these products, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\ RMS}^2 + V_{DC}^2} \quad (1)$$

or

$$V_{AC\ RMS} = \sqrt{V_{RMS}^2 - V_{DC}^2} \quad (2)$$

where:

$V_{AC\ RMS}$  is the time varying portion of the working voltage.

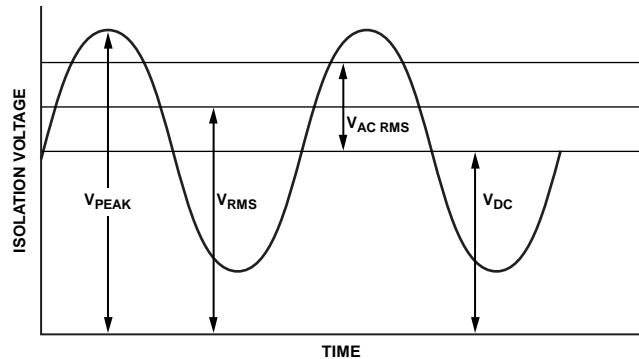
$V_{DC}$  is the dc offset of the working voltage.

$V_{RMS}$  is the total rms working voltage.

### **Calculation and Use of Parameters Example**

The following example frequently arises in power conversion applications. Assume that the line voltage on one side of the

isolation is 240 V<sub>AC</sub> rms and a 400 V<sub>DC</sub> bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage, clearance and lifetime of a device, see Figure 19 and the following equations.



1319-013

Figure 19. Critical Voltage Example

The working voltage across the barrier from Equation 1 is

$$V_{RMS} = \sqrt{V_{AC\ RMS}^2 + V_{DC}^2}$$

$$V_{RMS} = \sqrt{240^2 + 400^2}$$

$$V_{RMS} = 466 \text{ V}$$

This is the working voltage used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. To obtain the ac rms voltage, use Equation 2.

$$V_{AC\ RMS} = \sqrt{V_{RMS}^2 - V_{DC}^2}$$

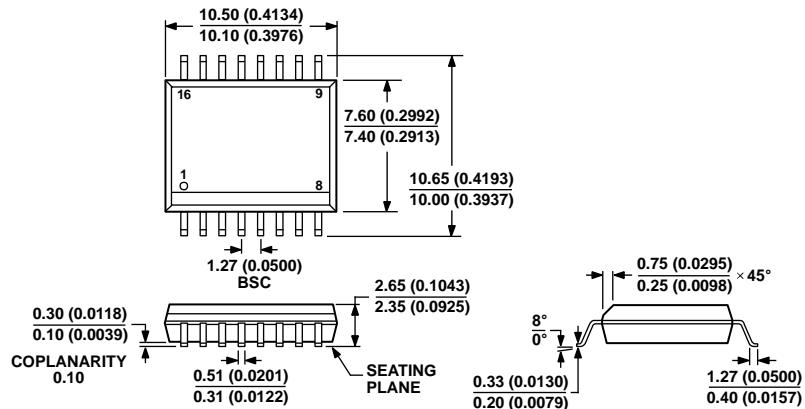
$$V_{AC\ RMS} = \sqrt{466^2 - 400^2}$$

$$V_{AC\ RMS} = 240 \text{ V rms}$$

In this case, the ac rms voltage is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. The value is compared to the limits for working voltage in Table 15 for the expected lifetime, less than a 60 Hz sine wave, and it is well within the limit for a 50-year service life.

Note that the dc working voltage limit in Table 15 is set by the creepage of the package as specified in IEC 60664-1. This value can differ for specific system level standards.

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

03-27-2007-B

Figure 20. 16-Lead Standard Small Outline Package [SOIC\_W]

Wide Body  
(RW-16)

Dimensions shown in millimeters and (inches)

To order either the ADuM140D or ADuM140E, see the [ADuM140D](#) or [ADuM140E](#) product page.