# LTC3330EUH
# Nanopower Buck-Boost DC/DC with Energy Harvesting Battery Life Extender

## DESCRIPTION

Demonstration Circuit 2048A is a nanopower buck-boost DC/DC with energy harvesting battery life extender featuring the LTC®3330. The LTC3330 integrates a high voltage energy harvesting power supply plus a DC/DC converter powered by a primary cell battery to create a single output supply for alternative energy applications. The energy harvesting power supply, consisting of an integrated low-loss full-wave bridge with a high voltage buck converter, harvests energy from piezoelectric, solar or magnetic sources. The primary cell input powers a buck-boost converter capable of operating down to 1.8V at its input. Either DC/DC converter can deliver energy to a single output. The buck operates when harvested energy is available, reducing the quiescent current drawn on the battery to essentially zero. The buck-boost takes over when harvested energy goes away.

A low noise LDO post regulator and a supercapacitor balancer are also integrated, accommodating a wide range of output storage configurations.

Voltage and current settings for both input and outputs are programmable via pin-strapped logic inputs.

The LTC3330EUH is available in a 5mm × 5mm 32-lead QFN surface mount package with exposed pad.

**Design files for this circuit board are available at http://www.linear.com/demo/DC2048A**



## BOARD PHOTO

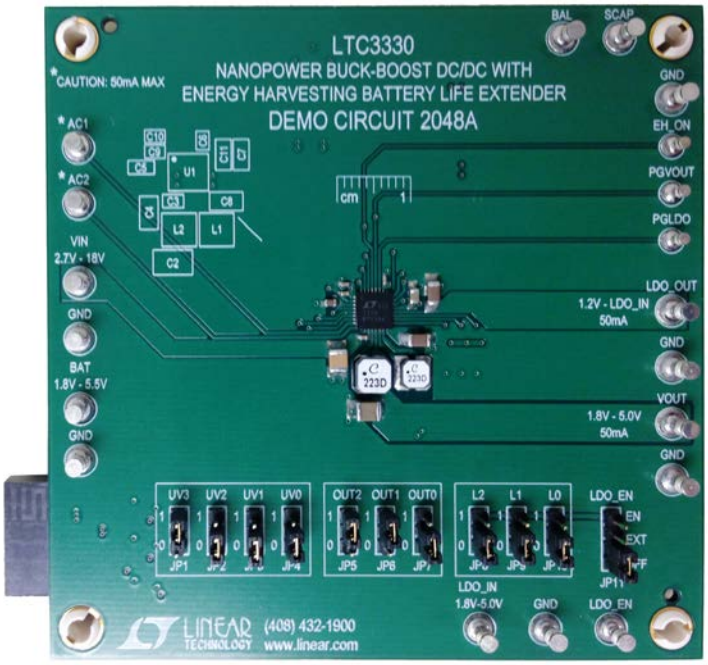


Figure 1. DC2048A Demo Board

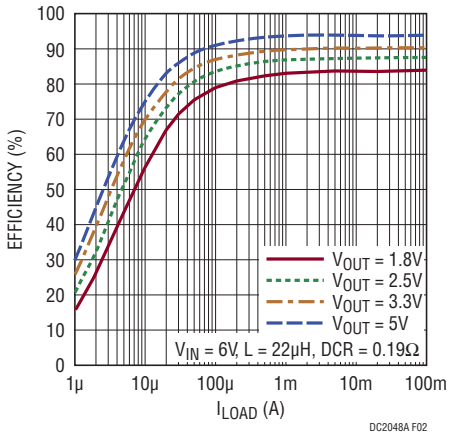


**Figure 2. Typical Efficiency of DC2048A. Buck Efficiency vs $I_{LOAD}$**

## PERFORMANCE SUMMARY

**Specifications are at $T_A$ = 25°C**

| SYMBOL | PARAMETER | CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| $V_{IN}$ | Input Voltage Range | | 3.0 | 18.0 | V |
| $V_{BAT}$ | Battery Voltage Range | | 1.8 | 5.5 | V |
| $V_{OUT}$ 1.8V | Output Voltage Range | OUT0 = 0, OUT1 = 0, OUT2 = 0 | 1.728 | 1.872 | V |
| $V_{OUT}$ 2.5V | Output Voltage Range | OUT0 = 1, OUT1 = 0, OUT2 = 0 | 2.425 | 2.575 | V |
| $V_{OUT}$ 2.8V | Output Voltage Range | OUT0 = 0, OUT1 = 1, OUT2 = 0 | 2.716 | 2.884 | V |
| $V_{OUT}$ 3.0V | Output Voltage Range | OUT0 = 1, OUT1 = 0, OUT2 = 0 | 2.910 | 3.090 | V |
| $V_{OUT}$ 3.3V | Output Voltage Range | OUT0 = 0, OUT1 = 0, OUT2 = 1 | 3.200 | 3.400 | V |
| $V_{OUT}$ 3.6V | Output Voltage Range | OUT0 = 1, OUT1 = 0, OUT2 = 1 | 3.492 | 3.708 | V |
| $V_{OUT}$ 4.5V | Output Voltage Range | OUT0 = 0, OUT1 = 1, OUT2 = 1 | 4.365 | 4.635 | V |
| $V_{OUT}$ 5.0V | Output Voltage Range | OUT0 = 1, OUT1 = 1, OUT2 = 1 | 4.850 | 5.150 | V |
| LDO 1.2V | LDO Voltage Range | LDO0 = 0, LDO1 = 0, LDO2 = 0 | 1.176 | 1.224 | V |
| LDO 1.5V | LDO Voltage Range | LDO0 = 1, LDO1 = 0, LDO2 = 0 | 1.470 | 1.530 | V |
| LDO 1.8V | LDO Voltage Range | LDO0 = 0, LDO1 = 1, LDO2 = 0 | 1.764 | 1.836 | V |
| LDO 2.0V | LDO Voltage Range | LDO0 = 1, LDO1 = 1, LDO2 = 0 | 1.960 | 2.040 | V |
| LDO 2.5V | LDO Voltage Range | LDO0 = 0, LDO1 = 0, LDO2 = 1 | 2.450 | 2.550 | V |
| LDO 3.0V | LDO Voltage Range | LDO0 = 1, LDO1 = 0 ,LDO2 = 1 | 2.940 | 3.060 | V |
| LDO 3.3V | LDO Voltage Range | LDO0 = 0, LDO1 = 1, LDO2 = 1 | 3.234 | 3.366 | V |
| LDO LD0_IN | LDO Voltage Range | LDO0 = 1, LDO1 = 1, LDO2 = 1 | | LDO_IN | V |

## OPERATING PRINCIPLE

Refer to the block diagram within the LTC3330 data sheet for its operating principle.

The LTC3330 combines a buck switching regulator and a buck-boost switching regulator to produce an energy harvesting solution with battery backup. The converters are controlled by a prioritizer that selects which converter to use based on the availability of a battery and/or harvestable energy. If harvested energy is available, the buck regulator is active and the buck-boost is off. With an optional LDO and supercapacitor balancer and an array of different configurations, the LTC3330 suits many applications.

The synchronous buck converter is an ultralow quiescent current power supply tailored to energy harvesting applications. It is designed to interface directly to a piezoelectric or alternative A/C energy source, rectify and store the harvested energy on an external capacitor while maintaining a regulated output voltage. It can also bleed off any excess input power via an internal protective shunt regulator.

An internal full-wave bridge rectifier accessible via AC1 and AC2 inputs, rectifies AC sources such as those from a piezoelectric element. The rectified output is stored on a capacitor at the $V_{IN}$ pin and can be used as an energy reservoir for the buck converter. The bridge rectifier has a total drop of about 800mV at typical piezo-generated currents, but is capable of carrying up to 50mA.

When the voltage on $V_{IN}$ rises above the UVLO rising threshold the buck converter is enabled and charge is transferred from the input capacitor to the output capacitor. When the input capacitor voltage is depleted below the UVLO falling threshold the buck converter is disabled.

These thresholds can be set according to Table 4 of the data sheet which offers UVLO rising thresholds from 4V to 18V with large or small hysteresis windows.

Two internal rails, CAP and $V_{IN2}$, are generated from $V_{IN}$ and are used to drive the high side PMOS and low side NMOS of the buck converter, respectively. Additionally the $V_{IN2}$

## OPERATING PRINCIPLE

rail serves as logic high for output voltage select bits UV [3:0]. The $V_{IN2}$ rail is regulated at 4.8V above GND while the CAP rail is regulated at 4.8V below $V_{IN}$. These are not intended to be used as external rails. Bypass capacitors should be connected to the CAP and $V_{IN2}$ pins to serve as energy reservoirs for driving the buck switches. When $V_{IN}$ is below 4.8V, $V_{IN2}$ is equal to $V_{IN}$ and CAP is held at GND. $V_{IN3}$ is an internal rail used by the buck and the buck-boost. When the LTC3330 runs the buck, $V_{IN3}$ will be a Schottky diode drop below $V_{IN2}$. When it runs as a buck-boost $V_{IN3}$ is equal to BAT.

The buck regulator uses a hysteretic voltage algorithm to control the output through internal feedback from the $V_{OUT}$ sense pin. The buck converter charges an output capacitor through an inductor to a value slightly higher than the regulation point. It does this by ramping the inductor current up to 250mA through an internal PMOS switch and then ramping it down to 0mA through an internal NMOS switch. When the buck brings the output voltage into regulation, the converter enters a low quiescent current sleep state that monitors the output voltage with a sleep comparator. During this operating mode, load current is provided by the buck output capacitor. When the output voltage falls below the regulation point, the buck regulator wakes up and the cycle repeats. This hysteretic method of providing a regulated output reduces losses associated with FET switching and maintains an output at light loads. The buck delivers a minimum of 100mA average load current when it is switching. $V_{OUT}$ can be set from 1.8V to 5.0V via the output voltage select bits OUT [2:0] according to Table 1 of the data sheet.

The buck-boost uses the same hysteretic algorithm as the buck to control the output, $V_{OUT}$, with the same sleep comparator. The buck-boost has three modes of operation; buck, buck-boost and boost. An internal mode comparator determines the mode of operation based on BAT and $V_{OUT}$. In each mode, the inductor current ramps up to $I_{PEAK}$ which is programmable via $I_{PK}$ [2:0]. See Table 3 of the data sheet.

An integrated low drop out regulator (LDO) is available with its own input, LDO_IN. It will regulate LDO_OUT to seven different output voltages based on the LDO [2:0] selection bits according to Table 2 of the data sheet. A mode is provided to turn the LDO into a current-limited switch in which the PMOS is always on. LDO_EN enables the LDO when high and when low, eliminates all quiescent current into LDO_IN. The LDO is designed to provide 50mA over a range of LDO_IN and LDO_OUT combinations. The LDO also features a 1ms soft-start for smooth output start-up.

Power good comparators, PGVOUT and PGLDO, produce a logic high referenced to highest of $V_{IN2}$, BAT and $V_{OUT}$ less a Schottky diode drop. PGVOUT and PGLDO will transition high the first time the respective converter reaches the programmed sleep threshold, signaling that the output is in regulation. The pin will remain high until the voltage falls to 92% of the desired regulated voltage.

An integrated supercapacitor balancer with 165nA of quiescent current is available to balance a stack of two supercapacitors. Typically the input, SCAP, will be tied to $V_{OUT}$ to allow for increased energy storage at $V_{OUT}$ with supercapacitors. The BAL pin is tied to the middle of the stack and can source or sink 10mA to regulate the BAL pin's voltage to half that of the SCAP voltage. To disable the balancer and its associated quiescent current, the SCAP and BAL pins can be tied to ground.

## QUICK START PROCEDURE

Using short twisted pair leads for any power connections, with all loads and power supplies off, refer to Figure 3 for the proper measurement and equipment setup.

Follow the procedure below:

1. Before connecting PS1 to the DC2048A, PS1 must have its current limit set to 300mA and PS2 must have its current limit set to 500mA. For most power supplies with a current limit adjustment feature the procedure to set the current limit is as follows. Turn the voltage and current adjustment to minimum. Short the output terminals and turn the voltage adjustment to maximum. Adjust the current limit to 300mA for PS1 and 500mA for PS2. Turn the voltage adjustment to minimum and remove the short between the output terminals. The power supply is now current limited to 300mA and 500mA respectively.

   Verify that there is not a battery installed in the BH1 battery holder.

2. Initial Jumper, PS and LOAD settings:

   **JP1** = 0 **JP2** = 0 **JP3** = 0 **JP4** = 0

   **JP5** = 0 **JP6** = 0 **JP7** = 0

   **JP8** = 0 **JP9** = 0 **JP10** = 0

   **JP11** = OFF

   **PS1** = OFF **PS2** = OFF

   **LOAD1** = OFF **LOAD2** = OFF

3. Connect PS1 to the $V_{IN}$ terminals, then turn on PS1 and slowly increase voltage to 2.0V while monitoring the input current. If the current remains less than 5mA, increase PS1 to 5.0V.

4. Set LOAD1 to 50mA. Verify voltage on $V_{OUT}$ is within the $V_{OUT}$ 1.8V range in Table 1. Verify that the output ripple voltage is between 20mV and 60mV. Verify that PGVOUT is high. Decrease LOAD1 to 5mA.Verify that PGVOUT is high. Decrease PS1 to 0V.

5. Set JP1, JP2, JP3, JP4 to 1. Slowly increase PS1 to 16V and verify that $V_{OUT}$ is off. Increase PS1 to 19V and verify that $V_{OUT}$ is within the $V_{OUT}$ 1.8V range of Table 1.

6. Decrease PS1 to 0V and disconnect PS1 from $V_{IN}$. Set the current limit of PS1 to 25mA as described above.

7. Connect PS1 to AC1 and slowly increase PS1 voltage to 2.0V while monitoring the input current. If the current remains less than 5mA, increase PS1 to 19V. Verify voltage on $V_{OUT}$ is within the $V_{OUT}$ 1.8V range in Table 1.Decrease PS1 to 0V, swap the AC1 connection to AC2 and repeat the test. Decrease PS1 to 0V and disconnect PS1 from AC2.

8. Set JP5 to 1, JP6 to 1, and JP7 to 1. Connect PS1 to the $V_{IN}$ turret. Increase PS1 to 19V and set LOAD1 to 50mA. Verify voltage on $V_{OUT}$ is within the $V_{OUT}$ 5.0V range in Table 1. Verify that the output ripple voltage is between 20mV to 60mV. Set PS1 to 0V and disconnect PS1.

9. Set JP1 to 1; JP2, JP3, JP4 and JP5 to 0; JP6 and JP7 to 1; PS1 to 0V and disconnect PS1. Connect PS2 to the BAT Terminals, then turn on PS2 and slowly increase voltage to 1.0V while monitoring the input current. If the current remains less than 5mA, increase PS2 to 2.0V. Verify voltage on $V_{OUT}$ is within the $V_{OUT}$ 3.0V range in Table 1. Verify that the output ripple voltage is between 20mV to 60mV.

10. Increase PS2 to 3.0V. Verify voltage on $V_{OUT}$ is within the $V_{OUT}$ 3.0V range in Table 1. Verify that the output ripple voltage is between 20mV to 60mV.

11. Increase PS2 to 5.0V. Verify voltage on $V_{OUT}$ is within the $V_{OUT}$ 3.0V range in Table 1. Verify that the output ripple voltage is between 20mV to 60mV. Decrease PS2 to 0V and disconnect PS2.

12. Set the current limit of PS1 to 300mA as described above. Connect PS1 to the $V_{IN}$ terminals. Set JP5 to 1, JP6 to 1 and JP7 to 1. Set PS1 to 14V.Connect a jumper lead from $V_{OUT}$ to LDO_IN. Verify that LDO is off. Move JP11 jumper to EN and verify that LDO_OUT is now 1.2V. Increase Load 2 to 50mA and verify than LDO is within the 1.2V range in Table 1. Verify that PGLDO is high.

13. Set JP8 to 1, JP9 to 1, JP10 to 1, verify that LDO_OUT is slightly below $V_{OUT}$. Verify that PGLDO is low.

## QUICK START PROCEDURE

14. Add a jumper lead from $V_{OUT}$ to SCAP. Verify that BAL is approximately ½ of $V_{OUT}$.
15. Set JP8 to 0, JP9 to 0 and JP10 to 0 and verify that LDO_OUT is now 1.2V. Quickly remove PS1 + lead from $V_{IN}$ and verify that LDO_OUT remains at 1.2V for approximately 5 seconds.
16. Turn off PS1, PS2, LOAD1 and LOAD2.

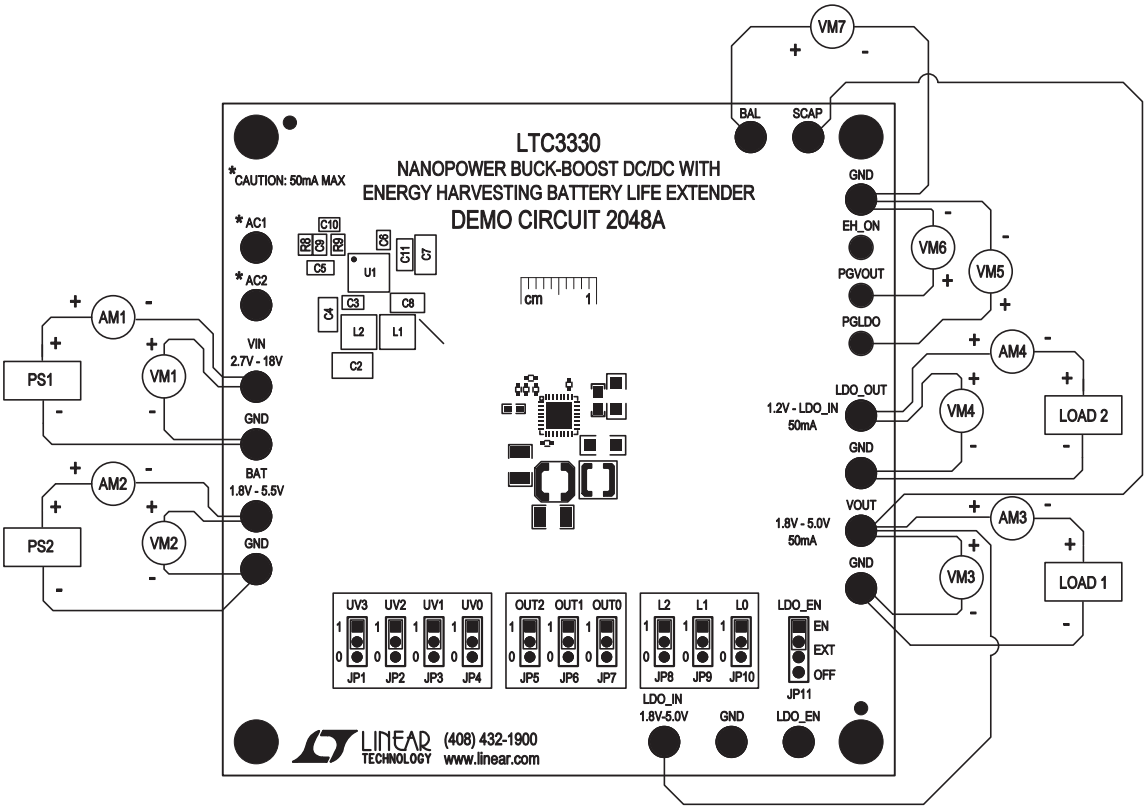


**Figure 3. Proper Measurement Equipment Setup**

## CONNECTION TO A DUST MOTE (DC9003A-B)

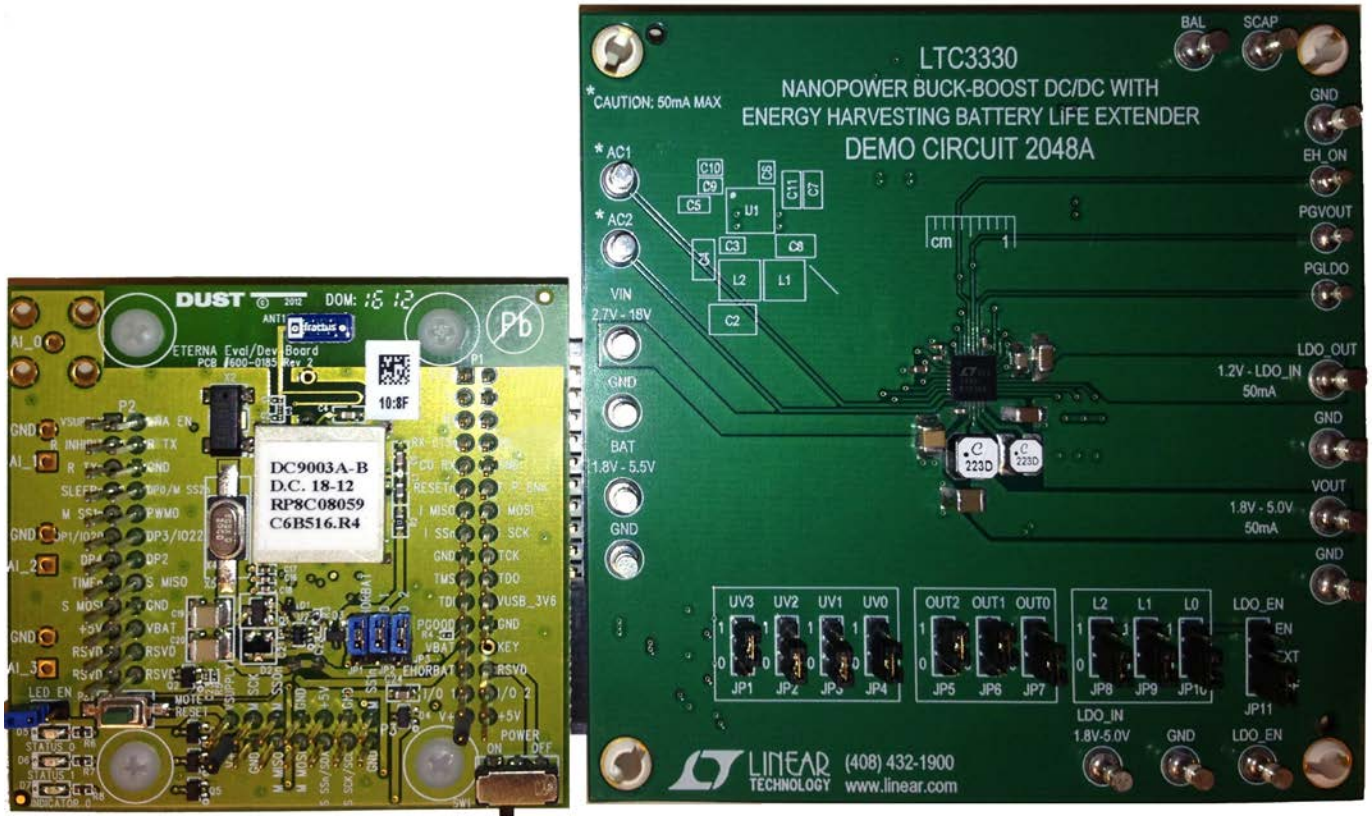


**Figure 4. DC2048A with Dust™ Mote**

Remove the battery from the BH1 holder on the bottom side of the DC2048A. Attach a Dust mote to J1 of the DC2048A, refer to Figure 4 for the proper setup. J1 is a keyed connector and is connected to the left side of the P1 connector on the Dust mote. Figure 12 is a schematic of the Dust mote and the DC2048A interconnections plus three extra connections which; 1) connect the SCAP to $V_{OUT}$, 2) connect BAL to the middle of the supercapacitors and 3) connect EH_ON to OUT2. The DC2048A contains NC7SZ58P6X universal configurable 2-input logic gates that are input voltage tolerant and allow level shifting between the LTC3330 and the Dust mote.

On the DC2048A set JP1 to 0, JP2 to 0, JP3 to 1, JP4 to 0, JP5 to 1, JP6 to 0, JP7 to 0, JP8, JP9 and JP10 to 0, JP11 to OFF.

### Piezoelectric Transducer Evaluation

Mount a series connected MIDE V25W to a vibration source and connect the electrical connections to the AC1 and AC2 turrets. Activate the vibration source to an acceleration of 1G and a frequency of 60Hz. Figure 5 shows an open circuit voltage of 10.6V for the Mide V25W piezoelectric device that was tuned to 60Hz. In order to set the VIN_UVLO_RISING and VIN_UVLO_FALLING thresholds, the open circuit voltage of the piezoelectric device must be measured. The internal bridge network of the LTC3330 will have approximately 800mV drop at an input current of 300µA.

The peak power load voltage of a purely resistive source is at one half (½) of the rectified no load voltage. In this case, the optimal average input voltage regulation level would be 4.9V. Using a VIN_UVLO_RISING threshold of 6V and a VIN_UVLO_FALLING threshold of 5V (UV3 = 0, UV2 = 0, UV1 = 1, UV0 = 0) yields an average input voltage close to the theoretical optimal voltage.

## CONNECTION TO A DUST MOTE (DC9003A-B)

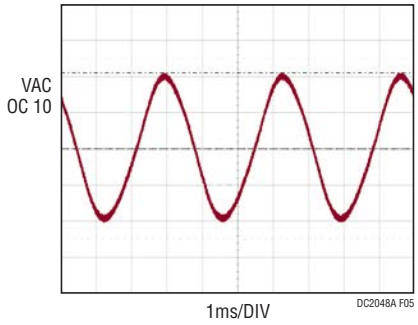


**Figure 5. MIDE V25W Open Circuit AC Voltage with $1g_{rms}$, 60Hz Acceleration Applied**

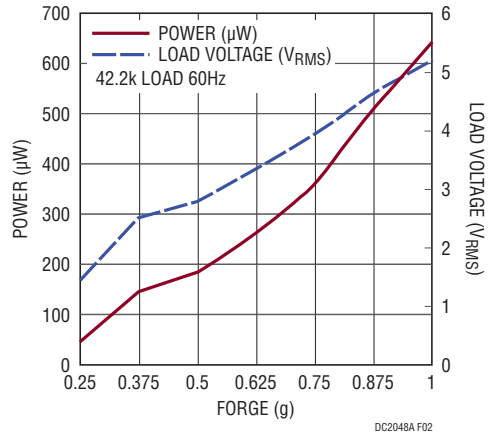


**Figure 6. Mide V25W Output Power Into a 42.2kΩ Load with $1g_{rms}$, 60Hz Acceleration Applied to the Mide V25W Piezoelectric Transducer, [$\sqrt{2}$ • sin(2π • 60Hz • t)]**

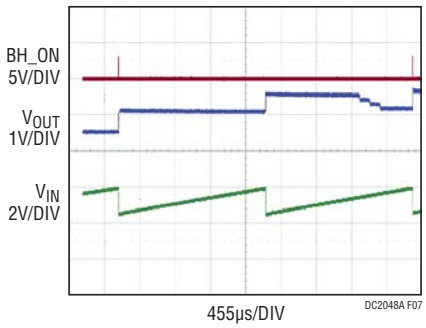


**Figure 7. Mide V25W Charging the 18µF Input Capacitance from 4.48V to 5.92V in 208ms**

Figure 6 is a plot of the output power and load voltage of the V25W piezoelectric transducer into a 42.2kΩ load for various rms acceleration levels. The output power compares well with the input power that is charging $C_{IN}$ during the sleep cycle between VIN_UVLO_FALLING and VIN_UVLO_RISING thresholds at an acceleration force of 1grms, shown in Figure 7.

In Figure 7, the input capacitor is being recharged from the V25W piezoelectric transducer. The input capacitor is charging from 4.48V to 5.92V in 208 milli-seconds. The power delivered from the V25W is 648µW.

Assuming that the circuit is configured as shown in Figure 8, it will take a significant amount of time for the piezo transducer to charge the 0.09F supercapacitor on the output of the LTC3330. As used above, the 22µF input capacitor is only 18µF at an applied voltage of 5V, so every VIN_UVLO_RISING and FALLING event produces 26 micro-coulombs [(5.92V – 4.48V) • 18µF)] that may be transferred from the input capacitor to the output capacitor, minus the losses of the buck regulator in the LTC3330. The buck regulator efficiency is approximately 90% at $V_{IN}$ equal to 5V and $V_{OUT}$ between 2.5V and 3.6V. Thus, for every UVLO event, 23.3 microcoulombs are added to the output supercapacitor. Given a 0.09F output supercapacitor charging to 3.6V, 324 millicoulombs are required to fully charge the supercapacitor. Assuming no additional load on the output, it takes 13,906 (.324/23.3e-6) UVLO events to charge the output supercapacitor to 3.6V. From Figure 7, it can be observed that each VIN_UVLO event takes 208ms so the total time to charge the output capacitor from 0V to 3.6V will be greater than 2900s. Figure 9 shows the no load charging of the output supercapacitor, which takes approximately 3300s. The above calculation neglects the lower efficiency at low output voltages and the time it takes to transfer the energy from the input capacitor to the output supercapacitor so predicting the actual value within –12% is to be expected.

## CONNECTION TO A DUST MOTE (DC9003A-B)

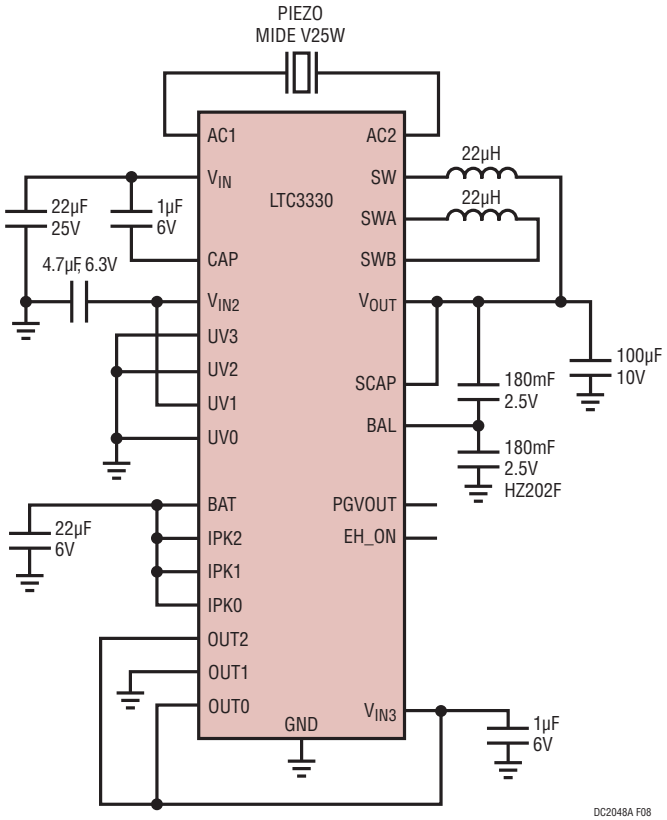


**Figure 8. LTC3330 Circuit Charging Supercapacitor at No Load without a Battery ($V_{OUT}$ = 3.6V)**

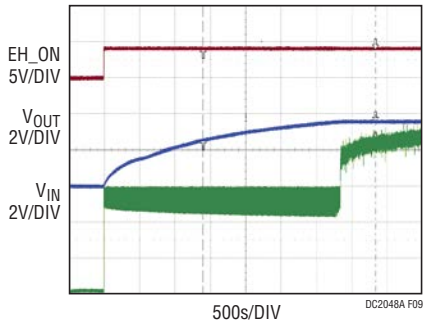


**Figure 9. Scope Shots of LTC3330 Charging Supercapacitor at No Load without a Battery ($V_{OUT}$ = 3.6V)**

## CONNECTION TO A DUST MOTE (DC9003A-B)

Figure 10 shows the LTC3330 with a supercapacitor on the output, a battery installed and the output voltage set to 3.6V. The scope shots in Figure 11 were taken after applying a pulsed load of 15mA for 10ms. With the battery attached and a pulsed load applied, the EH_ON signal will switch back and forth from high to low every time the $V_{IN}$ voltage transitions from the VIN_UVLO_RISING to VIN_UVLO_FALLING threshold. When the pulsed load is applied, the output capacitor is depleted slightly and the input capacitor must recharge the output cap. Because the input capacitance is much less than the output capacitance, the input capacitor will go through many UVLO transitions to charge the output capacitor back up to the sleep threshold. Once the output is charged to the output sleep threshold, the EH_ON signal will again be consistently high indicating that the energy harvesting source is powering the output.

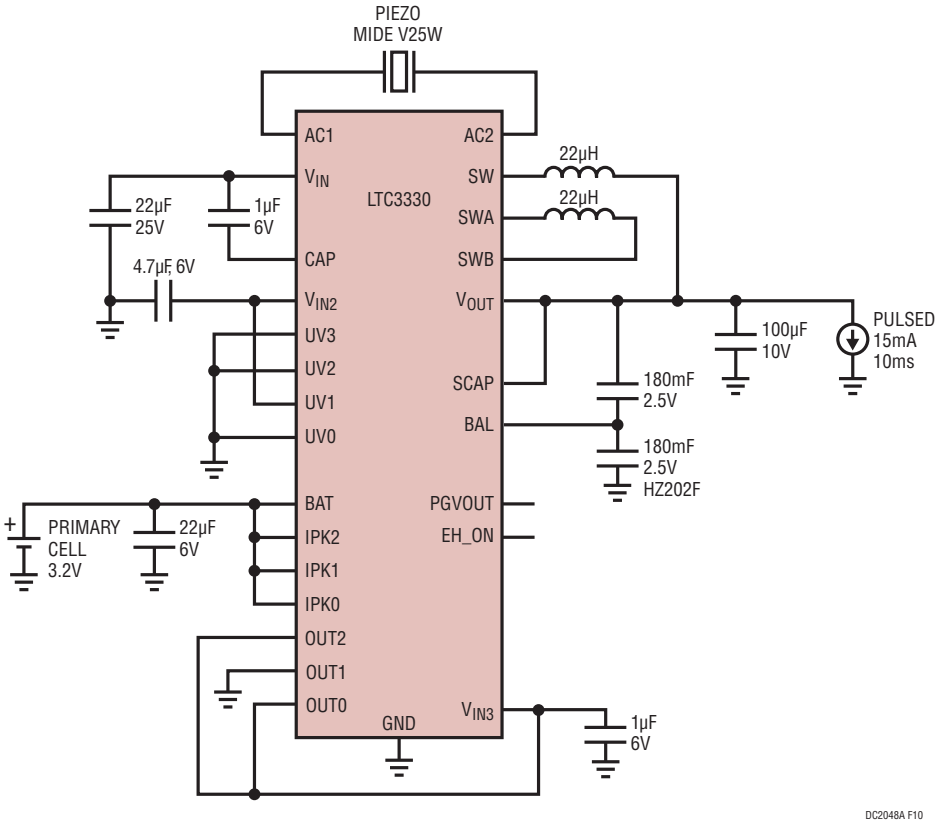


**Figure 10. LTC3330 Circuit with a Supercapacitor, a Battery Installed and a Pulsed Load Applied ($V_{OUT}$ = 3.6V)**

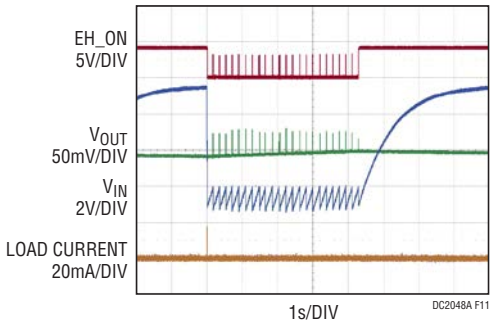


**Figure 11. Charging a Supercapacitor with a Battery Installed and a Pulsed Load ($V_{OUT}$ = 3.6V)**

## CONNECTION TO A DUST MOTE (DC9003A-B)

Figure 12 shows the LTC3330 with an output supercapacitor, a Dust mote attached, a battery installed and EH_ON connected to OUT2. In this configuration, when EH_ON is low, $V_{OUT}$ will be set to 2.5V and when EH_ON is high, $V_{OUT}$ will be set to 3.6V. The first marker in Figure 13 is where the vibration source was activated; $V_{IN}$ then rises above the VIN_UVLO_RISING threshold. EH_ON will then go high causing $V_{OUT}$ to rise towards 3.6V ($V_{OUT}$ started at 2.5V because the battery had charged it up initially). At the same time EH_ON goes high, PGVOUT will go low, since the new $V_{OUT}$ level of 3.6V has not been reached. As the charge on $V_{IN}$ is being transferred to $V_{OUT}$, $V_{IN}$ is discharging and when $V_{IN}$ reaches its UVLO_FALLING threshold, EH_ON will go low, causing the targeted $V_{OUT}$ to again be 2.5V. Given that the output capacitor is very large and the average load is less than the input power supplied by the Mide piezoelectric transducer, the output voltage will increase to the higher set-point of 3.6V over many cycles. During the transition from the BAT set-point of 2.5V to the energy harvester set-point of 3.6V, $V_{OUT}$ is above the 2.5V PGVOUT threshold, hence, PGVOUT will go high every time EH_ON goes low. This cycle will be repeated until $V_{OUT}$ reaches the PGVOUT threshold for the $V_{OUT}$ setting of 3.6V. When a pulse load is applied that is greater than the energy supplied by the input capacitor, VIN will drop below the VIN_UVLO_FALLING threshold, EH_ON will go low and the buck-boost regulator will be ready to support the load requirement from the battery, but will not start to switch until the supercapacitor is discharged to 2.5V. In this way, the circuit can store a lot of harvested energy and use it for an extended period of time before switching over to the battery energy. The supercapacitor could be sized to accommodate known repeated periods of time that the energy harvester source will not be available, such as overnight when a vibrating machine is turned off or in the case of a solar application, when the lights are turned off or the sun goes down.

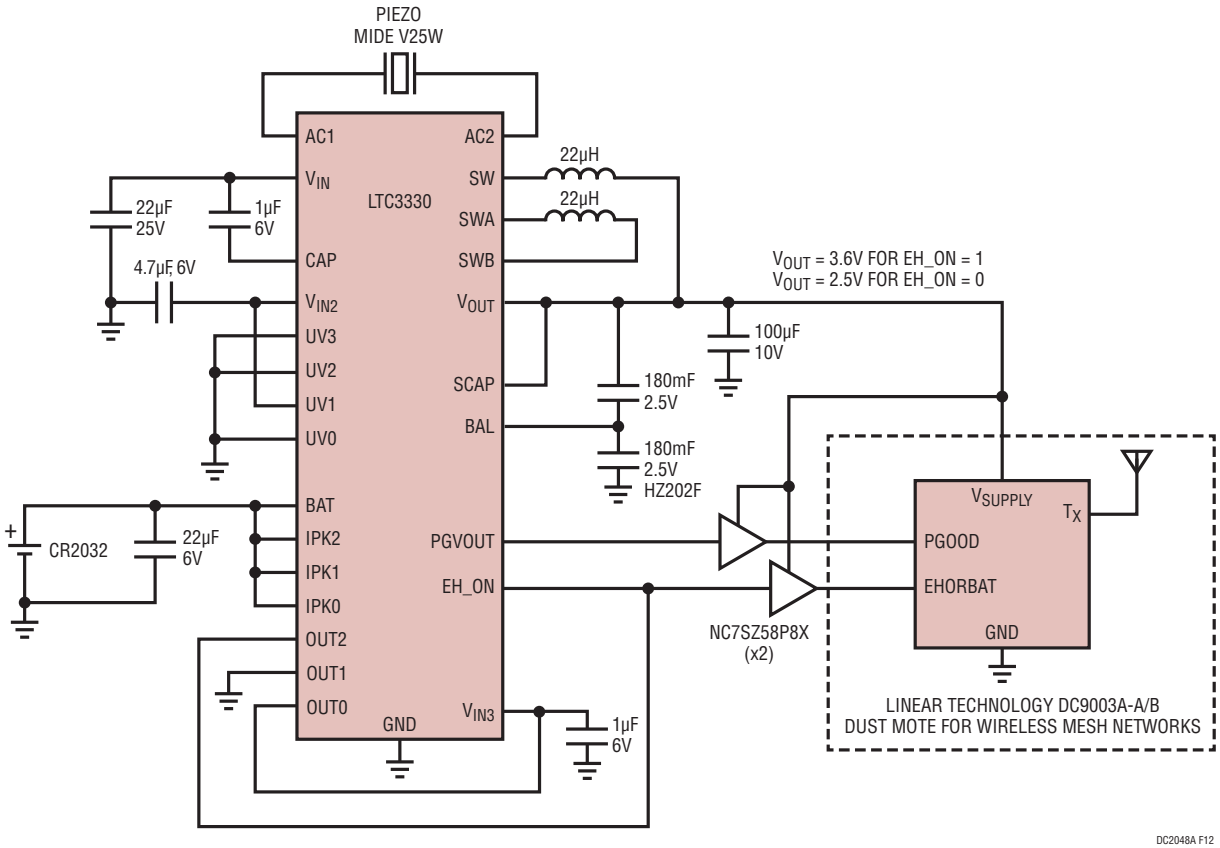


**Figure 12. Dust Mote Setup with a Supercapacitor, a Battery and EH_ON Connected to OUT2**

## CONNECTION TO A DUST MOTE (DC9003A-B)

While the EH_ON signal is low the buck-boost circuit will consume 750nA from the battery in the sleeping state. The effects of a pulsed load are shown in Figure 13 at approximately 1850s, where $V_{IN}$ is discharged and the EH_ON signal pulses low to high for a brief period of time, which occurred as a result of the Dust mote radio making a data transmission.

Figure 14 shows the discharging of $V_{OUT}$ when the vibration source is removed and $V_{IN}$ drops below the UVLO_FALLING threshold causing EH_ON to go low. The supercapacitor on $V_{OUT}$ will discharge down to the new target voltage of 2.5V at which point the buck-boost regulator will turn on supplying power to the Dust mote. The discharging of the supercapacitor on $V_{OUT}$ provides an energy source for short term loss of the vibration source and extends the life of the battery.

Figure 15 is the same Dust mote configuration as Figure 12 but without the output supercapacitor. Figure 16 shows the charging of the output without the supercapacitor attached.

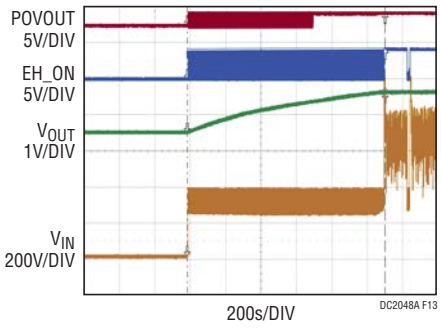


**Figure 13. Mide 25W Charging Output Supercapacitor from 2.5V to 3.6V with Dust Mote Attached**

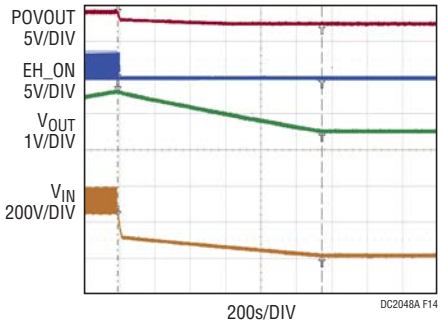


**Figure 14. Output Supercapacitor Discharging When the Vibration Source Is Switched Off**

## CONNECTION TO A DUST MOTE (DC9003A-B)

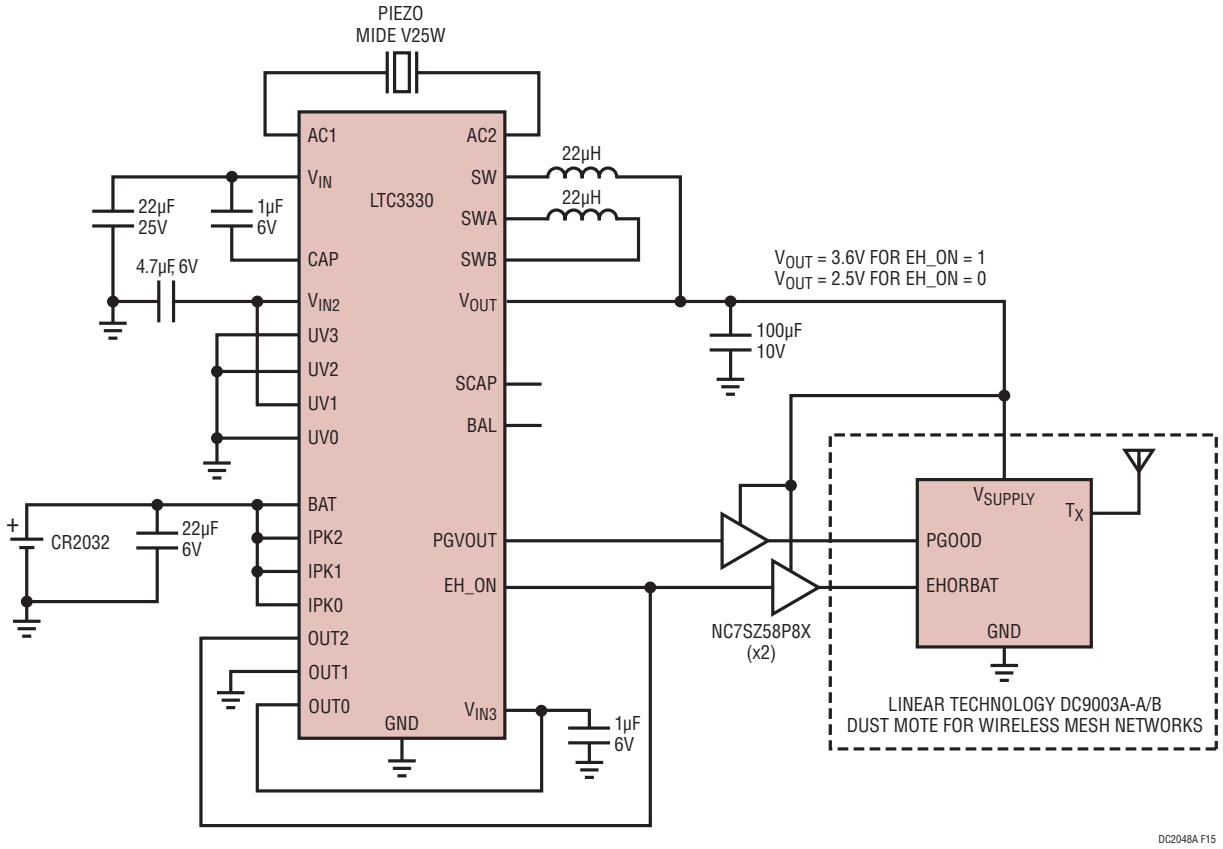


**Figure 15. Dust Mote Setup without a Supercapacitor and with EH_ON Connected to OUT2**

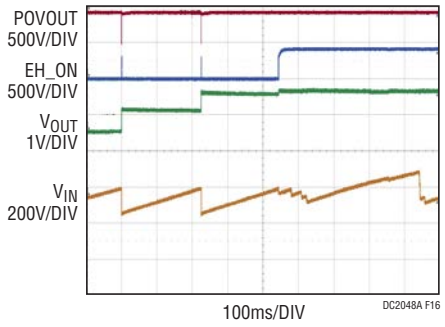


**Figure 16. Output Voltage Charging with Dust Mote Attached without Supercapacitor**

## PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
|---|---|---|---|---|
| **Required Circuit Components** | | | | |
| 1 | 1 | BAT1 | CR2032 COIN LI-ION BATTERY | DURACELL, CR2032 |
| 2 | 1 | BTH1 | SMT, CR2032 BATTERY HOLDER | MPD INC, BU2032SM-HD-GCT-ND |
| 3 | 1 | C1 | SUPERCAP, 90mF, 5.5V, 20mm × 15mm | CAP-XX, HZ202F |
| 4 | 1 | C2 | CAP, CHIP, X5R, 100µF, 20%, 10V, 1210 | TAIYO YUDEN, LMK325ABJ107MM |
| 5 | 2 | C7, C8 | CAP, CHIP, X5R, 22µF, 20%, 6.3V, 1206 | TAIYO YUDEN, JMK316BJ226ML-T |
| 6 | 2 | C3, C6 | CAP, CHIP, X5R, 1µF, 10%, 6.3V, 0402 | TDK, C1005X5R0J105KT |
| 7 | 1 | C11 | CAP, CHIP, X5R, 10µF, 10%, 6.3V, 0805 | AVX, 08056D106KAT2A |
| 8 | 1 | C4 | CAP, CHIP, X5R, 22µF, 10%, 25V, 1210 | AVX, 12103D226KAT1A |
| 9 | 1 | C5 | CAP, CHIP, X5R, 4.7µF, 10%, 6.3V, 0603 | TDK, C1608X5R0J475KT |
| 10 | 2 | C9, C10 | CAP, CHIP, X5R, 0.1µF, 10%, 10V, 0402 | TDK, C1005X5R1A104K |
| 11 | 1 | L1 | INDUCTOR, 22µH, 0.35A, 1.9Ω, 4.1mm × 4.1mm | COILCRAFT, LPS4018-223MLC |
| 12 | 1 | L2 | INDUCTOR, 22µH, 0.75A, 0.19Ω, 4.8mm × 4.8mm | COILCRAFT, LPS5030-223MLC |
| 13 | 3 | R2, R4, R6 | RES, CHIP, 0Ω, 0603 | VISHAY, CRCW06030000FKED |
| 14 | 0 | R3, R5, R7 | RES, CHIP, 0Ω, 0603 | VISHAY, CRCW06030000FKED |
| 15 | 2 | R8, R9 | RES, CHIP, 7.5k, 1/16W,1%,0402 | VISHAY, CRCW04027K50FKED |
| 16 | 1 | U1 | ENERGY HARVESTING DC/DC WITH BATTERY B | LINEAR TECH, LTC3330EUH |
| **Additional Demo Board Circuit Components** | | | | |
| 1 | 0 | BTH2 | SMT, CR2477 BATTERY HOLDER | RENATA, SMTU2477-1 |
| 2 | 1 | R1 | RES,CHIP, 1k, 1/16W, 1%, 0402 | VISHAY, CRCW04021K00FKED |
| 3 | 3 | U2, U3, U4 | IC, UHS UNIV. CONFIG. TWO-INPUT GATES, SC | FAIRCHILD, NC7SZ58P6X |
| **Hardware: For Demo Board Only** | | | | |
| 1 | 15 | E1-E8, E12-E19 | TURRET, 0.09 DIA | MILL-MAX, 2501-2 |
| 2 | 3 | E9-E11 | TURRET, 0.061 DIA | MILL-MAX, 2308-2 |
| 3 | 1 | J1 | HEADER, 12 PIN, DUST HEADER 2×6 | SAMTEC, SMH-106-02-L-D-05 |
| 4 | 10 | JP1-JP10 | HEADER, 3 PINS, 2mm | SAMTEC, TMM-103-02-L-S |
| 5 | 1 | JP11 | HEADER, 4 PINS, 2mm | SAMTEC, TMM-104-02-L-S |
| 6 | 11 | JP1-JP11 | SHUNT 2MM | SAMTEC, 2SN-BK-G |

## SCHEMATIC DIAGRAM

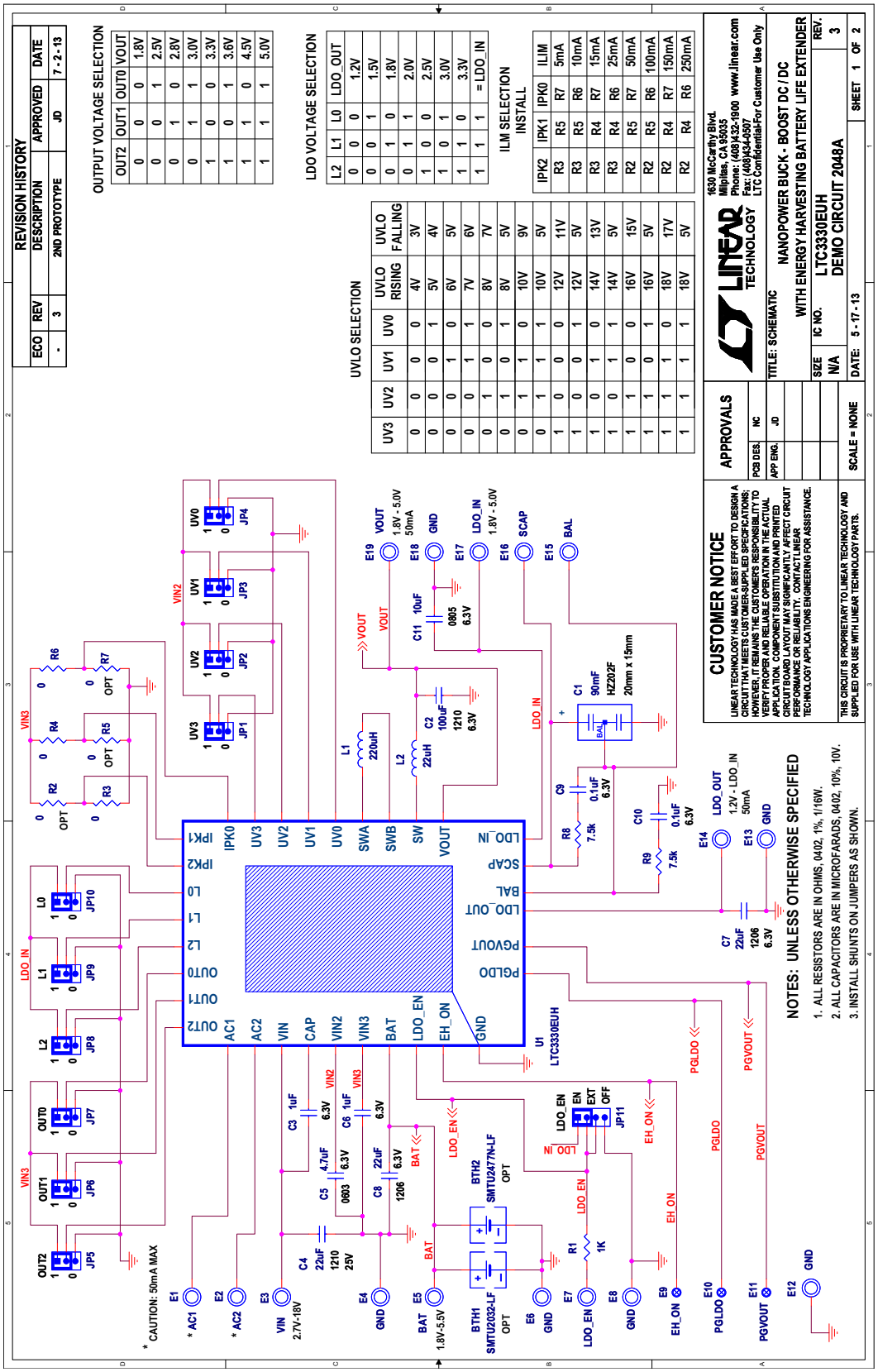


Figure 17. DC2048A Demo Circuit Schematic

## SCHEMATIC DIAGRAM

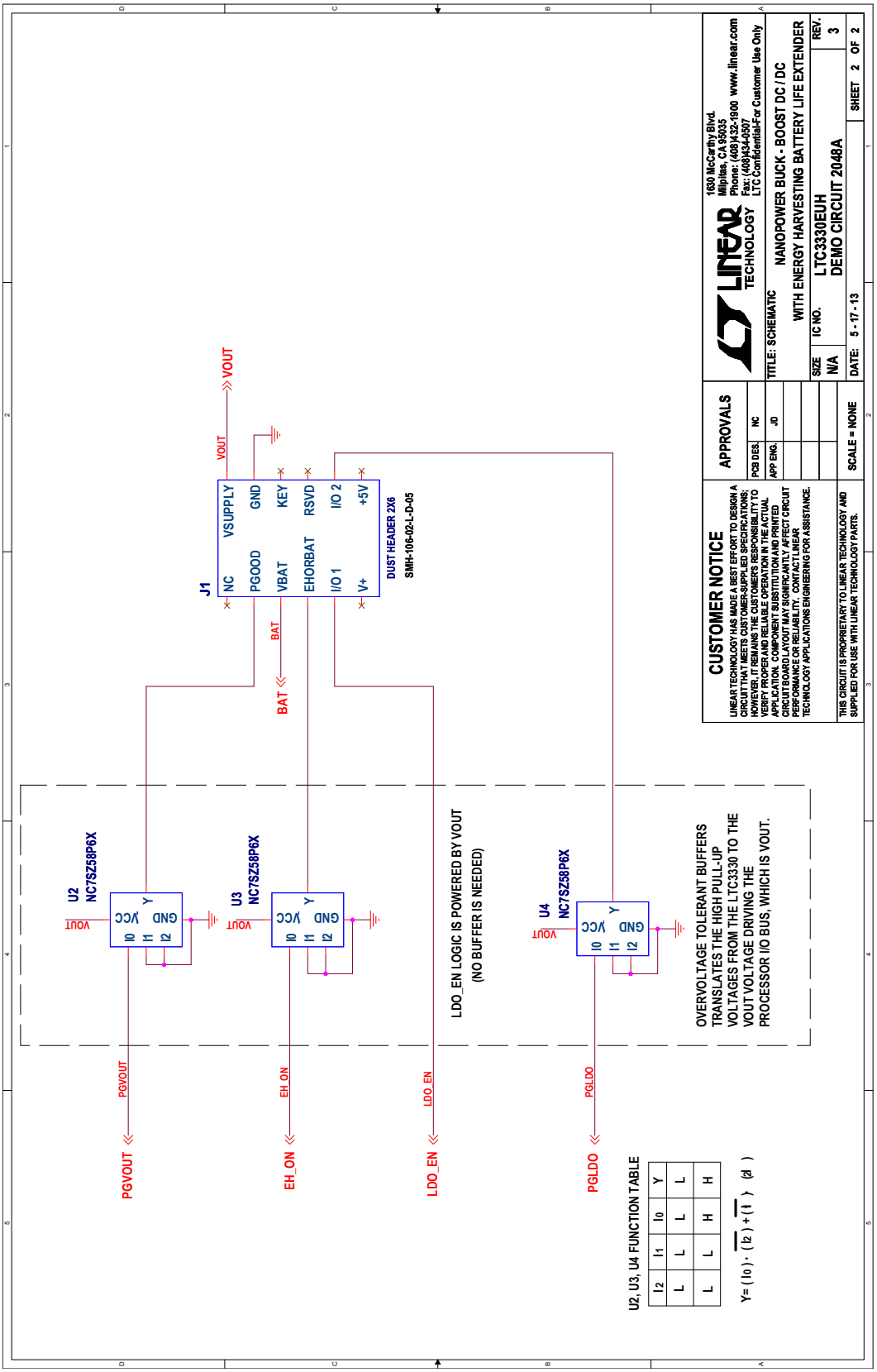


Figure 18. DC2048A Demo Circuit Schematic

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