HMC541LP3 / 541LP3E

v01.1005

10 dB GaAs MMIC 1-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, DC - 5 GHz

Typical Applications

The HMC541LP3 / HMC541LP3E is ideal for both RF and IF applications:

- Cellular Infrastructure
- ISM, MMDS, WLAN, WiMAX, WiBro
- Microwave Radio & VSAT
- Test Equipment and Sensors

Features

± 0.2 dB Typical Step Error

Low Insertion Loss: 1 dB

High IP3: +50 dBm

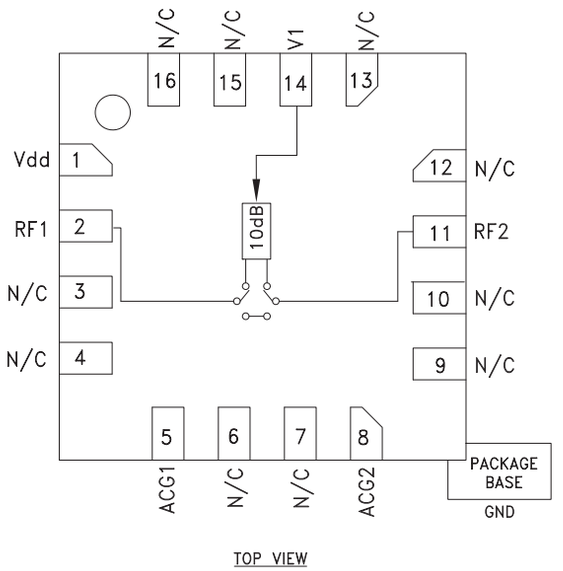
Single Control Line

TTL/CMOS Compatible Control

Single +5V Supply

3x3 mm SMT Package

Functional Diagram



TOP VIEW

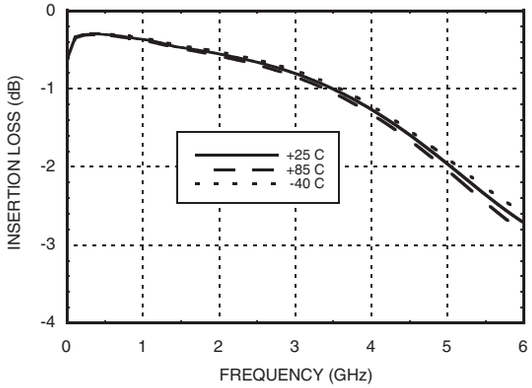
General Description

The HMC541LP3 & HMC541LP3E are broadband 1-bit GaAs IC digital attenuators in low cost leadless surface mount packages. This single positive control line digital attenuator utilizes off chip AC ground capacitors for near DC operation, making it suitable for a wide variety of RF and IF applications. Covering DC to 5 GHz, the insertion loss is less than 1 dB typical. Attenuation accuracy is excellent at ± 0.2 dB typical step error. The attenuator also features a high IIP3 of +50 dBm. One TTL/CMOS control input is used to select the attenuation state. A single Vdd bias of +5V is required.

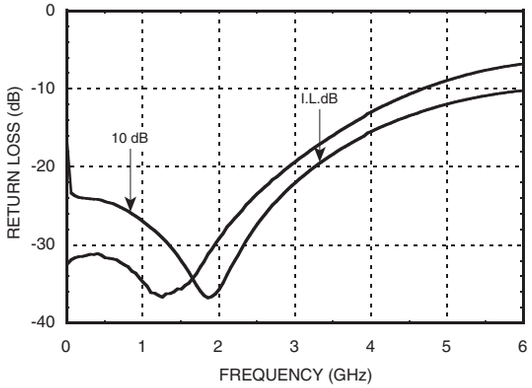
Electrical Specifications, T_A = +25° C, With Vdd = +5V & Vctl = 0/+5V (Unless Otherwise Noted)

Parameter	Frequency (GHz)	Min.	Typ.	Max.	Units
Insertion Loss	DC - 2.0 GHz 2.0 - 3.5 GHz 3.5 - 5.0 GHz		0.5 1.0 2.0	0.8 1.3 2.3	dB dB dB
Attenuation Range	DC - 5 GHz		10		dB
Return Loss (RF1 & RF2, All Atten. States)	DC - 2.5 GHz 2.5 - 5.0 GHz		25 15		dB dB
Attenuation Accuracy: (Referenced to Insertion Loss)	DC - 5 GHz		± 0.4 Max.		dB
Input Power for 0.1 dB Compression	0.1 - 5.0 GHz		27		dBm
Input Third Order Intercept Point (Two-Tone Input Power= 0 dBm Each Tone)	0.1 - 5.0 GHz		50		dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)	DC - 5 GHz		 20 23		 ns ns

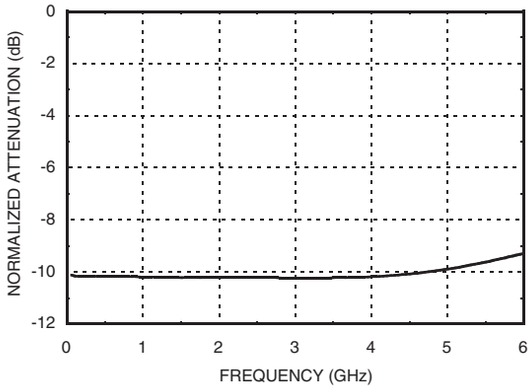
Insertion Loss



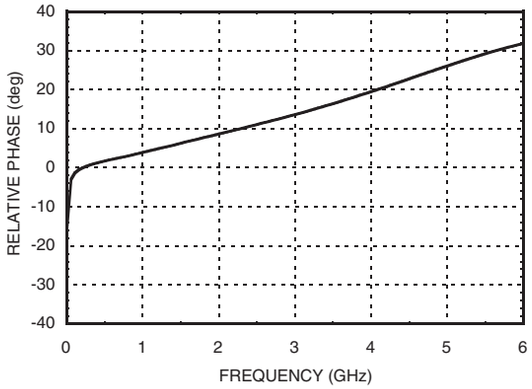
Return Loss RF1, RF2



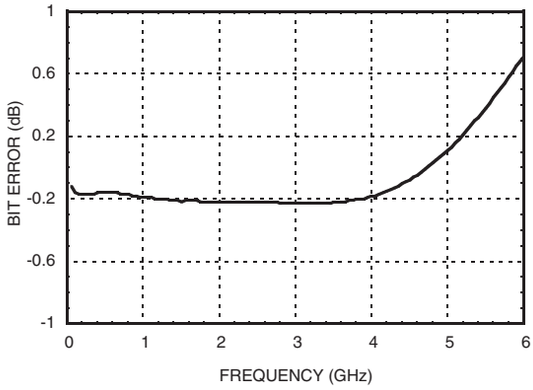
Normalized Attenuation



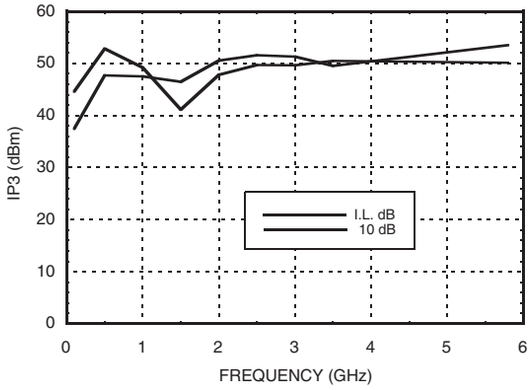
Relative Phase vs. Frequency



Bit Error vs. Frequency



Input IP3 vs. Frequency



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Bias Voltage & Current

Vdd = +5.0 Vdc ± 10%	
Vdd (VDC)	Idd (Typ.) (mA)
+4.5	1.3
+5.0	1.5
+5.5	1.7

Truth Table

Control Voltage Input	Attenuation State RF1 - RF2
V1 10 dB	
High	Reference I.L.
Low	10 dB

Control Voltage

State	Bias Condition
Low	0 to +0.8V @ -5 uA Typ.
High	+2.0 to + 5.0 Vdc @ 40 uA Typ.
Note: Vdd = +5V	

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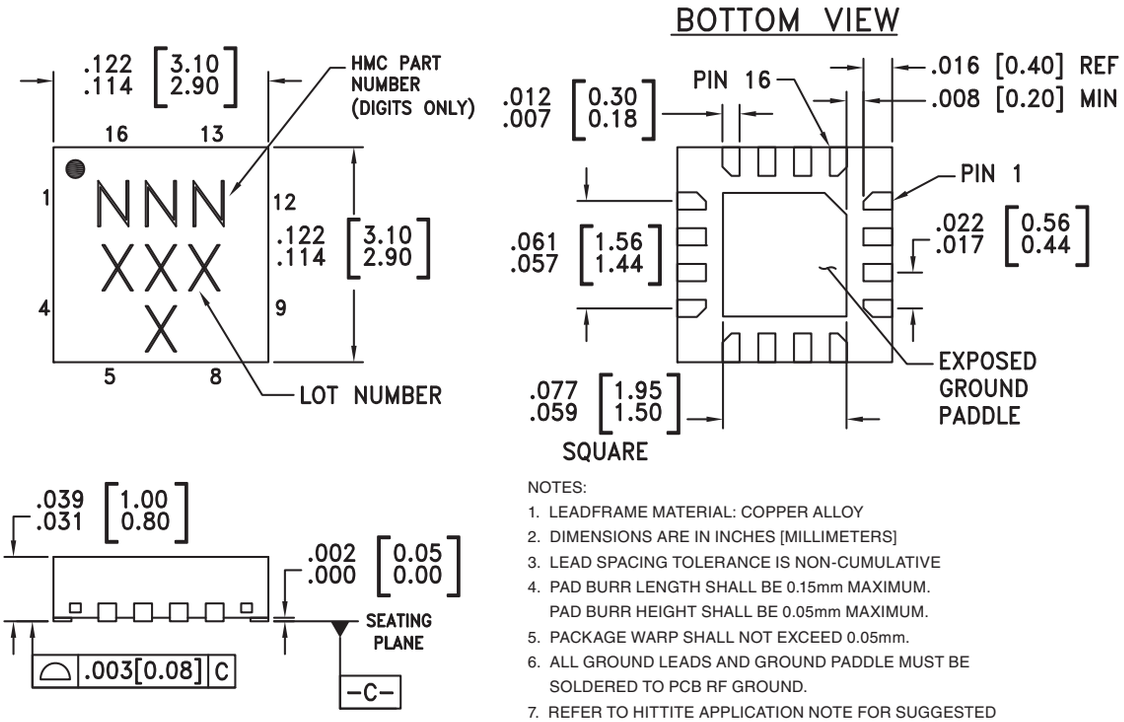
Absolute Maximum Ratings

RF Input Power (DC - 5 GHz)	+27 dBm (T = +85 °C)
Control Voltage Range (V1)	-1V to Vdd +1V
Bias Voltage (Vdd)	+7.0 Vdc
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 14.7 mW/°C above 85 °C)	0.96 W
Thermal Resistance	68 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1B

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

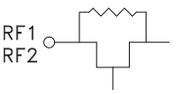
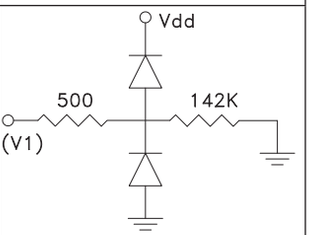
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

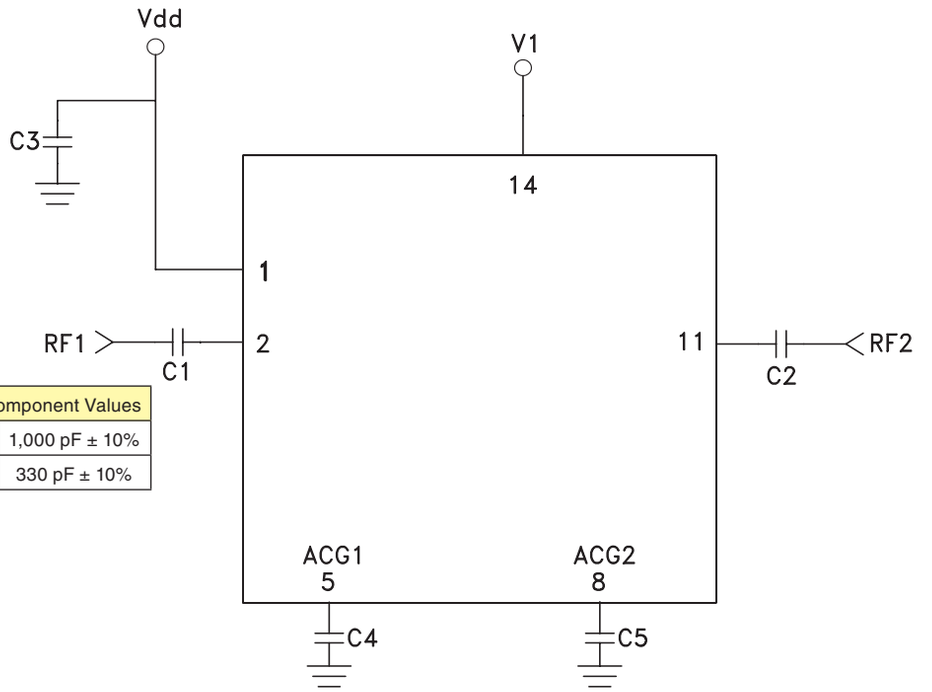
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC541LP3	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	541 XXXX
HMC541LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	541 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

Pin Descriptions

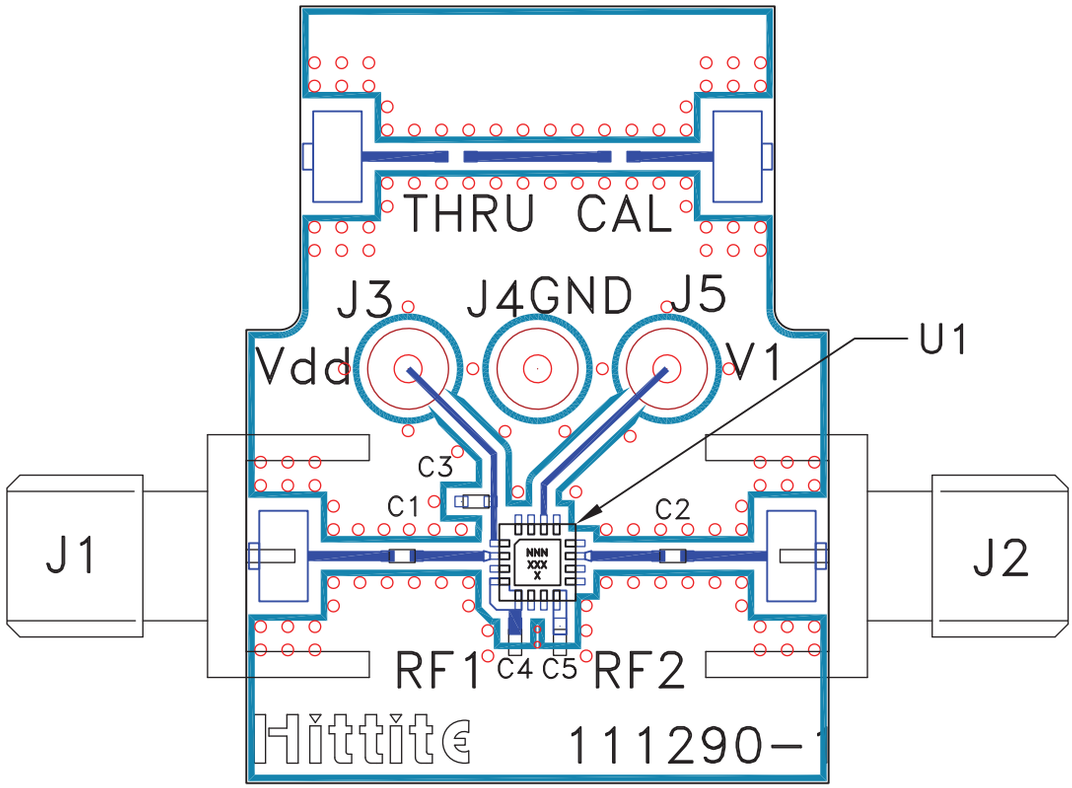
Pin Number	Function	Description	Interface Schematic
1	Vdd	Supply Voltage.	
2, 11	RF1, RF2	This pin is DC coupled and matched to 50 Ohm. Blocking capacitors are required. Select value based on lowest frequency of operation.	
3, 4, 6, 7, 9, 10, 12, 13, 15, 16	N/C	These pins should be connected to PCB RF ground to maximize performance.	
5, 8	ACG1, ACG2	External capacitor to ground is required. Select value for lowest frequency of operation. Place capacitor as close to pins as possible.	
14	V1	See truth table and control voltage table.	
	GND	Package bottom has an exposed metal paddle that must be connected to RF Ground.	

Application Circuit



Recommended Component Values	
C1 - C3	1,000 pF ± 10%
C4, C5	330 pF ± 10%

Evaluation PCB



List of Material for Evaluation PCB 111317 [1]

Item	Description
J1 - J2	PCB Mount SMA Connector
J3 - J5	DC Connector
C1 - C3	1000 pF Capacitor, 0402 Pkg.
C4 - C5	330 pF Capacitor, 0402 Pkg.
U1	HMC541LP3 / HMC541LP3E Digital Attenuator
PCB [2]	111290 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.