v01.1008

HMC718LP4 / 718LP4E

GaAs PHEMT MMIC HIGH IP3 LOW NOISE AMPLIFIER, 0.6 - 1.4 GHz

Typical Applications

The HMC718LP4(E) is ideal for:

- Cellular/3G and LTE/WiMAX/4G
- BTS & Infrastructure
- Repeaters and Femtocells
- Access Points
- Test Equipment

Features

Noise Figure: 0.9 dB

Gain: 32 dB

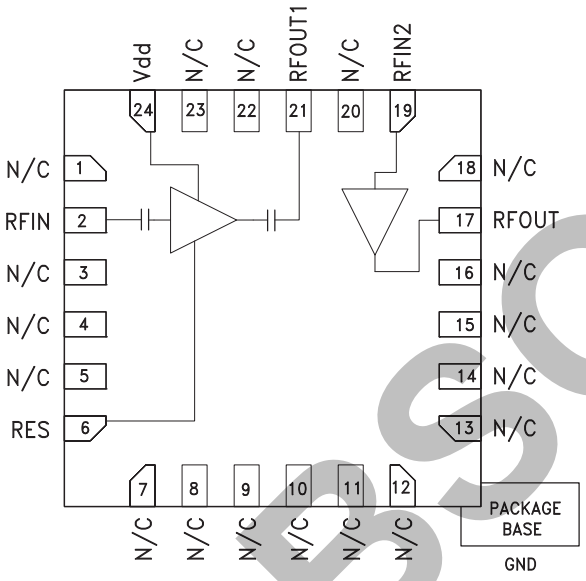
Output IP3: +40 dBm

Single Supply: +3V to +5V

50 Ohm Matched Input/Output

24 Lead 4x4 mm SMT Package: 16 mm^2

Functional Diagram



General Description

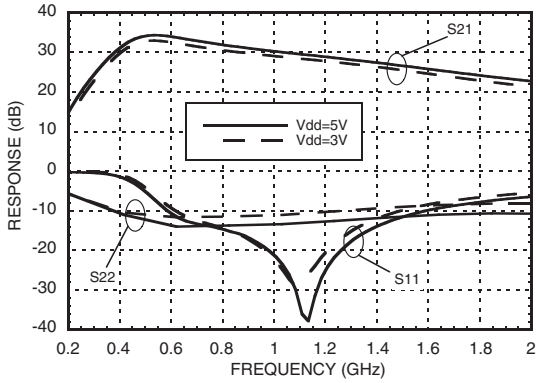
The HMC718LP4(E) is a GaAs PHEMT MMIC Low Noise Amplifier that is ideal for Cellular/3G and LTE/WiMAX/4G basestation front-end receivers operating between 600 and 1400 MHz. The amplifier has been optimized to provide 0.9 dB noise figure, 32 dB gain and +40 dBm output IP3 from a single supply of +5V. Input and output return losses are excellent and the LNA requires minimal external matching and bias decoupling components. The HMC718LP4(E) shares the same package and pinout with the HMC719LP3(E) 1.3 - 2.9 GHz LNA. The HMC718LP4(E) can be biased with +3V to +5V and features an externally adjustable supply current which allows the designer to tailor the linearity performance of the LNA for each application.

Electrical Specifications, T_A = +25°C, Rbias = 3.92k Ohms*

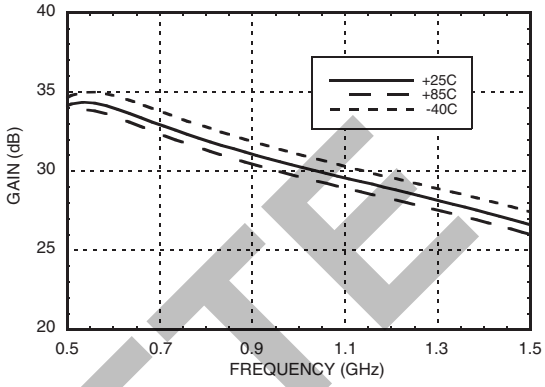
Parameter	Vdd = +3V						Vdd = +5V						Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	0.6 - 1.0			1.0 - 1.4			0.6 - 1.0			1.0 - 1.4			GHz
Gain	26	30.5		25	27.5		27	32		25	29		dB
Gain Variation Over Temperature		0.01			0.01			0.01			0.01		dB/ °C
Noise Figure		0.95			0.75			0.95			0.8		dB
Input Return Loss		15			20			15.5			23		dB
Output Return Loss		13			10			15.5			13		dB
Output Power for 1 dB Compression (P1dB)	13	15.5		13	15.7		19	21.5		19	21.5		dBm
Saturated Output Power (Psat)		19			19			23.5			23.3		dBm
Output Third Order Intercept (IP3)		35			34.5			40.5			40		dBm
Supply Current (Idd)		187	200		187	200		254	281		254	281	mA

* Rbias resistor sets current, see application circuit herein

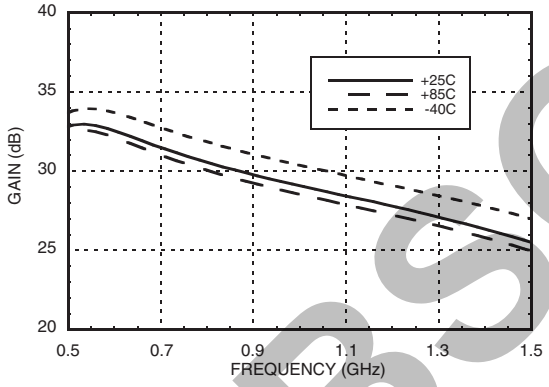
Broadband Gain & Return Loss [1] [2]



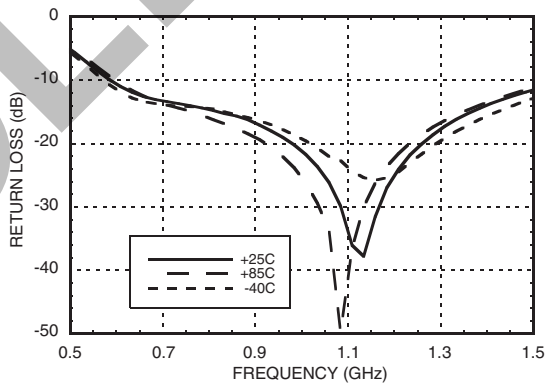
Gain vs. Temperature [1]



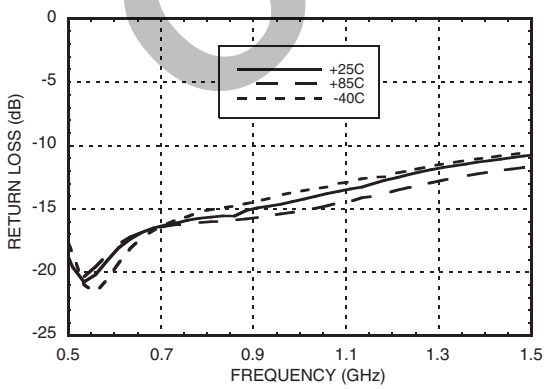
Gain vs. Temperature [2]



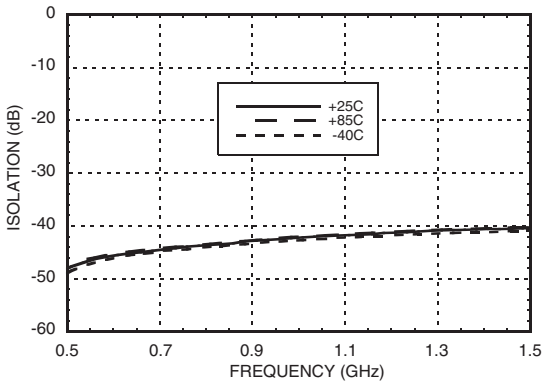
Input Return Loss vs. Temperature [1]



Output Return Loss vs. Temperature [1]

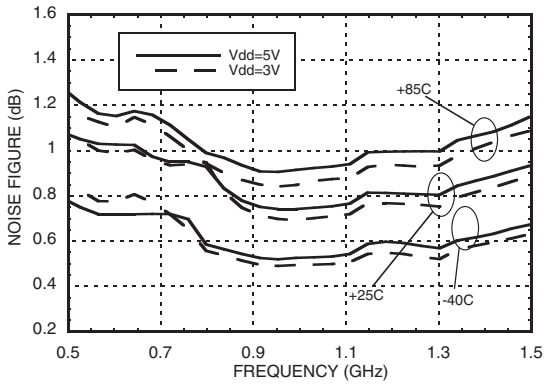


Reverse Isolation vs. Temperature [1]

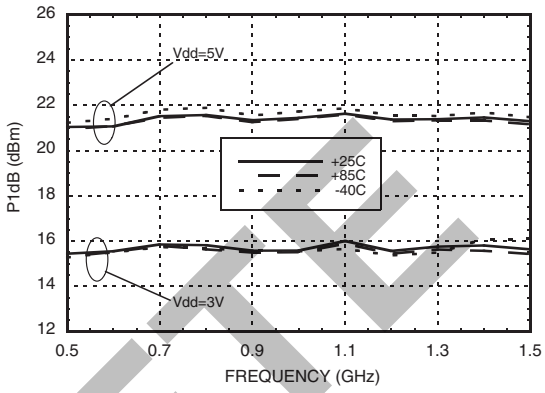


[1] Vdd = 5V, Rbias = 3.92K [2] Vdd = 3V, Rbias = 3.92K

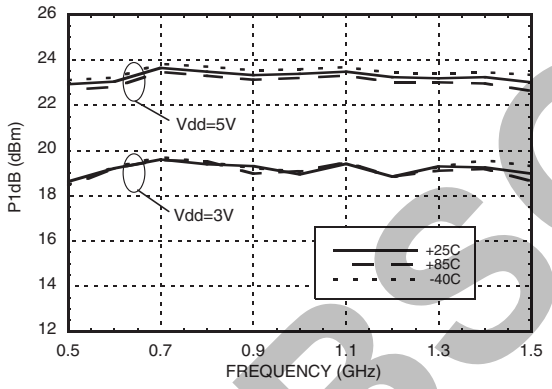
Noise Figure vs. Temperature [1] [2]



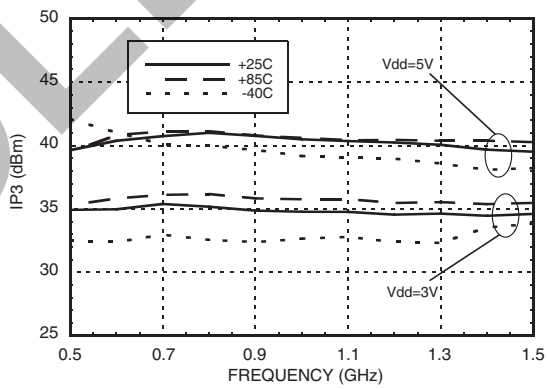
P1dB vs. Temperature [1] [2]



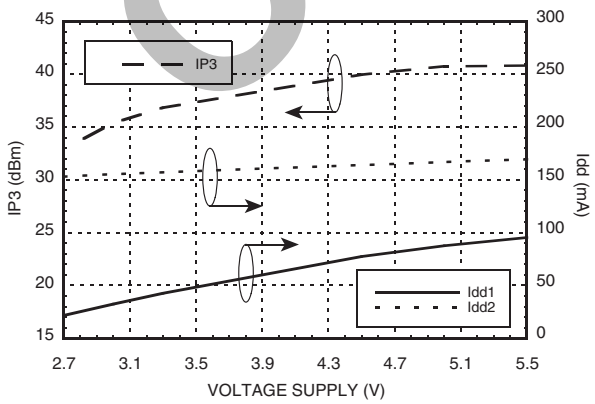
Psat vs. Temperature [1] [2]



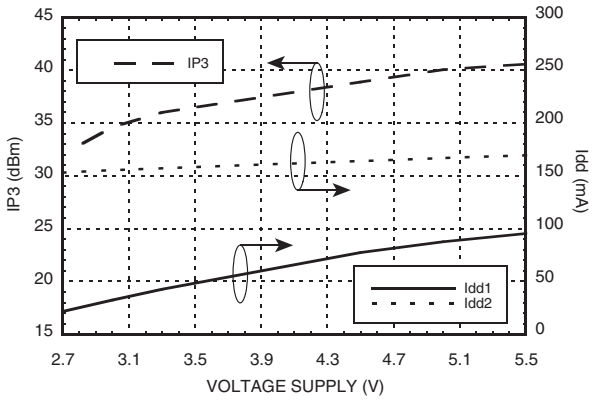
Output IP3 vs. Temperature [1] [2]



Output IP3 and Idd vs. Supply Voltage @ 700 MHz [3]

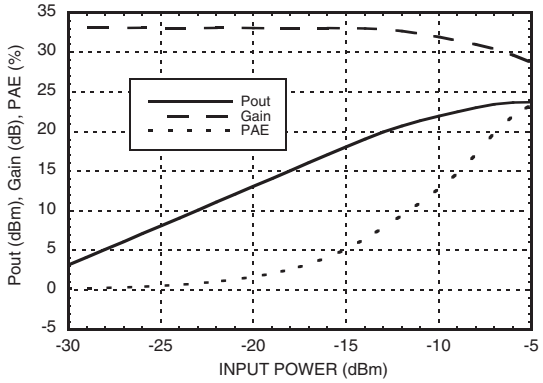


Output IP3 and Idd vs. Supply Voltage @ 1300 MHz [3]

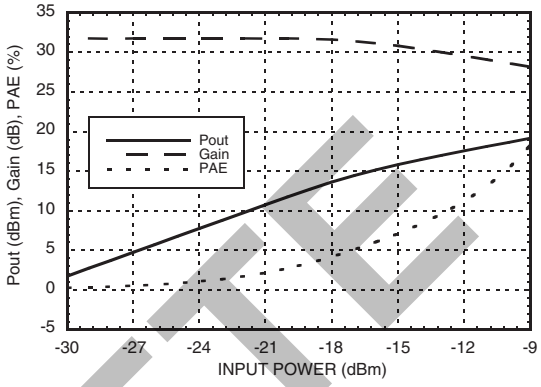


[1] Vdd = 5V, Rbias = 3.92K [2] Vdd = 3V, Rbias = 3.92K [3] Rbias = 3.92K

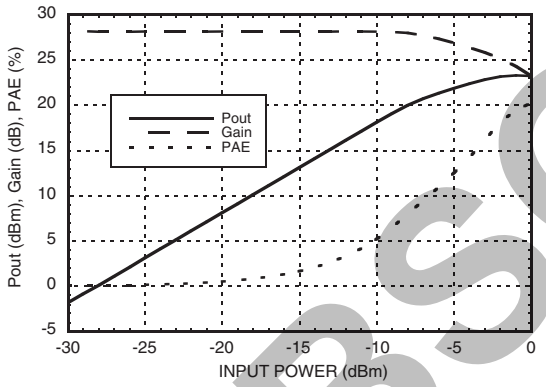
Power Compression @ 700 MHz [1]



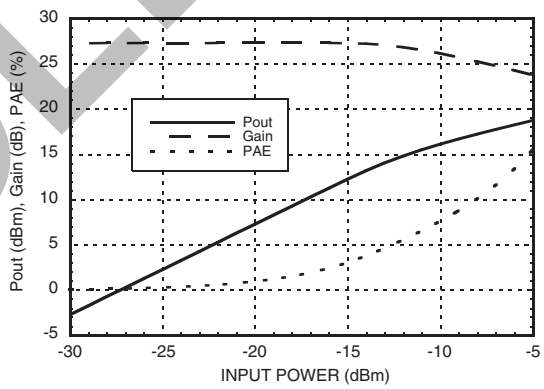
Power Compression @ 700 MHz [2]



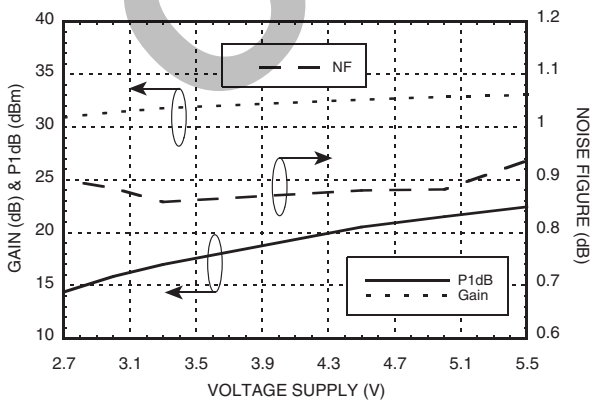
Power Compression @ 1300 MHz [1]



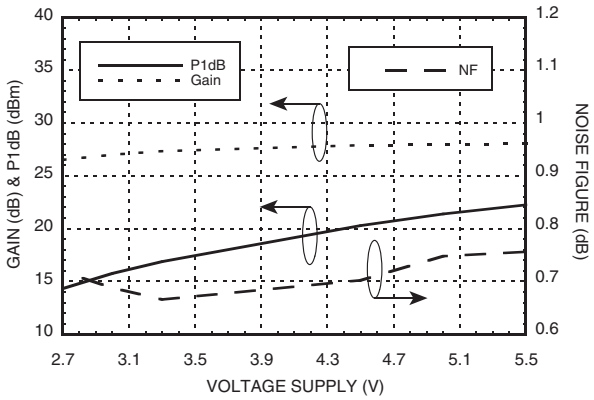
Power Compression @ 1300 MHz [2]



Gain, Power & Noise Figure vs. Supply Voltage @ 700 MHz [3]

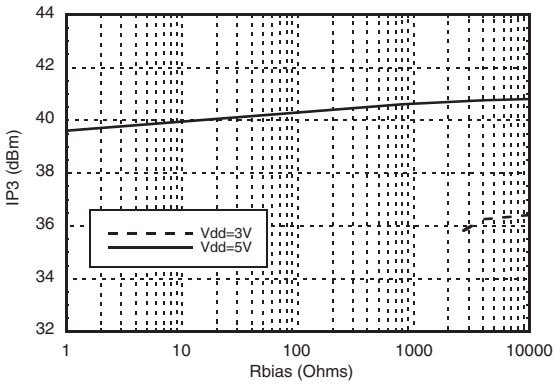


Gain, Power & Noise Figure vs. Supply Voltage @ 1300 MHz [3]

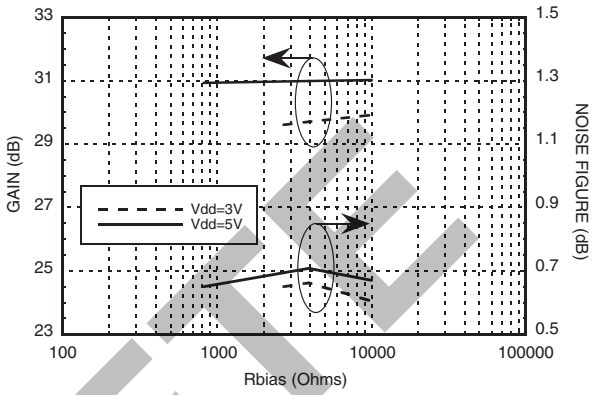


[1] Vdd = 5V, Rbias = 3.92K [2] Vdd = 3V, Rbias = 3.92K [3] Rbias = 3.92K

Output IP3 vs. Rbias @ 900 MHz



Gain, Noise Figure & Rbias @ 900 MHz



Absolute Bias Resistor Range & Recommended Bias Resistor Values for Idd

Vdd (V)	Rbias Ω			Idd1 (mA)	Idd2 (mA)
	Min	Max	Recommended		
3V	1K [1]	Open Circuit	2.7k	27	155
			3.9k	32	155
			10k	41	155
5V	0	Open Circuit	820	67	166
			3.92k	88	166
			10k	92	166

[1] Operation with Vdd= 3V and Rbias < 1K Ohm may result in the part becoming conditionally stable which is not recommended.

Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	5.5 V
RF Input Power (RFIN) (Vdd = +5 Vdc)	-5 dBm
Channel Temperature	175 °C
Continuous Pdiss (T= 85 °C) (derate 20 mW/°C above 85 °C)	1.8 W
Thermal Resistance (channel to ground paddle)	50 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

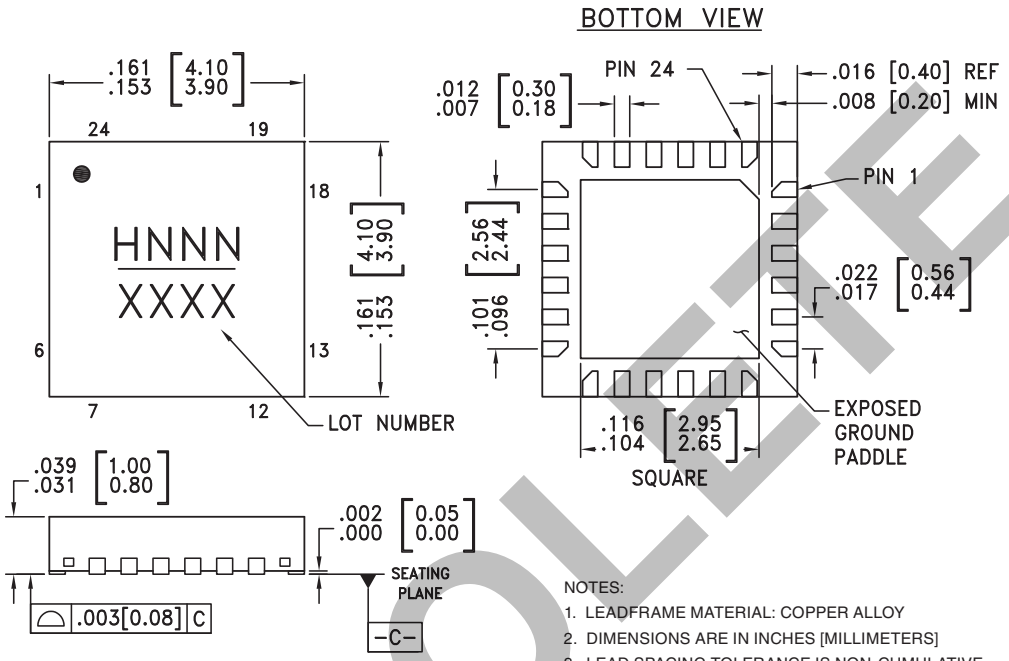
ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Typical Supply Current vs. Vdd (Rbias = 3.92k)

Vdd (V)	Idd1 (mA)	Idd2 (mA)
2.7	22	153
3.0	32	155
3.3	43	157
4.5	77	164
5.0	88	166
5.5	95	169

Note: Amplifier will operate over full voltage ranges shown above.

Outline Drawing



NOTES:

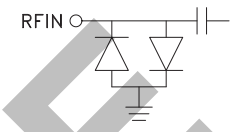
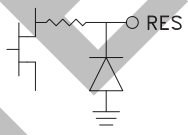
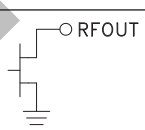
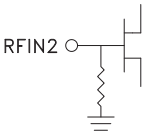
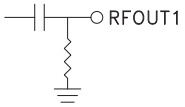
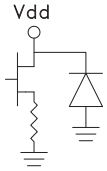
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

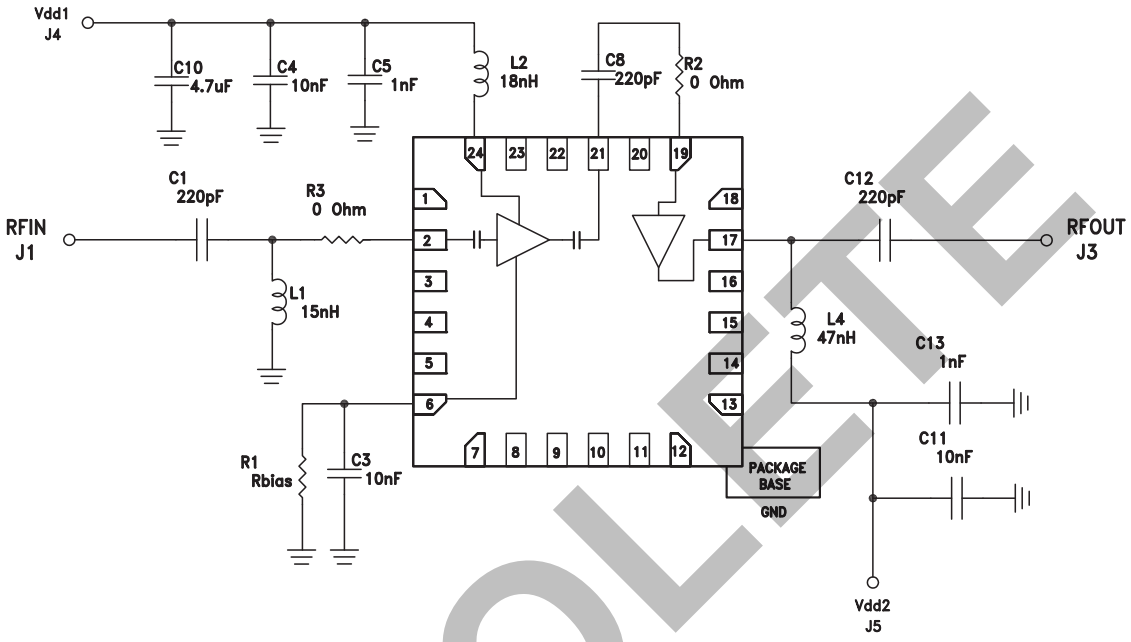
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC718LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H718 XXXX
HMC718LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H718 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

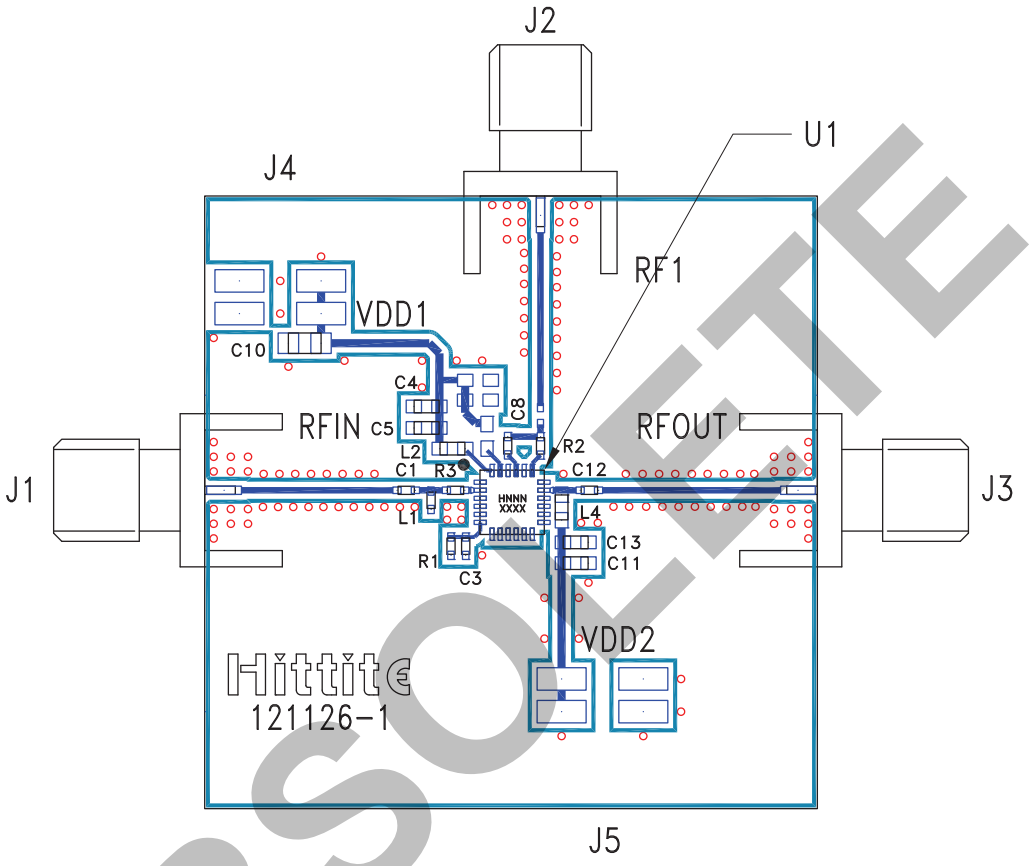
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 3 - 5, 7 - 16, 18, 20, 22, 23	N/C	No connection necessary. These pins may be connected to RF/DC ground without affecting performance.	
2	RFIN	This pin is DC coupled and matched to 50 Ohms.	
6	RES	This pin is used to set the DC current of the amplifier by selection of external bias resistor. See application circuit.	
17	RFOUT	RF Output and DC BIAS for the second amplifier. See Application Circuit for off-chip components.	
19	RFIN2	This pin is DC coupled. An off-chip DC blocking capacitor is required.	
21	RFOUT1	This pin is matched to 50 Ohms.	
24	Vdd	Power Supply Voltage for the first amplifier. Choke inductor and bypass capacitors are required. See application circuit.	

Application Circuit



Evaluation PCB



List of Materials for Evaluation PCB 121128 [1]

Item	Description
J1 - J3	PCB Mount SMA Connector
J4 - J5	2mm Vertical Molex Connector
C1, C8, C12	220 pF Capacitor, 0402 Pkg.
C3	10 nF Capacitor, 0402 Pkg.
C4, C11	10 nF Capacitor, 0603 Pkg.
C5, C13	1000 pF Capacitor, 0603 Pkg.
C10	4.7 uF Capacitor, 0805 Pkg.
L1	15 nH Inductor, 0402 Pkg.
L2	18 nH Inductor, 0603 Pkg.
L4	47 nH Inductor, 0603 Pkg.
R1	Rbias Resistor, 0402 Pkg.
R2, R3	0 Ohm Resistor, 0402 Pkg.
U1	HMC718LP4(E) Amplifier
PCB [2]	121126 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR

The circuit board used in this application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.