HMC8200LP5ME

v01.0216

INTERMEDIATE FREQUENCY TRANSMITTER 800 MHz - 4000 MHz

Features

High linearity: Support modulations to 1024 QAM

Tx IF range: 200 MHz - 700 MHz

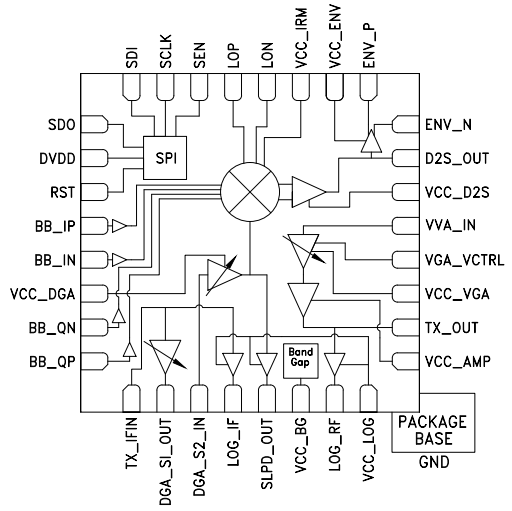
Tx RF range: 800 MHz - 4000 MHz

Tx power control range: 25 dB

SPI controlled interface

32 - lead 5 mm × 5 mm LFCSP package

Functional Diagram



Typical Applications

- Point to point communications
- Satellite communications
- Wireless microwave backhaul systems

General Description

The HMC8200LP5ME is a highly integrated Intermediate Frequency Transmitter chip that converts the industry standard 300 MHz to 400 MHz intermediate frequency input signal to an 800 MHz to 4000 MHz single ended radio frequency signal at its output. The Intermediate Frequency Transmitter chip is housed in a compact 5 mm x 5 mm LFCSP package and supports complex modulations up to 1024 QAM. The HMC8200LP5ME simultaneously reduces the design complexity of traditional microwave radios while realizing significant size and cost improvements. With intermediate frequency input power ranges from –31 dBm to +4 dBm, the HMC8200LP5ME provides 35 dB of digital gain control in 1 dB steps while an analog voltage gain amplifier (VGA) continuously controls the transmitter output power from -20 dBm to +5 dBm. The device also features three integrated power detectors. The first detector (LOG_IF) can be utilized to monitor the intermediate frequency input power. The second detector (SLPD_OUT) is a square law power detector that monitors the power going into the mixer. The third power detector (LOG_RF) is used to monitor the output power, which can be used for fine output power adjustment.

Table 1. Electrical Specifications, TA = +25° C, See Test Conditions.

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
OPERATING CONDITIONS										
RF Frequency Range	800		1800	1800		2800	2800		4000	MHz
LO Frequency Range	300		2300	1300		3300	2300		4500	MHz
IF Frequency Range	200		700	200		700	200		700	MHz
IF INPUT INTERFACE										
Input Impedance		50			50			50		Ω
Return Loss		20			20			20		dB
LOG IF Power Detector 1 dB Dynamic Range		50			50			50		dB
LOG IF Power Detector Range	-30		+10	-30		+10	-30		+10	dBm
LOG IF Power Detector Slope		37			37			37		mV / dB
Square Log Power Detector Range		17			17			17		dB
RF OUTPUT INTERFACE										
Input Impedance		50			50			50		Ω
Return Loss	7	13		12	15		15	23		dB
LOG Power Detector 1 dB Dynamic Range		50			50			50		dB
LOG Power Detector Range	-25		+10	-25		+10	-25		+10	dBm
LOG Power Detector Slope		37			37			37		mV / dB

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

Table 2. Electrical Specifications, TA = +25° C, See Test Conditions.

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
OPERATING CONDITIONS										
RF Frequency Range	800		1800	1800		2800	2800		4000	MHz
LO Frequency Range	300		2300	1300		3300	2300		4500	MHz
IF Frequency Range	200		700	200		700	200		700	MHz
LO INPUT INTERFACE										
Input Impedance		50			50			50		Ω
Return Loss	7	12		8	15		12	17		dB
DYNAMIC PERFORMANCE										
Conversion Gain	30	34		28	32		22	30		dB
Digital VGA Dynamic Range	30	35		30	35		30	35		dB
Analog VGA Dynamic Range	23	27		22	26		20	25		dB
Sideband Rejection[1]	28	32		28	32		22	30		dBc
Noise Figure		6			5.5			5.5		dB
Output Third-Order Intercept (OIP3)	28	31		25	28		20	26		dBm
Output 1 dB Compression Point (OP1dB)	11	15		10	15		7	14		dBm
LO to RF Rejection[1]		30			34			32		dBc
IF to RF Rejection	56	63		55	58		50	55		dBc

[1] Measurement was taken uncalibrated

Table 3. Test Conditions[1]

Temperature	+25°C
IF Frequency	350 MHz
LO Input Signal Level	0 dBm
RF Input Signal Level	-31 dBm per tone
DGA Setting (dec)	35 (Max Gain)
VGA Setting	+3.3V (Max Gain)
Sidband Select	LSB

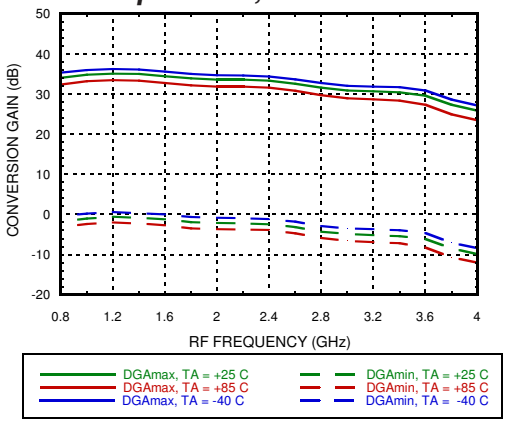
[1] Unless otherwise stated on plots, the above test conditions were used.

Table 4. Recommended Operation Conditions

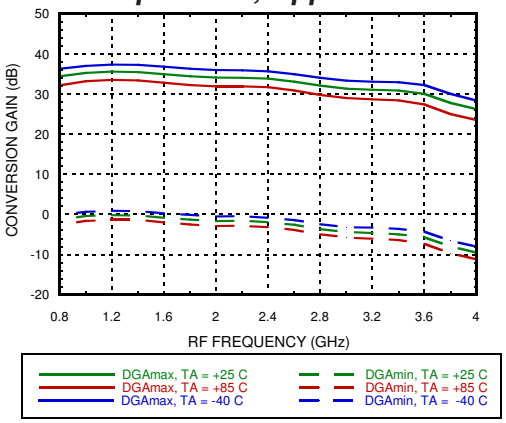
Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
POWER SUPPLY										
Supply Voltage										
V_{CCx}		3.3			3.3			3.3		V
$V_{CC_}$VGA		3.3			3.3			3.3		V
Supply Current										
V_{CCx}		540			540			540		mA
$V_{CC_}$VGA		11			11			11		µA

[1] Vcc-VGA can be adjusted from 3.3V(Max Gain) to 0V (Min Gain) to control the RF VGA.

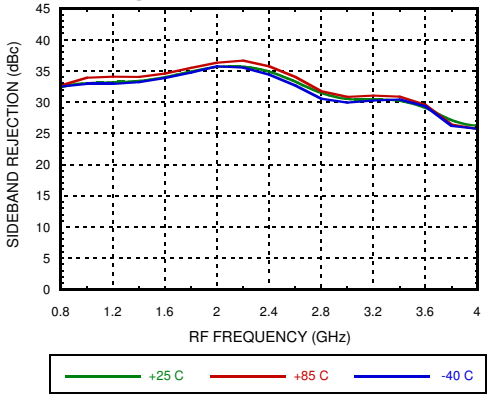
Conversion Gain vs. RF Frequency over Temperature, Lower Sideband



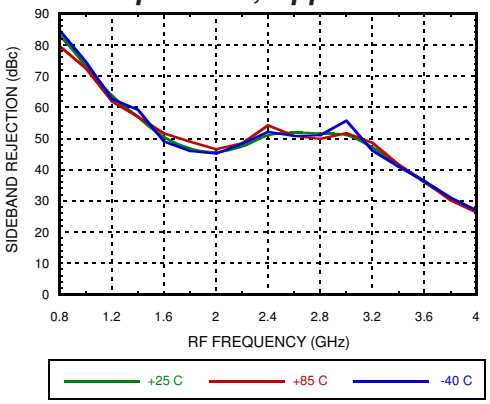
Conversion Gain vs. RF Frequency over Temperature, Upper Sideband



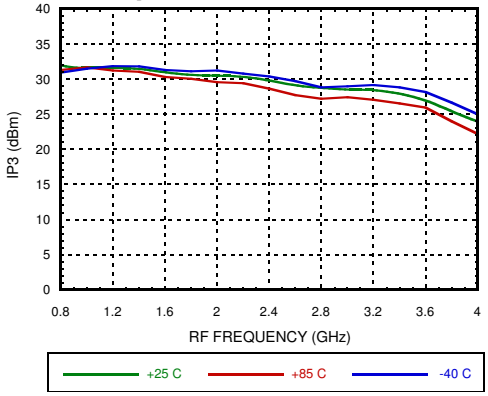
Sideband Rejection vs. RF Frequency over Temperature, Lower Sideband



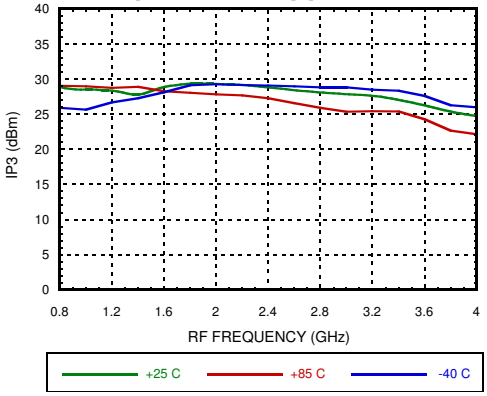
Sideband Rejection vs. RF Frequency over Temperature, Upper Sideband



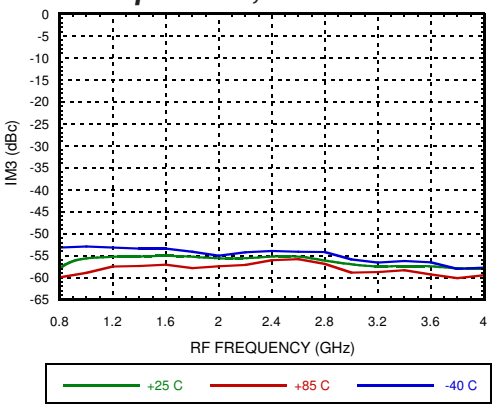
Output IP3 vs. RF Frequency over Temperature, Lower Sideband



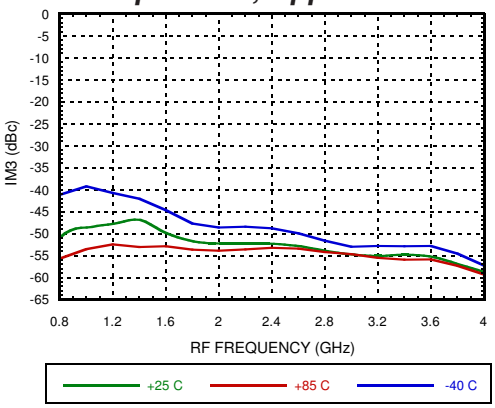
Output IP3 vs. RF Frequency over Temperature, Upper Sideband



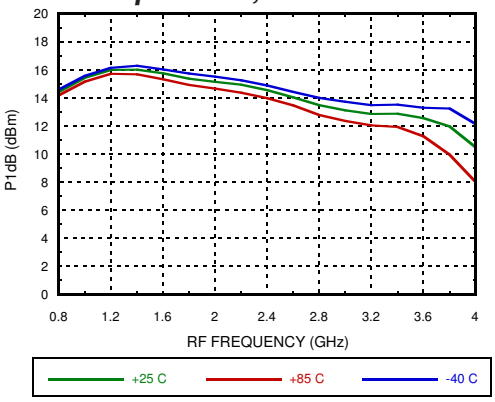
IM3 vs. RF Frequency over Temperature, Lower Sideband



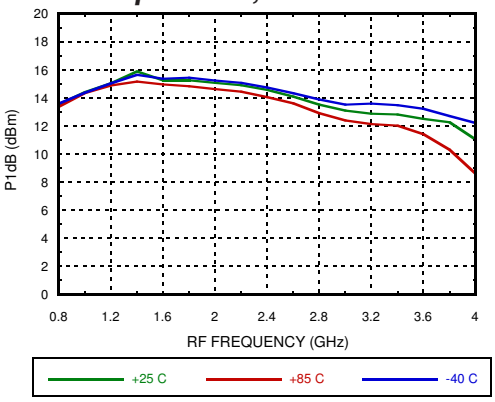
IM3 vs. RF Frequency over Temperature, Upper Sideband



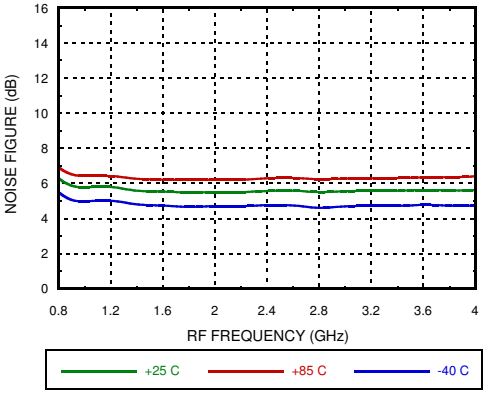
Output P1dB vs. RF Frequency over Temperature, Lower Sideband



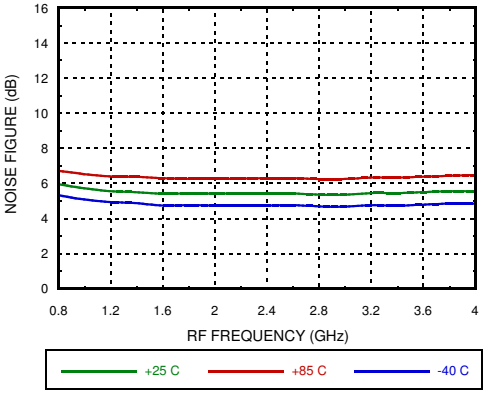
Output P1dB vs. RF Frequency over Temperature, Lower Sideband



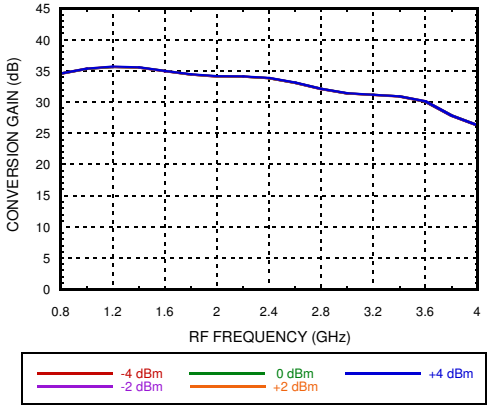
Noise Figure vs. RF Frequency over Temperature, Lower Sideband



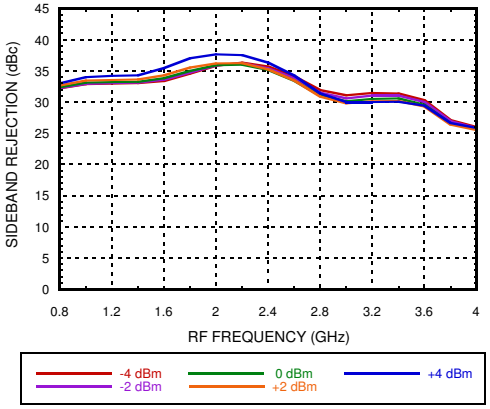
Noise Figure vs. RF Frequency over Temperature, Upper Sideband



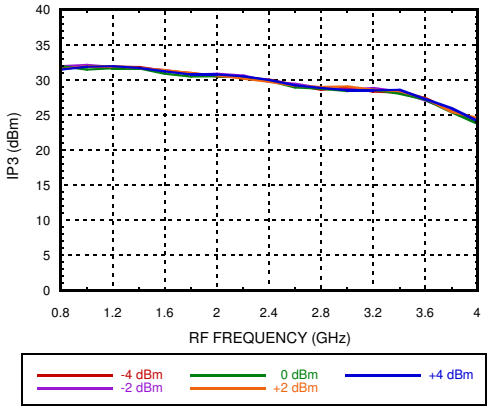
Conversion Gain vs. RF Frequency at Various LO Powers



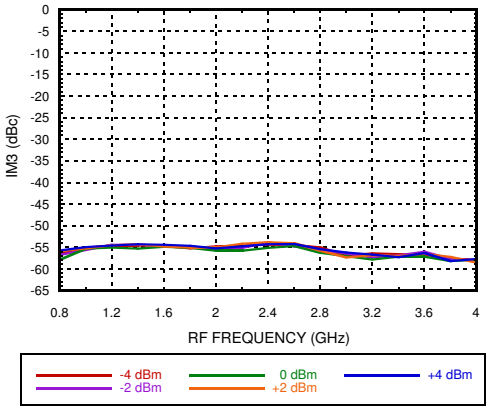
Sideband Rejection vs. RF Frequency at Various LO Powers



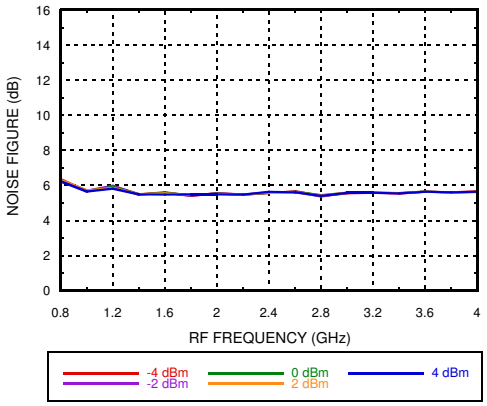
Output IP3 vs. RF Frequency at Various LO Powers



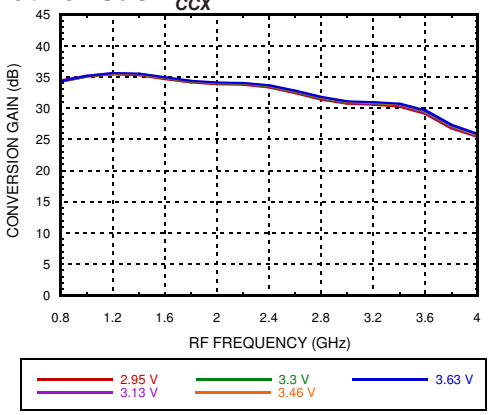
IM3 vs. RF Frequency at Various LO Powers



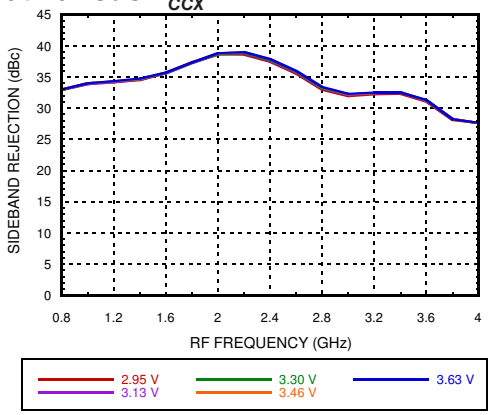
Noise Figure vs. RF Frequency at Various LO Powers



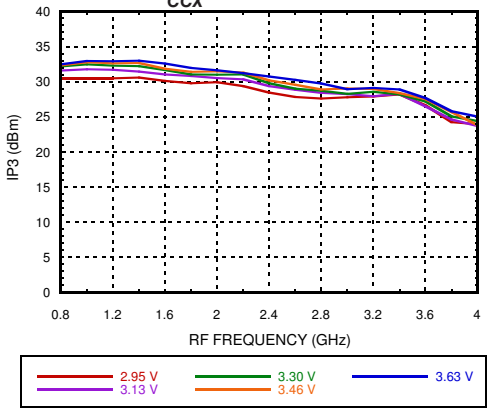
Conversion Gain vs. RF Frequency at Various V_{CCX}



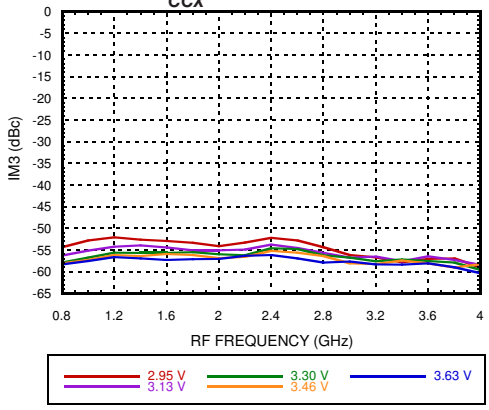
Sideband Rejection vs. RF Frequency at Various V_{CCX}



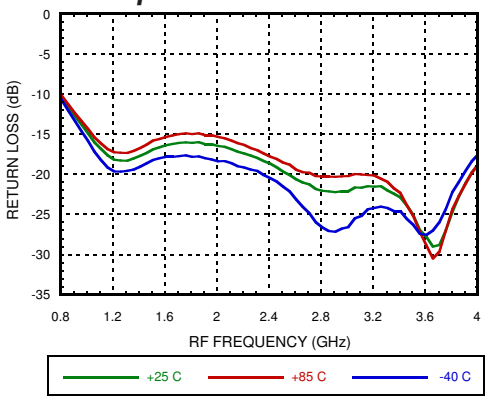
Output IP3 vs. RF Frequency at Various V_{CCX}



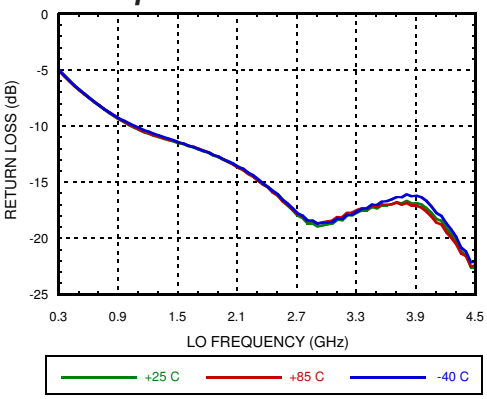
IM3 vs. RF Frequency at Various V_{CCX}



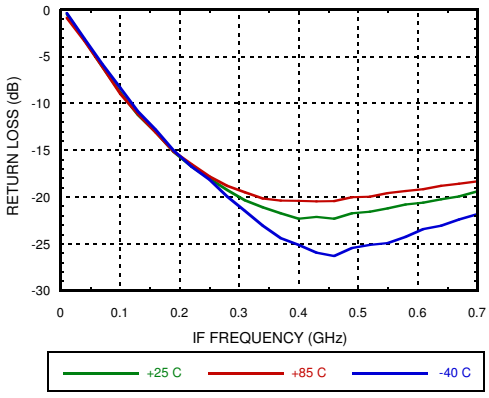
RF Return Loss vs. RF Frequency over Temperature



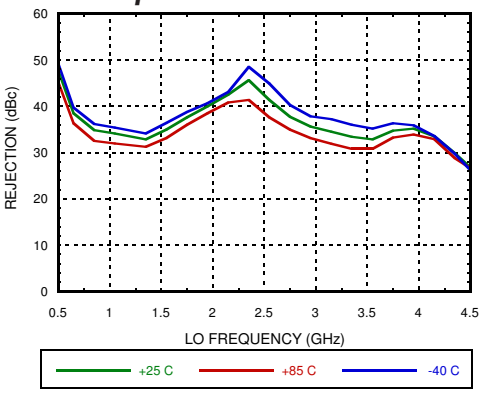
LO Return Loss vs. RF Frequency over Temperature



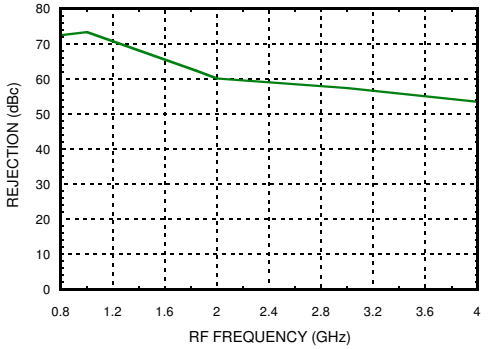
IF Return Loss vs. RF Frequency over Temperature



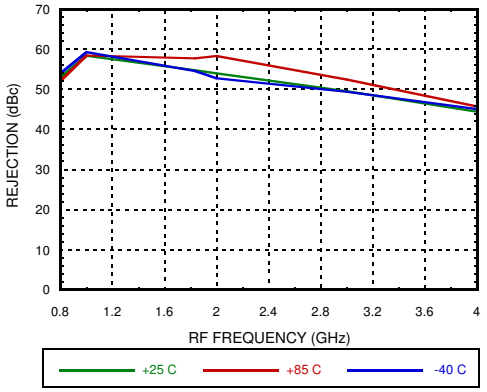
LO to RF Rejection vs. LO Frequency over Temperature[1]



IF to RF Rejection vs. RF Frequency at +25° C



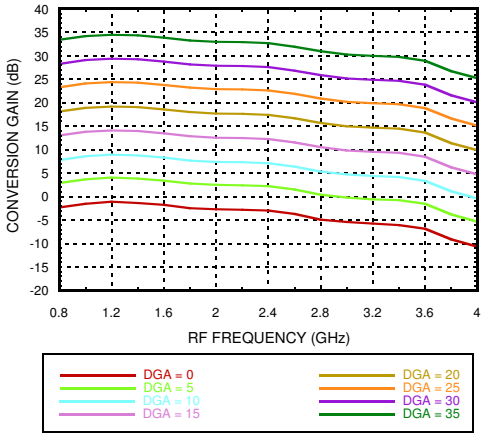
IF to RF Rejection vs. RF Frequency over Temperature[2]



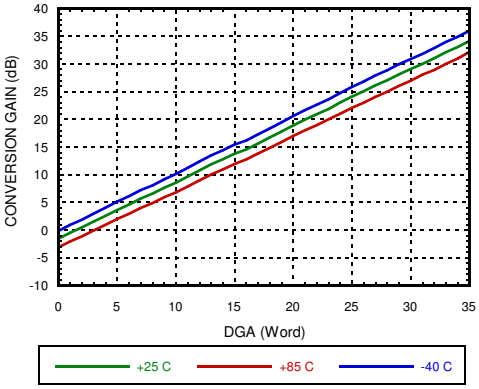
[1] Measurement uncalibrated for LO Leakage

[2] Measured at the input of the external low pass filter after C55. Please refer to Application Circuit.

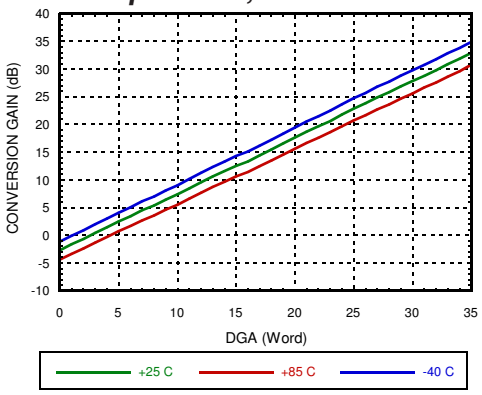
Conversion Gain vs. RF Frequency over DGA Word [1]



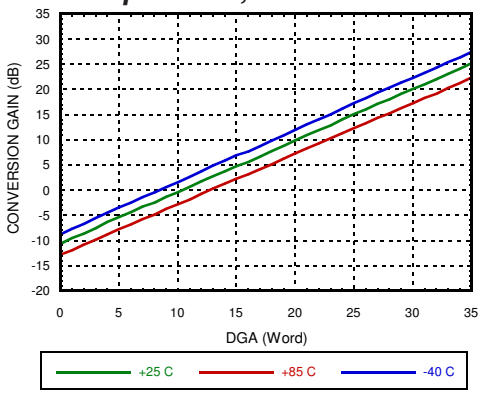
Conversion Gain vs. DGA Word over Temperature, RF = 1 GHz [1]



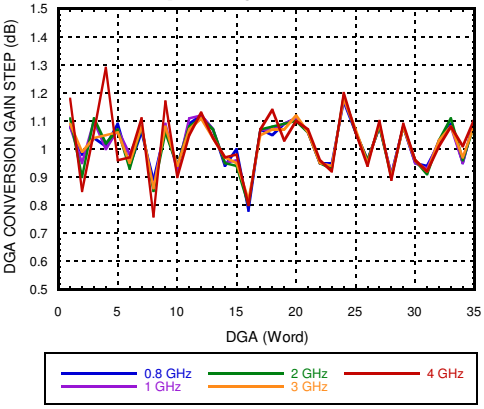
Conversion Gain vs. DGA Word over Temperature, RF = 2 GHz [1]



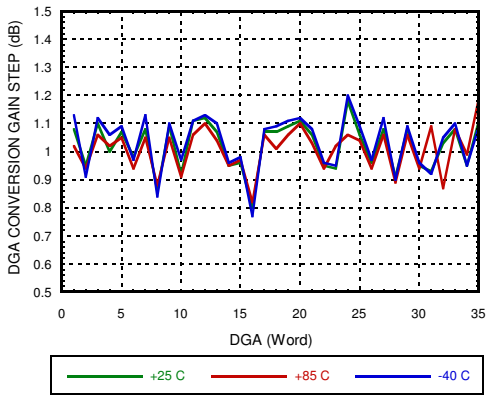
Conversion Gain vs. DGA Word over Temperature, RF = 4 GHz [1]



Conversion Gain Step vs. DGA word over RF Frequency

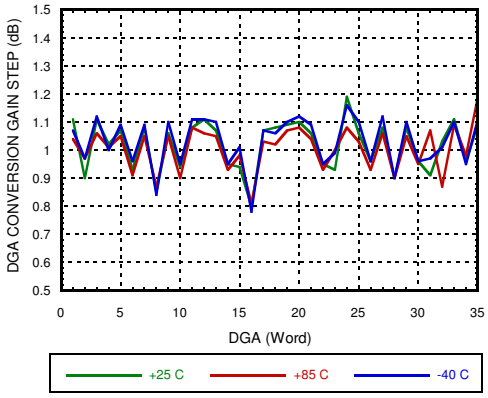


Conversion Gain Step vs. DGA word over Temperature, RF = 1 GHz

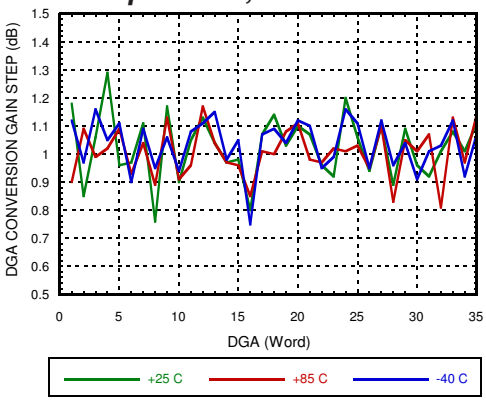


[1] Measurement conducted with $V_{cc\text{-}VGA}$ = +3.3V (Max Gain) on RF VGA.

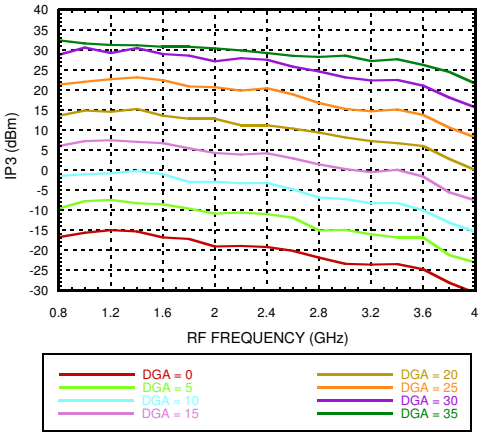
Conversion Gain Step vs. DGA word over Temperature, RF = 2 GHz



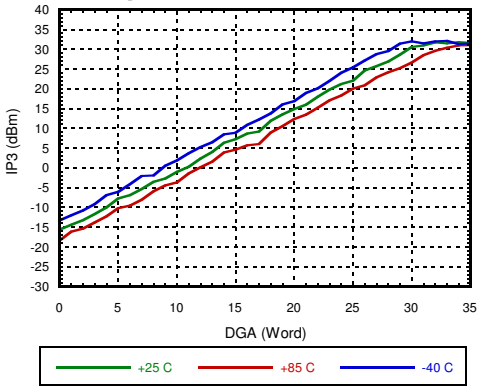
Conversion Gain Step vs. DGA word over Temperature, RF = 4 GHz



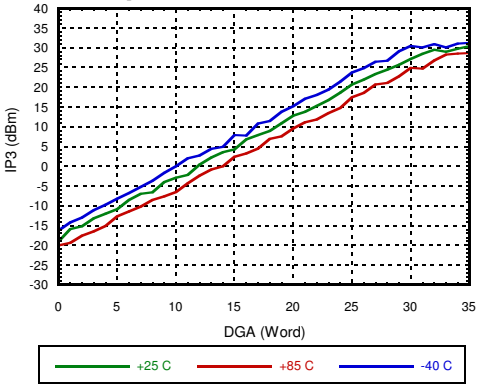
Output IP3 vs. RF Frequency over DGA Word [1]



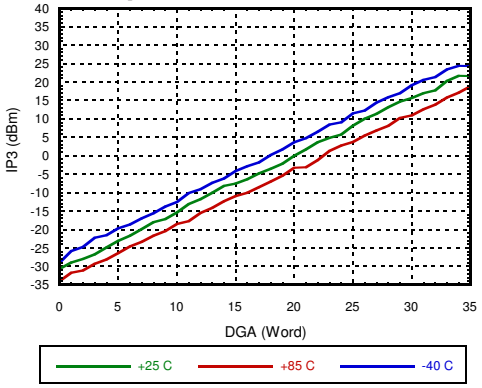
Output IP3 vs. DGA Word over Temperature, RF = 1 GHz [1]



Output IP3 vs. DGA Word over Temperature, RF = 2 GHz [1]

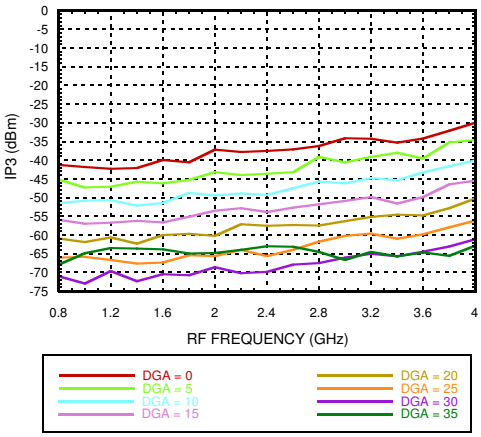


Output IP3 vs. DGA Word over Temperature, RF = 4 GHz [1]

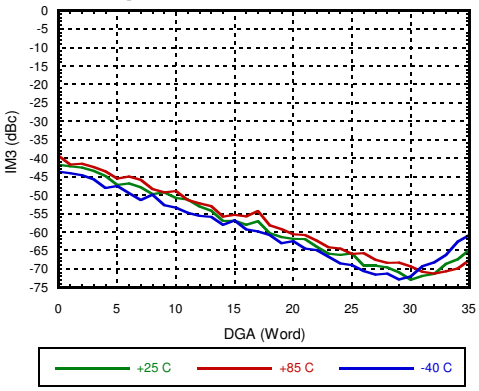


[1] Measurement conducted with $V_{cc\text{-}VGA}$ = +3.3V (Max Gain) on RF VGA.

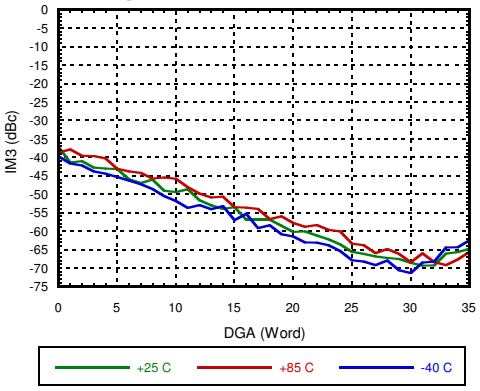
IM3 vs. RF Frequency over DGA Word [1]



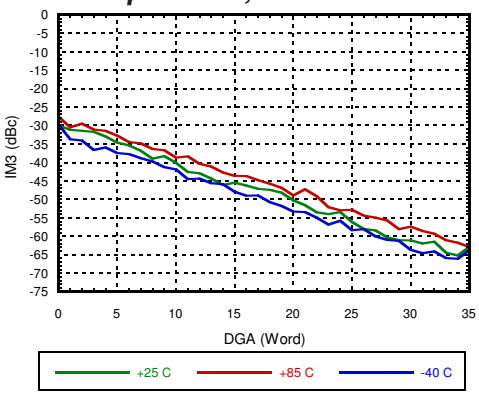
IM3 vs. DGA Word over Temperature, RF = 1 GHz [1]



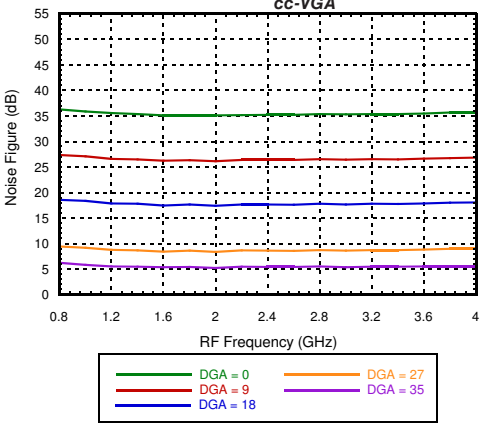
IM3 vs. DGA Word over Temperature, RF = 2 GHz [1]



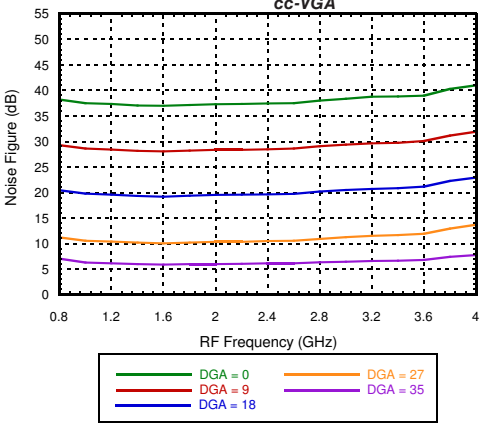
IM3 vs. DGA Word over Temperature, RF = 4 GHz [1]



Noise Figure vs. RF Frequency over DGA Word at V_{cc-VGA} = +3.3V

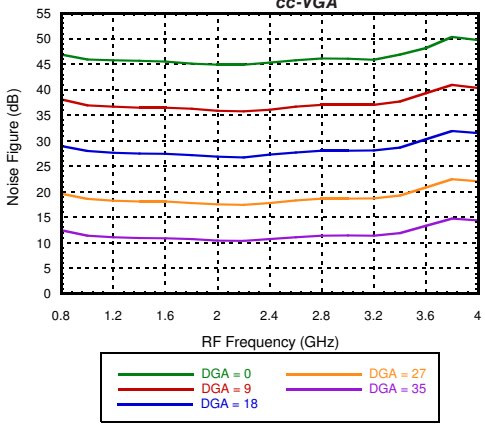


Noise Figure vs. RF Frequency over DGA Word at V_{cc-VGA} = +1.5V

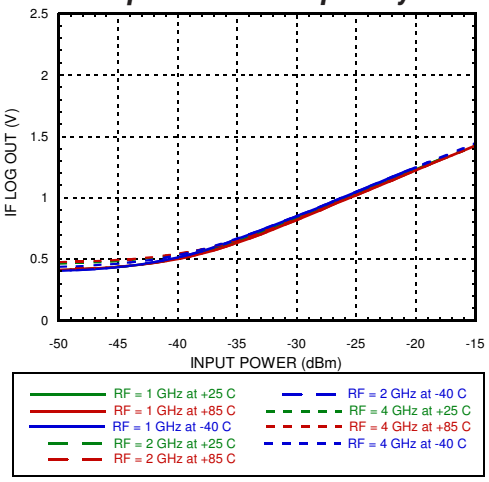


[1] Measurement conducted with V_{cc-VGA} = +3.3V (Max Gain) on RF VGA.

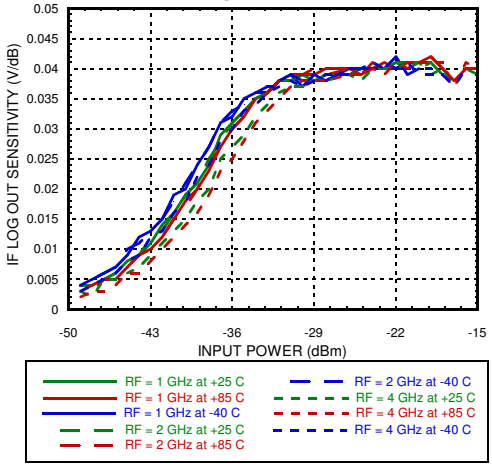
Noise Figure vs. RF Frequency over DGA Word at $V_{cc\text{-}VGA}$ = 0V



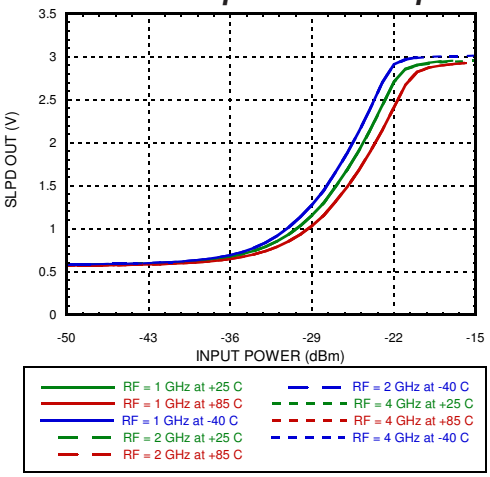
LOG IF Detector Output vs. Input Power over Temp. and RF Frequency



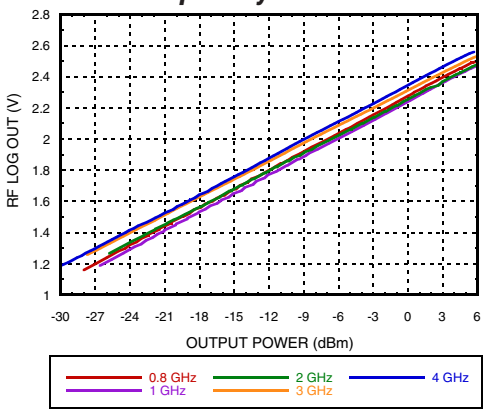
LOG IF Detector Sensitivity vs. Input Power over Temp. and RF Frequency



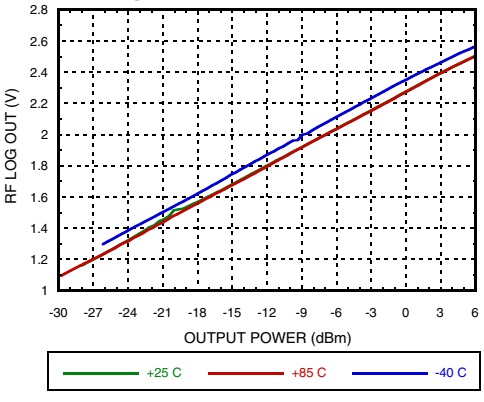
Square Law Detector Output vs. Input Power over Temp. and RF Frequency



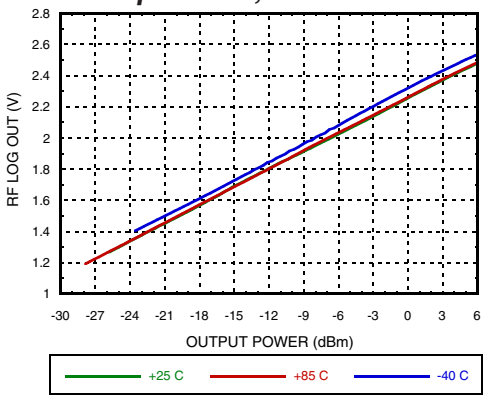
Log RF Detector vs. Output Power over RF Frequency



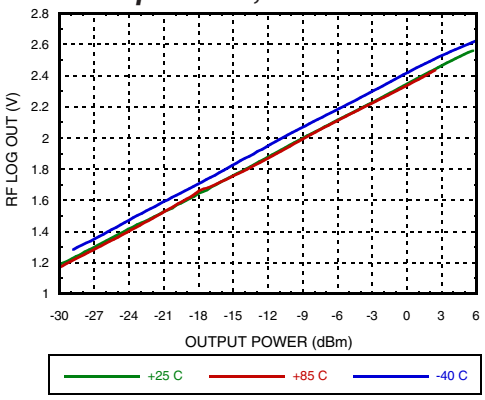
Log RF Detector vs. Output Power over Temperature, RF = 0.8 GHz



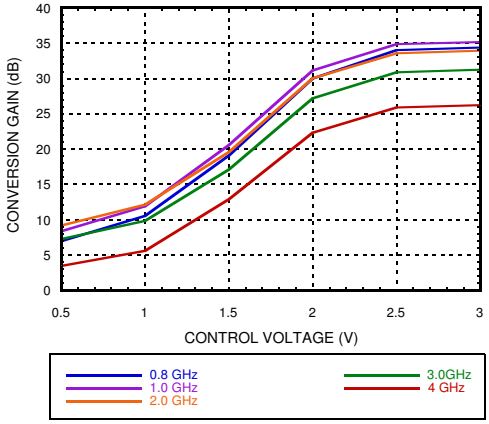
Log RF Detector vs. Output Power over Temperature, RF = 2 GHz



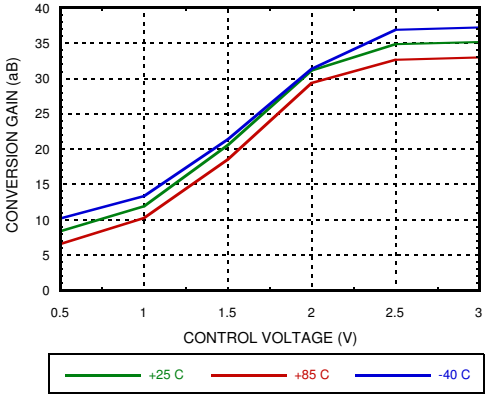
Log RF Detector vs. Output Power over Temperature, RF = 4 GHz



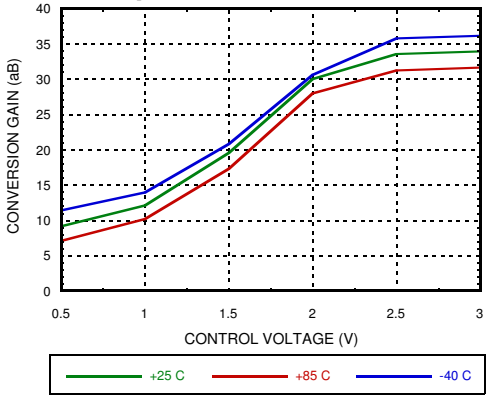
Conversion Gain vs. VGA Control Voltage over RF Frequency [1]



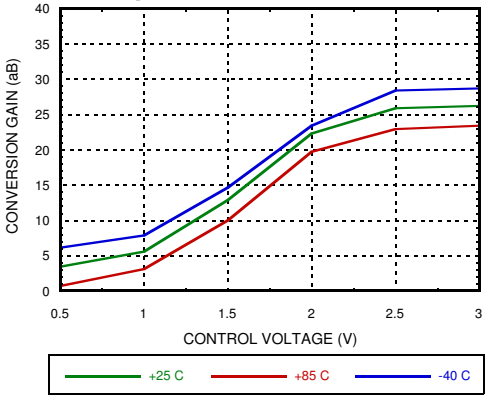
Conversion Gain vs. VGA Control Voltage over Temperature, RF = 1 GHz [1]



Conversion Gain vs. VGA Control Voltage over Temperature, RF = 2 GHz [1]



Conversion Gain vs. VGA Control Voltage over Temperature, RF = 4 GHz [1]



[1] Measurement conducted with DGA = 35 (Max Gain) on IF DGA.

Table 5. Absolute Maximum Ratings

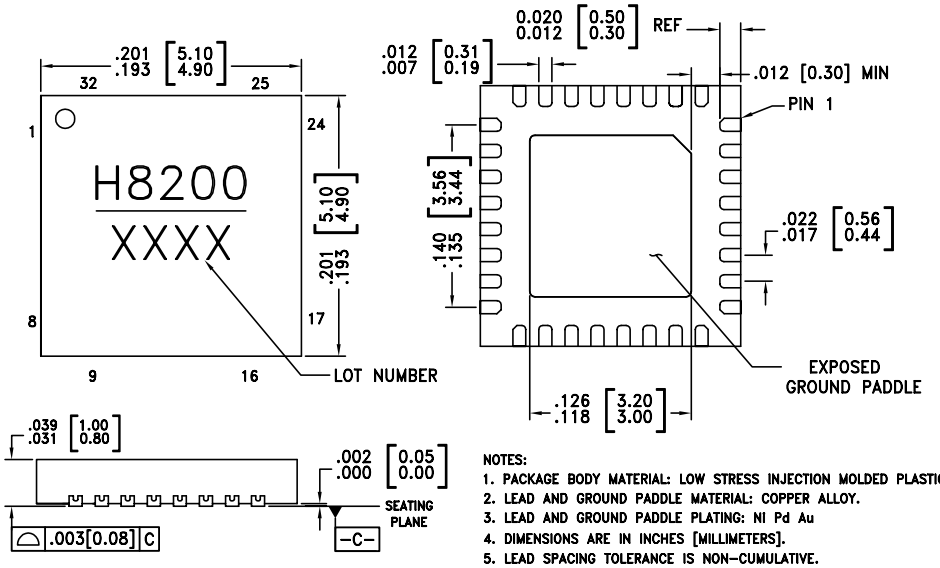
IF Input	+10 dBm
LO Input	+10 dBm
V_{CCx}	-0.5 V to +5.5 V
Digital Input/Output	-0.3 V to +3.6 V
Storage Temperature	-65°C to 150°C
ESD Sensitivity (HBM)	2000 V (Class 2)

Table 6. Reliability Infomration

Maximum Junction Temperature to Maintain 1 Million Hour MTTF	150 °C
Thermal Resistance (R_{TH}) (junction to ground paddle)	11 °C/W
Operating Temperature	-40°C to +85°C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: NI Pd Au
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. CHARACTERS TO BE HELVETICA MEDIUM, .025 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
7. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
8. PACKAGE WARP SHALL NOT EXCEED 0.05mm
9. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
10. REFER TO ADI APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Table 7. Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating [2]	Package Marking [1]
HMC8200LP5ME	32-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	100% matte Sn	MSL3	H8200 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

Table 8. Pin Descriptions

Pin Number	Function	Description
1	SDO	SPI Serial Data Output.
2	DVDD	SPI Digital Supply. Refer to the typical application circuit for required external components.
3	RST	SPI Reset. Connect to logic high for normal operation.
4, 5	BB_IP, BB_IN	Positive and Negative Filter Baseband IF I Inputs.
7, 8	BB_QN, BB_QP	Negative and Positive Filter Baseband IF Q Inputs.
6	VCC_DGA	Power Supply for the Digital Variable Gain Amplifier. Refer to the typical application circuit for required external components.
14	VCC_BG	Band Gap Supply. Power Supply Voltage for the Bias Controller. Refer to the typical application circuit for required external components.
16	VCC_LOG	RF Log Detector Supply. Refer to the typical application circuit for required external components.
17	VCC_AMP	Power Supply for the RF Output Amplifier. Refer to the typical application circuit for required external components.
19	VCC_VGA	Power Supply for the Variable Gain Amplifier. Refer to the typical application circuit for required external components.
22	VCC_D2S	Differential to Single Amplifier Supply. Refer to the typical application circuit for required external components.
26	VCC_ENV	Envelope Detector Supply. Refer to the typical application circuit for required external components.
27	VCC_IRM	Power Supply for the Mixer Output. Refer to the typical application circuit for required external components.
9	TX_IFIN	TX IF Input. Intermediate Frequency Input Port. This pin is matched to 50 Ω.
10	DGA_S1_OUT	Power Supply for the First Stage Digital Gain Amplifier. This pin is matched to 50 Ohms. Refer to the typical application circuit for required external components.
11	DGA_S2_IN	Second Stage Digital Gain Amplifier Input.
12	LOG_IF	IF Log Detector Output.
13	SLPD_OUT	Square Law Detector Output.
15	LOG_RF	RF Log Detector Output.
18	TX_OUT	Tx Chip Output.
20	VGA_CTL	VGA Control Voltage. Refer to the typical application circuit for required external components.
21	VVA_IN	VVA Intermediate Frequnecy Input Port.This pin is matched to 50Ω..
23	D2S_OUT	Differential to Single Amplifier Intermediate Frequnecy Ouput Port.This pin is matched to 50Ω.
24	ENV_N	Envelope Detector Output.
25	ENV_P	Envelope Detector Output.
28	LO_N	Local Oscillator Input. This pin is ac-coupled and matched to 50 Ω.
29	LO_P	Local Oscillator Input. This pin is ac-coupled and matched to 50 Ω.
30	SEN	SPI Serial Enable.
31	SCLK	SPI Clock Digital Input.
32	SDI	SPI Serial Data Input.
	EPAD	Exposed Pad. Connect to a low impedance thermal and electrical ground plane.

Theory of Operation

The HMC8200LP5ME is a highly integrated intermediate frequency transmitter chip that converts intermediate frequency (IF) to a single ended radio frequency (RF) signal at its output. The intermediate frequency (IF) can supplied to the HMC8200LP5ME singled ended or through the baseband differential inputs.

The single ended input of the HMC8200LP5ME utilizes an input digital gain amplifier (DGA) is controlled via SPI, which feeds the intermediate frequency (IF) signals to an image reject mixer. At the input of the device before the digital amplifier (DGA) an intermediate log power detector can be used to monitor input power levels into the device. A square law detector follows the digital gain amplifier to monitor the power entering the mixer. Please refer to the Register Array Assignments for more information regarding the digital gain amplifier control (DGA). The baseband differential inputs of the HMC8200LP5ME feed the intermediate frequency directly into the image reject mixer. It is recommended while using the single ended input that the baseband differential inputs are left not connected. The local oscillator port can either be driven single ended through LON or differentially through the combination of LON and LOP. If the local oscillator port is driven differential the LO to RF rejection will improve.

The intermediate frequency (IF) is then converted to radio frequency (RF), which is then followed by an amplifier. The amplified radio frequency (RF) signal is then fed off chip to a low pass filter. The external filter path feeds back into a variable gain amplifier (VGA) that is voltage controlled. The output of the variable gain amplifier (VGA) drives a final amplifier that is the output of the device. A radio frequency (RF) log detector is connected to the output of the final amplifier to monitor the output power of the HMC8200LP5ME.

Register Array Assignments and Serial Interface

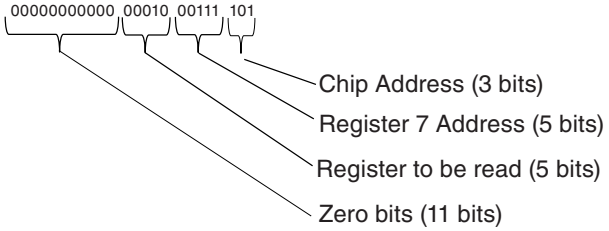
The register arrays for the HMC8200LP5ME are organized into 7 registers of 16 bits. Using the serial interface, the arrays are written or read one row at a time as shown in Figure 1 and Figure 2. Figure 1 shows the sequence of signals on the ENABLE (SEN), CLK, and DATA (SDI) lines to write one 16-bit array of data to a single register. The ENABLE line goes low, the first of 24 data bits is placed on the DATA line and the data is sampled-in on the rising edge of the clock. The DATA line should remain stable for at least 2 ns after the rising edge of CLK. The device will support a serial interface running up to 10 MHz, the interface is 3.3V CMOS logic.

A write operation requires 24 data bits and 24 clock pulses, as shown in Figure 1. The 24 data bits contain the 3-bit chip address, followed by the 5-bit register array number, and finally the 16-bit register data. After the 24th clock pulses of the write operation, the ENABLE line returns high to load the register array on the IC.

A read operation requires 24 data bits and 48 clock pulses, as shown in figure 2. For every register read operation you must first write to register 7. The data written should contain the 3-bit chip address, followed by the 5-bit register number for register 7, and finally the 5-bit number of the register to be read. The remaining 11 bits should be logic zeros. When the read operation is initiated the data is available on the Data Output (SDO) pin.

Read Example:

If reading register 2, the following 24 bits should be written to initiate the read operation.



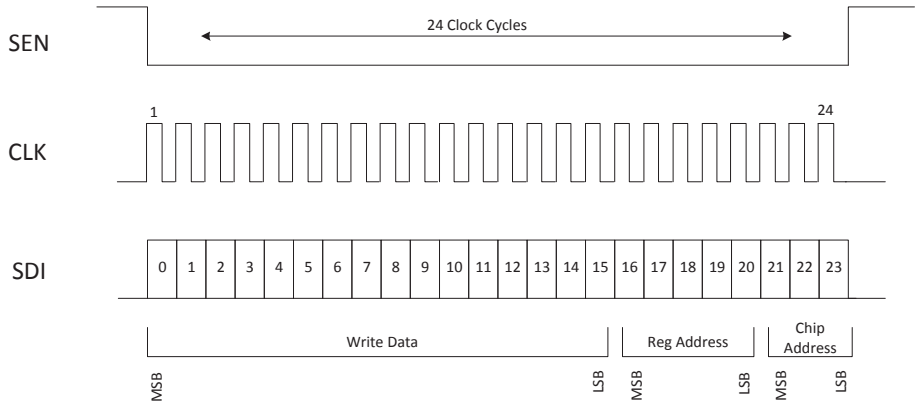


Figure 1. *Timing Diagram for writing to a register using the SPI*

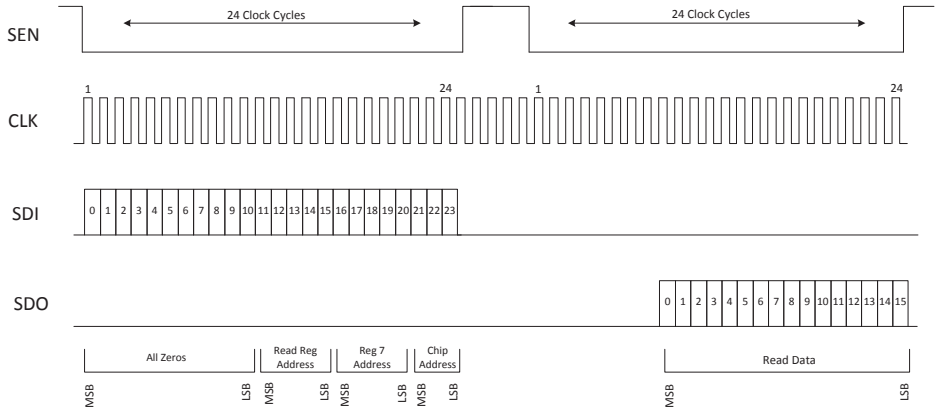


Figure 2. *Timing Diagram for reading a register using the SPI*

Register Array Assignments

Table 9. Bit Description for Enables - Register 0x01

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	Reserved		Not Used	0x6	R/W
12	LOG_IF_EN	0 1	Log Intermediate Frequency (IF) Detector Enable Disable Enable	0x1	R/W
11	D2SE_EN	0 1	Differential to Single (After Mixer) Enable Disable Enable	0x1	R/W
10	Factory Diagnostics	0	Logic 0 for normal operation	0x0	R/W
9	CM_BUFFER_EN	0 1	Common Mode Buffer Enable Disable Enable	0x0	R/W
8	Factory Diagnostics	1	Logic 1 for normal operation	0x1	R/W
7	LOG_DET_EN	0 1	Log Detector Enable Disable Enable	0x1	R/W
6	MS_EN	0 1	Square Detector Enable Disable Enable	0x1	R/W
5	ENVELOPE_EN	0 1	Envelope Detector Enable Enable Disable	0x1	R/W
4	VGA_EN	0 1	Variable Gain Amplifier (VGA) Enable Disable Enable	0x1	R/W
3	IRM_EN	0 1	Image Reject Mixer Enable Disable Enable	0x1	R/W
2	IRM_IQ_EN	0 1	IQ Line Enable Disable Enable	0x0	R/W
1	DGA_EN	0 1	Digital Gain Amplifier (DGA) Enable Disable Enable	0x1	R/W
0	LPF_EN	0 1	Low Pass Filter Enable Disable Enable	0x0	R/W

Table 10. Bit Description for Digital Gain Amplifier (DGA) - Register 0x03

Bits	Bit Name	Settings	Description	Reset	Access
15	Reserved		Not Used	0x0	R/W
[14:9]	DGA_CTRL	0 1 ... 100011	Override SPI FIL2_FRQ_SET and Use 8 Bit Word from OTP Minimum Gain ... Maximum Gain	0x0	R/W
[8:0]	Reserved		Not Used	0x0	R/W

Table 11. Bit Description - Register 0x04

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Reserved		Not Used	"0000111"	R/W
[8:7]	AMP_CUR		Amp Current	"11"	R/W
[6:2]	ENV_LVL		Envelope Level	"11100"	R/W
[1:0]	VGA_ATT_BIAS		VGA Attenuation Bias	"10"	R/W

Table 12. Bit Description for Image Reject Mixer - Register 0x05

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	Reserved		Reserved Logic "0010" for normal operation	"0010"	
11	IRM_IS	0 1	Image Sideband USB LSB	"1"	R/W
[10:9]	Reserved		Reserved Logic "01" for normal operation	"01"	R/W
8	OFFSET_POLARITY_I		Offset Polarity I	"0"	R/W
[7:0]	IRM_OFFSET_I		Image Reject Mixer Offset for I	0x0	R/W

Table 13. Bit Description for Image Reject Mixer - Register 0x06

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Reserved		Not Used	"1111000"	R/W
8	OFFSET_POLARITY_Q		Offset Polarity Q	"0"	R/W
[7:0]	IRM_OFFSET_Q		Image Reject Mixer Offset for Q	0x0	R/W

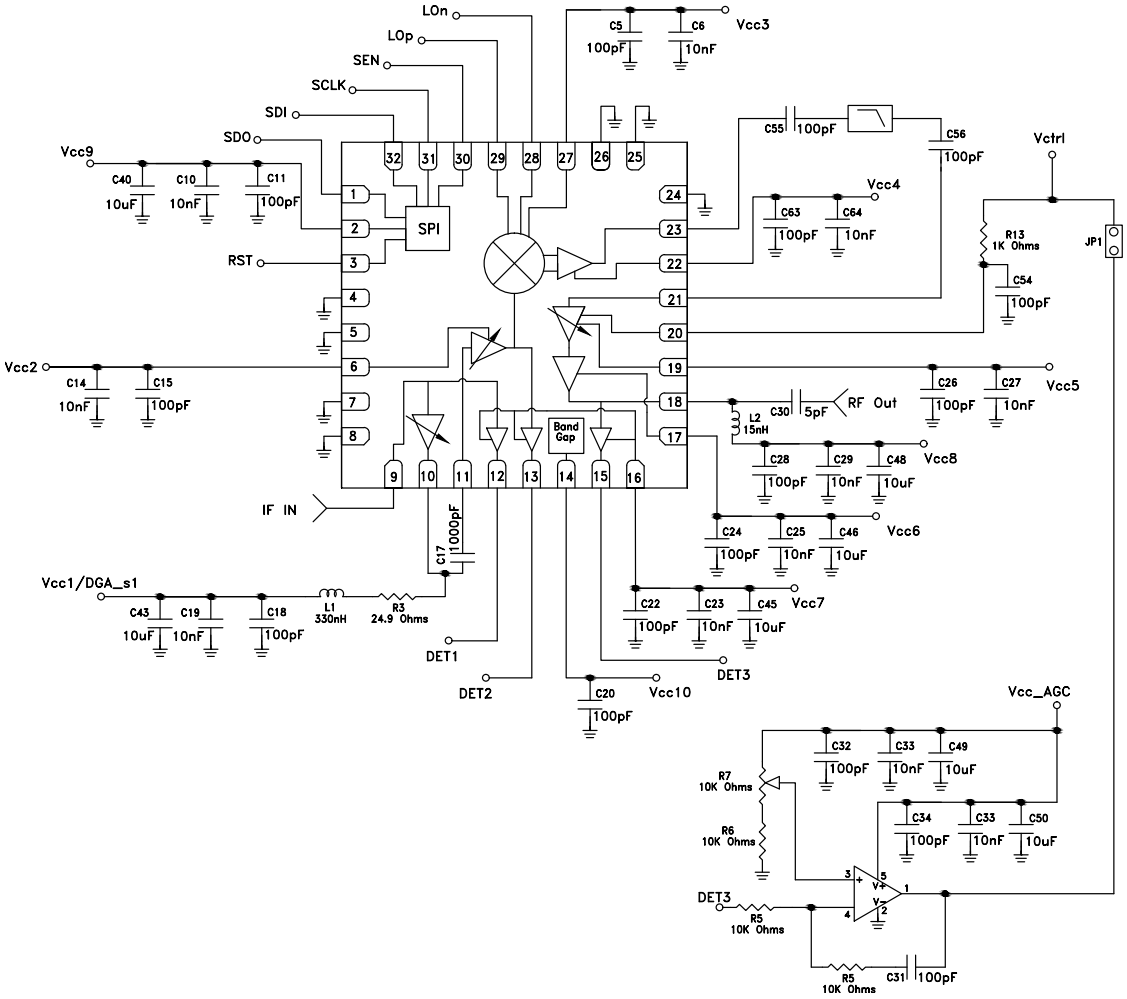
Table 14. Bit Description Phase_I - Register 0x08

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Reserved		Not Used	"1111000"	R/W
[8:0]	I_PHASE_ADJ		I Phase Adjust	0x0	R/W

Table 15. Bit Description for Phase_Q - Register 0x09

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Reserved		Not Used	"1111000"	R/W
[8:0]	Q_PHASE_ADJ		Q Phase Adjust	0x0	R/W

Evaluation PCB Schematic or Typical Application Circuit



Evaluation PCB

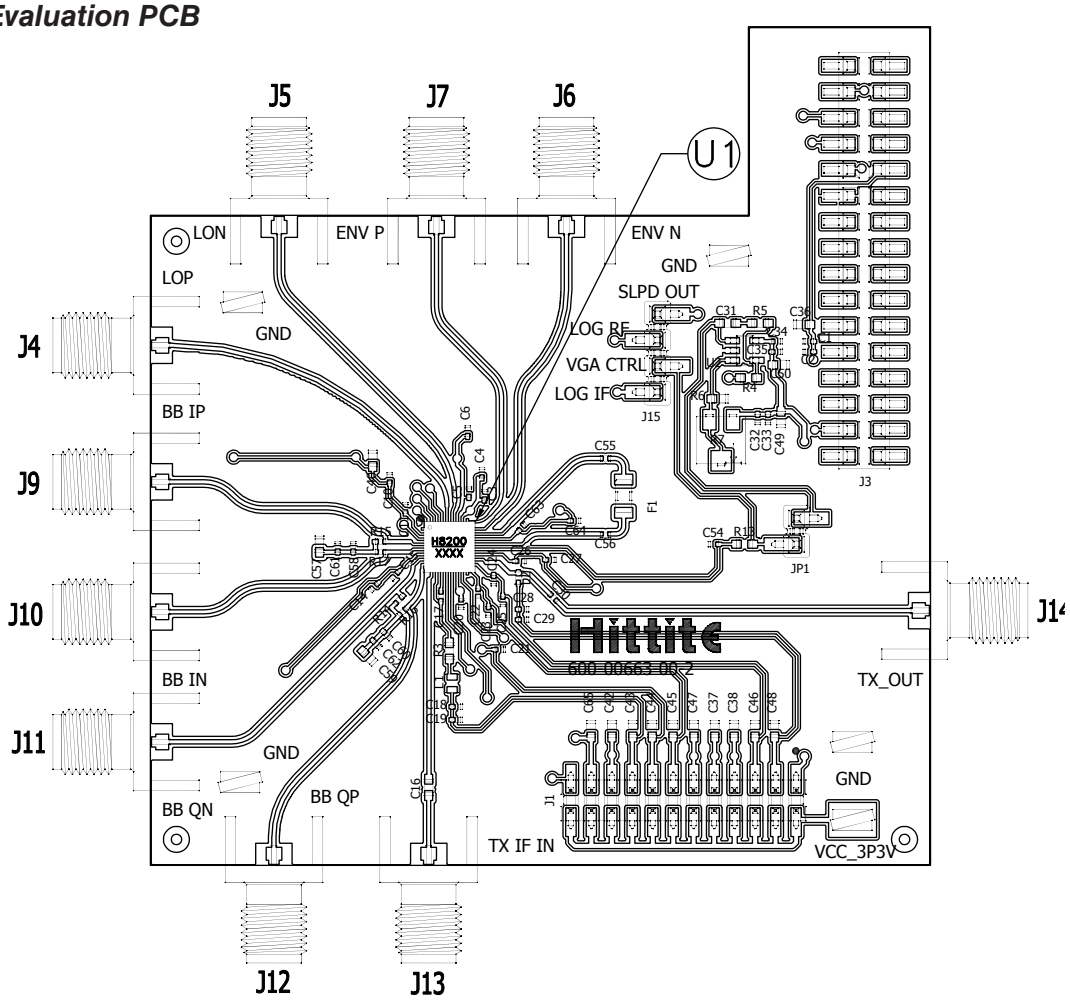


Table 16. Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	HMC8200LP5ME Evaluation PCB	EV1HMC8200LP5M [1]
Evaluation Kit	HMC8200LP5ME Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable	EK1HMC8200LP5M [2]

[1] Reference this number when ordering Evaluation PCB Only
[2] Reference this number when ordering an HMC8200LP5ME Evaluation Kit

Notes: