

Overvoltage Protection Regulator and Inrush Limiter

FEATURES

- Stops High Voltage Surges
- Adjustable Output Clamp Voltage
- Overcurrent Protection
- Wide Operation Range: 4V to 80V
- Reverse Input Protection to -60V
- Low 7 μ A Shutdown Current
- Adjustable Fault Timer
- Controls N-Channel MOSFET
- Shutdown Pin Withstands -60V to 100V
- Fault Output Indication
- Spare Amplifier for Level Detection Comparator or Linear Regulator Controller
- Available in (4mm $\times$ 3mm) 12-Pin DFN or 10-Pin MSOP Packages

APPLICATIONS

- Automotive/Avionic Surge Protection
- Hot Swap/Live Insertion
- High Side Switch for Battery Powered Systems

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DESCRIPTION

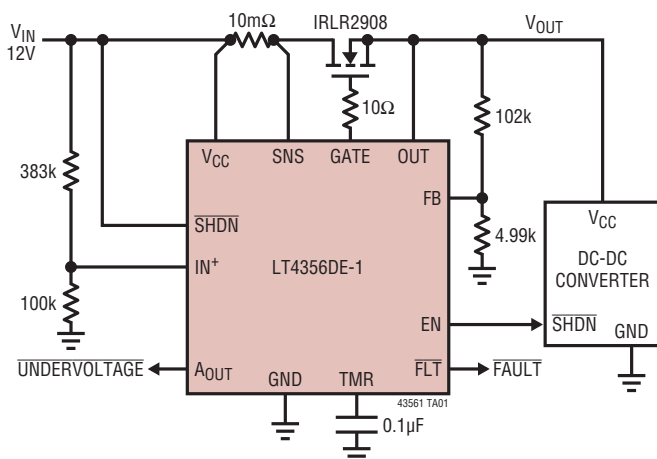
The LT[®]4356-1 surge stopper protects loads from high voltage transients. It regulates the output during an overvoltage event, such as load dump in automobiles, by controlling the gate of an external N-Channel MOSFET. The output is limited to a safe value thereby allowing the loads to continue functioning. The LT4356-1 also monitors the voltage drop between the V_{CC} and SNS pins to protect against overcurrent faults. An internal amplifier limits the current sense voltage to 50mV. In either fault condition, a timer is started inversely proportional to MOSFET stress. If the timer expires, the $\overline{\text{FLT}}$ pin pulls low to warn of an impending power down. If the condition persists, the MOSFET is turned off.

The spare amplifier may be used as a voltage detection comparator or as a linear regulator controller driving an external PNP pass transistor.

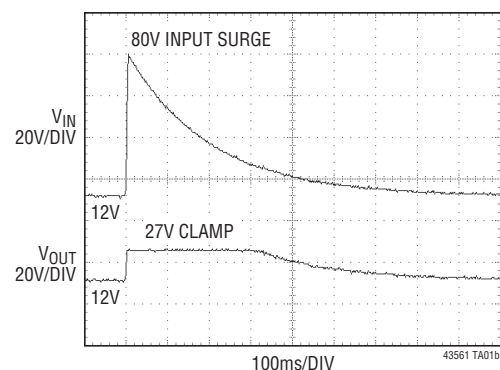
Back-to-back FETs can be used in lieu of a Schottky diode for reverse input protection, reducing voltage drop and power loss. A shutdown pin reduces the quiescent current to less than 7 μ A during shutdown.

TYPICAL APPLICATION

4A, 12V Overvoltage Output Regulator



**Overvoltage Protector Regulates
Output at 27V During Transient**



LT4356-1

ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

V_{CC} , $\overline{SHDN}$ -60V to 100V
 SNS $V_{CC} - 30V$ or -60V to $V_{CC} + 0.3V$
 OUT, A_{OUT} , $\overline{FLT}$, EN -0.3V to 80V
 GATE (Note 3) -0.3V to $V_{OUT} + 10V$
 FB, TMR, IN^+ -0.3V to 6V
 A_{OUT} , EN, $\overline{FLT}$ -3mA

Operating Temperature Range

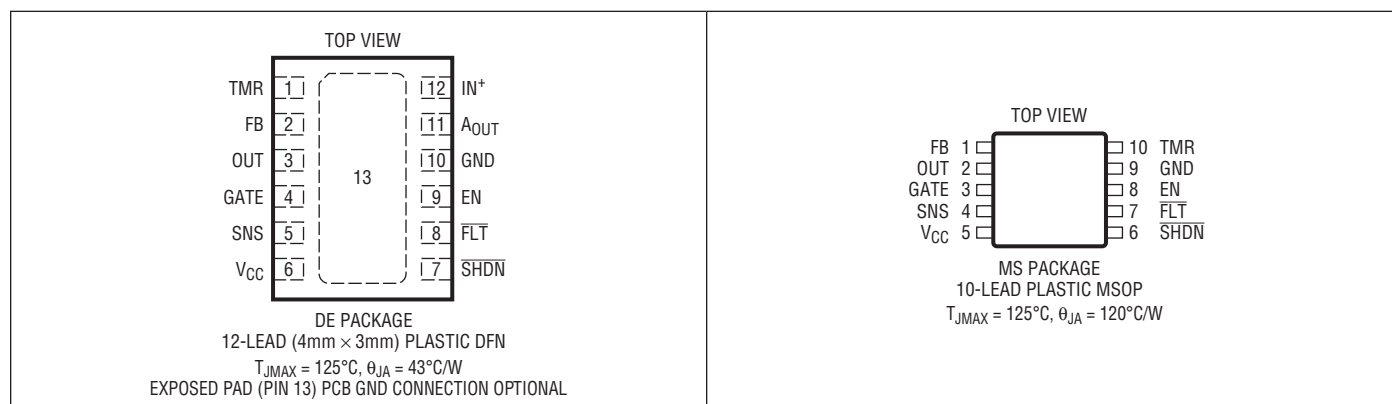
LT4356C-1 0°C to 70°C
 LT4356I-1 -40°C to 85°C
 LT4356H-1 -40°C to 125°C

Storage Temperature Range

DE12 -65°C to 125°C
 MS -65°C to 150°C

Lead Temperature (Soldering, 10 sec, MS10) 300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT4356CDE-1#PBF	LT4356CDE-1#TRPBF	43561	12-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LT4356IDE-1#PBF	LT4356IDE-1#TRPBF	43561	12-Lead (4mm × 3mm) Plastic DFN	-40°C to 85°C
LT4356HDE-1#PBF	LT4356HDE-1#TRPBF	43561	12-Lead (4mm × 3mm) Plastic DFN	-40°C to 125°C
LT4356CMS-1#PBF	LT4356CMS-1#TRPBF	LTCNS	10-Lead Plastic MSOP	0°C to 70°C
LT4356IMS-1#PBF	LT4356IMS-1#TRPBF	LTCNS	10-Lead Plastic MSOP	-40°C to 85°C
LT4356HMS-1#PBF	LT4356HMS-1#TRPBF	LTCNS	10-Lead Plastic MSOP	-40°C to 125°C
LEAD BASED FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT4356CDE-1	LT4356CDE-1#TR	43561	12-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LT4356IDE-1	LT4356IDE-1#TR	43561	12-Lead (4mm × 3mm) Plastic DFN	-40°C to 85°C
LT4356HDE-1	LT4356HDE-1#TR	43561	12-Lead (4mm × 3mm) Plastic DFN	-40°C to 125°C
LT4356CMS-1	LT4356CMS-1#TR	LTCNS	10-Lead Plastic MSOP	0°C to 70°C
LT4356IMS-1	LT4356IMS-1#TR	LTCNS	10-Lead Plastic MSOP	-40°C to 85°C
LT4356HMS-1	LT4356HMS-1#TR	LTCNS	10-Lead Plastic MSOP	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{CC} = 12\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V _{CC}	Operating Voltage Range		●	4		80	V
I _{CC}	V _{CC} Supply Current	V _{SHDN} = FLOAT	●		1	1.5	mA
		V _{SHDN} = 0V	●		7	25	μA
		LT4356I-1, LT4356C-1	●		7	30	μA
		LT4356H-1	●		7	40	μA
I _R	Reverse Input Current	V _{SNS} = V _{CC} = −30V, $\overline{\text{SHDN}}$ Open	●		0.3	1	mA
		V _{SNS} = V _{CC} = V _{SHDN} = −30V	●		0.8	2	mA
ΔV _{GATE}	GATE Pin Output High Voltage	V _{CC} = 4V; (V _{GATE} − V _{OUT}) 48V ≥ V _{CC} ≥ 8V; (V _{GATE} − V _{OUT})	● ●	4.5 10		8 18	V V
I _{GATE,UP}	GATE Pin Pull-Up Current	V _{GATE} = 12V; V _{CC} = 12V V _{GATE} = 48V; V _{CC} = 48V	● ●	−4 −4.5	−23 −30	−36 −50	μA μA
I _{GATE,DN}	GATE Pin Pull-Down Current	Overvoltage, V _{FB} = 1.4V, V _{GATE} = 12V	●	75	150		mA
		Overcurrent, V _{CC} − V _{SNS} = 120mV, V _{GATE} = 12V	●	5	10		mA
		Shutdown Mode, V _{SHDN} = 0V, V _{GATE} = 12V	●	1.5	5		mA
V _{FB}	FB Pin Servo Voltage	V _{GATE} = 12V; V _{OUT} = 12V, LT4356I-1, LT4356C-1	●	1.225	1.25	1.275	V
		V _{GATE} = 12V; V _{OUT} = 12V, LT4356H-1	●	1.215	1.25	1.275	V
I _{FB}	FB Pin Input Current	V _{FB} = 1.25V	●		0.3	1	μA
ΔV _{SNS}	Overcurrent Fault Threshold	ΔV _{SNS} = (V _{CC} − V _{SNS}), V _{CC} = 12V, LT4356I-1, LT4356C-1	●	45	50	55	mV
		ΔV _{SNS} = (V _{CC} − V _{SNS}), V _{CC} = 12V, LT4356H-1	●	42.5	50	55	mV
		ΔV _{SNS} = (V _{CC} − V _{SNS}), V _{CC} = 48V, LT4356I-1, LT4356C-1	●	46	51	56	mV
		ΔV _{SNS} = (V _{CC} − V _{SNS}), V _{CC} = 48V, LT4356H-1	●	43	51	56	mV
I _{SNS}	SNS Pin Input Current	V _{SNS} = V _{CC} = 12V to 48V	●	5	10	22	μA
I _{LEAK}	$\overline{\text{FLT}}$, EN Pins Leakage Current	$\overline{\text{FLT}}$, EN = 80V	●			2.5	μA
	A _{OUT} Pin Leakage Current	A _{OUT} = 80V				4.5	μA
I _{TMR}	TMR Pin Pull-up Current	V _{TMR} = 1V, V _{FB} = 1.5V, (V _{CC} − V _{OUT}) = 0.5V	●	−1.5	−2.5	−4	μA
		V _{TMR} = 1V, V _{FB} = 1.5V, (V _{CC} − V _{OUT}) = 75V	●	−44	−50	−55	μA
		V _{TMR} = 1.3V, V _{FB} = 1.5V	●	−3.5	−5.5	−8	μA
		V _{TMR} = 1V, ΔV _{SNS} = 60mV, (V _{CC} − V _{OUT}) = 0.5V	●	−2.5	−4.5	−6.5	μA
		V _{TMR} = 1V, ΔV _{SNS} = 60mV, (V _{CC} − V _{OUT}) = 80V	●	−195	−260	−315	μA
	TMR Pin Pull-down Current	V _{TMR} = 1V, V _{FB} = 1V, ΔV _{SNS} = 0V	●	1.7	2.2	2.7	μA
V _{TMR}	TMR Pin Thresholds	$\overline{\text{FLT}}$ From High to Low, V _{CC} = 5V to 80V	●	1.22	1.25	1.28	V
		V _{GATE} From Low to High, V _{CC} = 5V to 80V	●	0.48	0.5	0.52	V
ΔV _{TMR}	Early Warning Period	From $\overline{\text{FLT}}$ going Low to GATE going Low, V _{CC} = 5V to 80V	●	80	100	120	mV
V _{IN} ⁺	IN ⁺ Pin Threshold		●	1.22	1.25	1.28	V
I _{IN} ⁺	IN ⁺ Pin Input Current	V _{IN} ⁺ = 1.25V	●		0.3	1	μA
V _{OL}	$\overline{\text{FLT}}$, EN, A _{OUT} Pins Output Low	I _{SINK} = 2mA	●		2	8	V
		I _{SINK} = 0.1mA	●		300	800	mV
I _{OUT}	OUT Pin Input Current	V _{OUT} = V _{CC} = 12V	●		200	300	μA
		V _{OUT} = V _{CC} = 12V, V _{SHDN} = 0V	●		6	12	mA
ΔV _{OUT}	OUT Pin High Threshold	ΔV _{OUT} = V _{CC} − V _{OUT} ; EN From Low to High	●	0.25	0.5	0.7	V
V _{SHDN}	$\overline{\text{SHDN}}$ Pin Threshold	V _{CC} = 12V to 48V		0.6	1.4	1.7	V
			●	0.4		2.1	V
V _{SHDN(FLT)}	$\overline{\text{SHDN}}$ Pin Float Voltage	V _{CC} = 12V to 48V	●		1.7	2.2	V
I _{SHDN}	$\overline{\text{SHDN}}$ Pin Current	V _{SHDN} = 0V	●	−1	−4	−8	μA
t _{OFF(OC)}	Overcurrent Turn Off Delay Time	GATE From High to Low, ΔV _{SNS} = 0 → 120mV	●		2	4	μs
t _{OFF(OV)}	Overvoltage Turn Off Delay Time	GATE From High to Low, V _{FB} = 0 → 1.5V	●		0.25	1	μs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

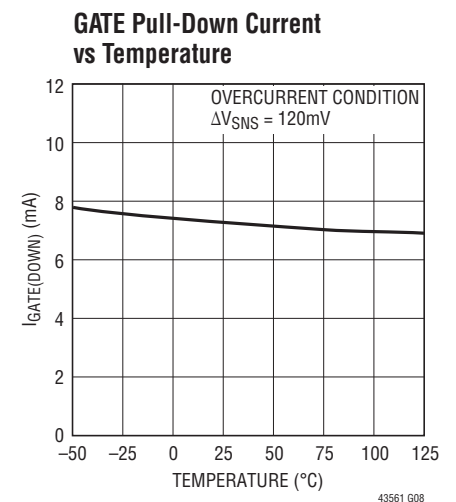
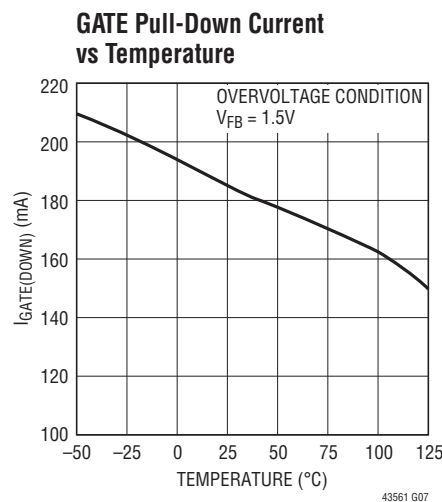
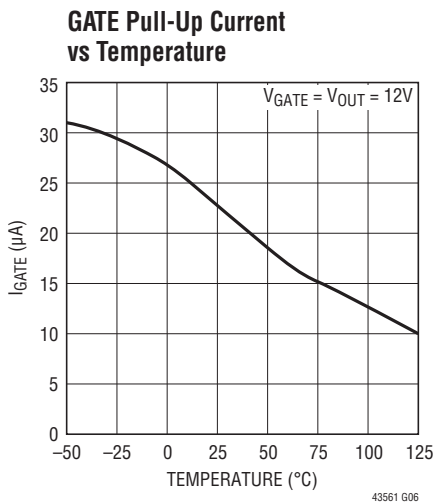
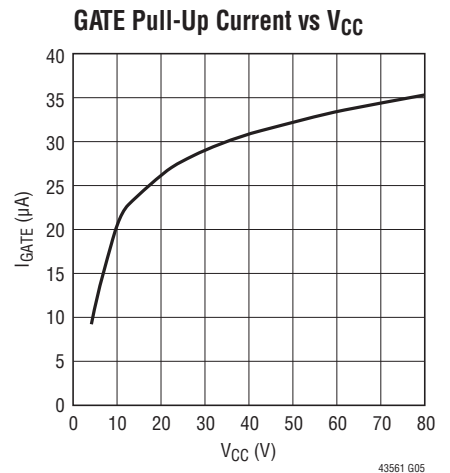
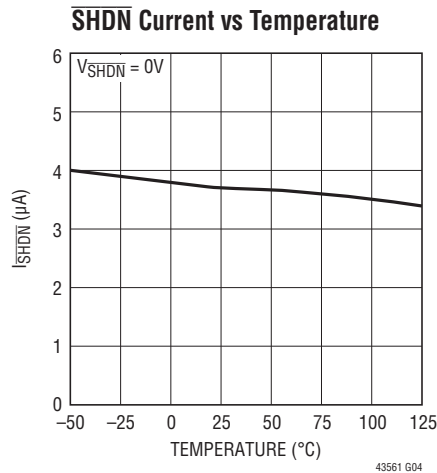
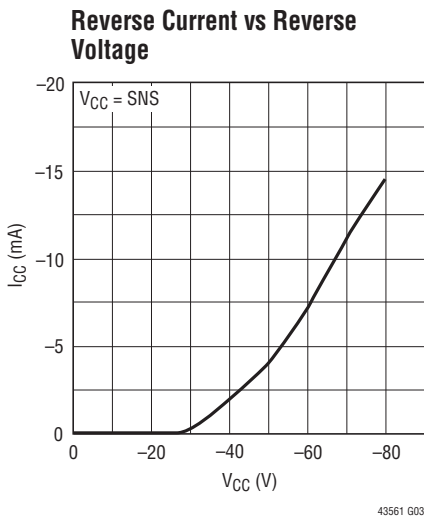
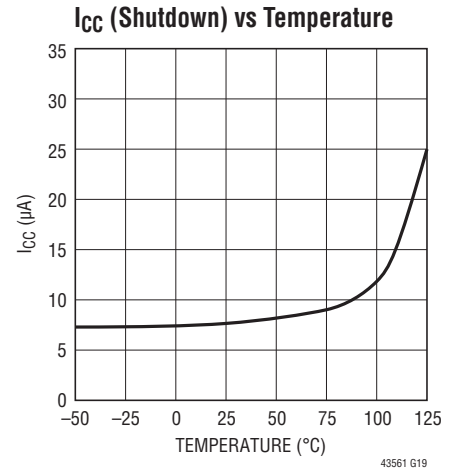
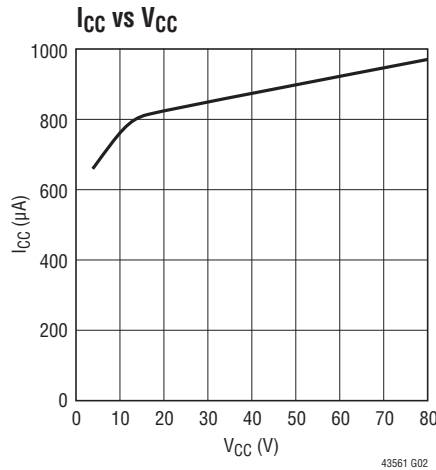
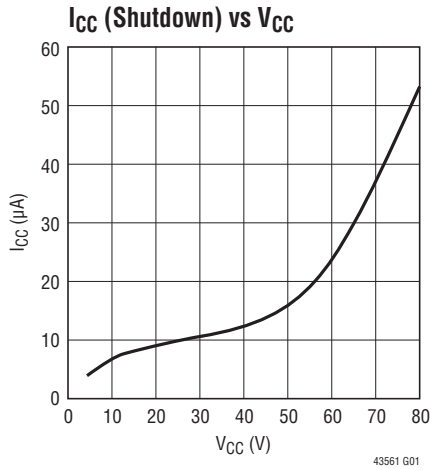
Note 2: All currents into device pins are positive; all currents out of device

pins are negative. All voltages are referenced to GND unless otherwise specified.

Note 3: An internal clamp limits the GATE pin to a minimum of 10V above the OUT pin. Driving this pin to voltages beyond the clamp may damage the device.

TYPICAL PERFORMANCE CHARACTERISTICS

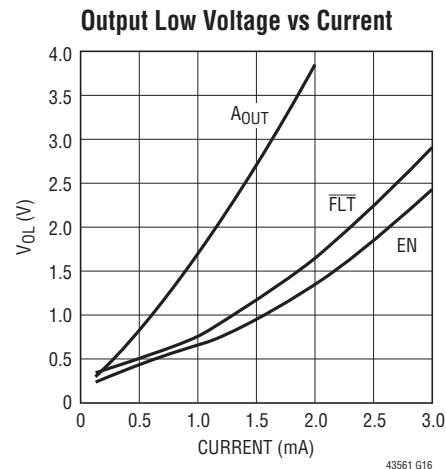
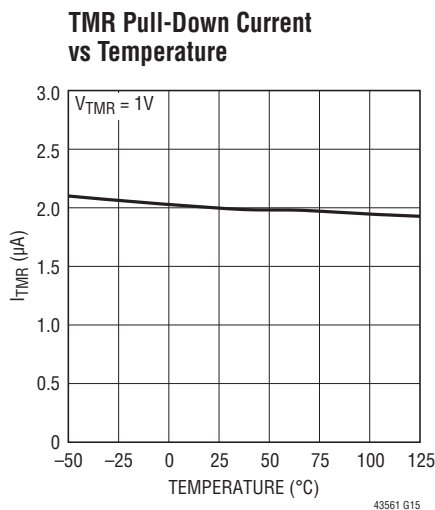
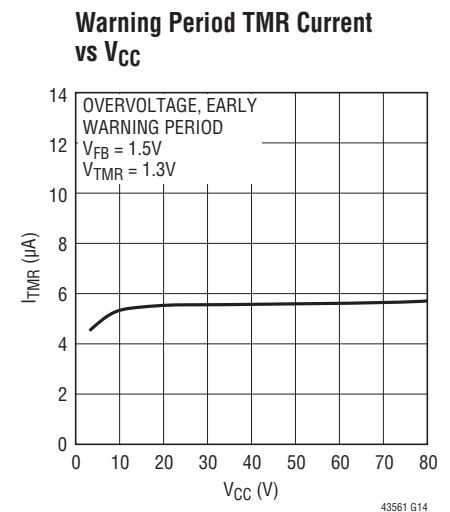
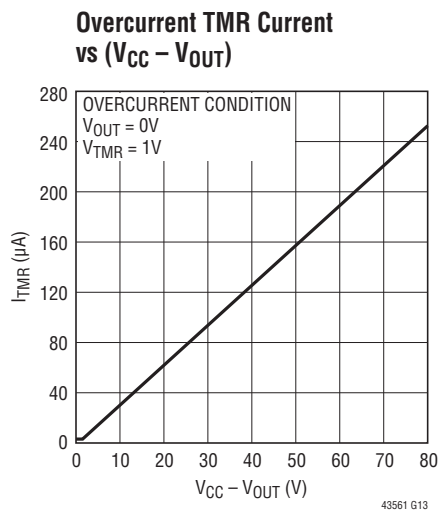
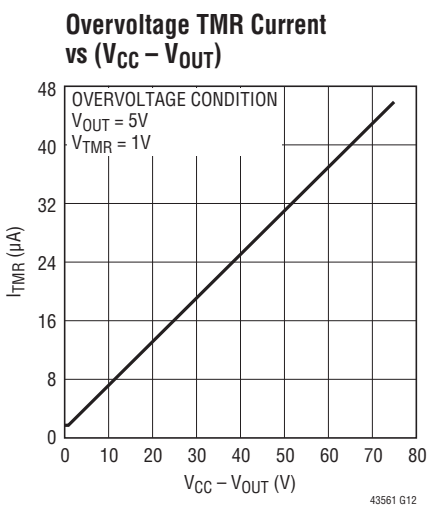
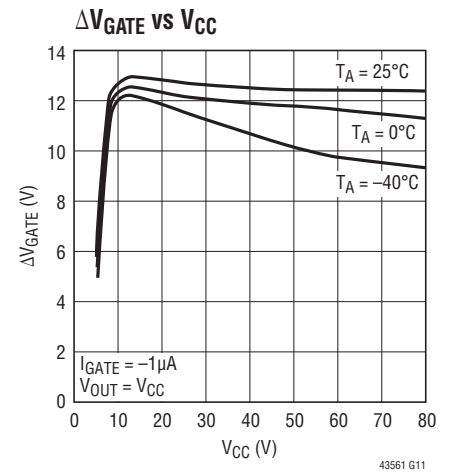
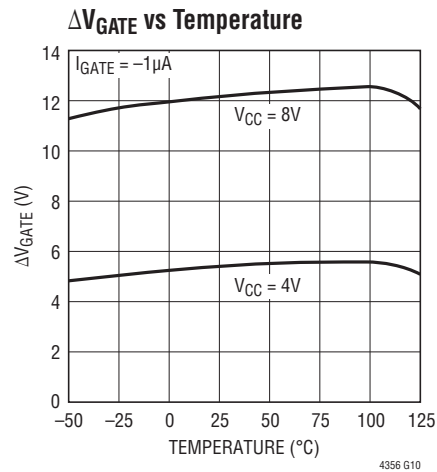
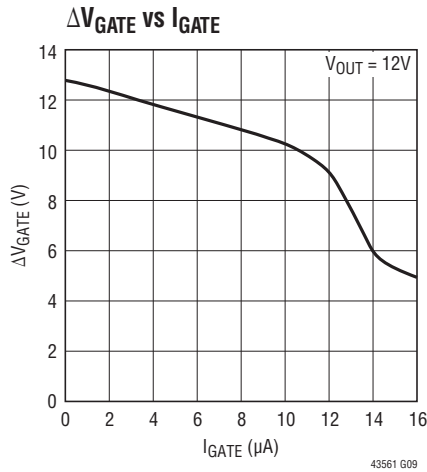
Specifications are at $V_{CC} = 12V$, $T_A = 25^\circ C$ unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS

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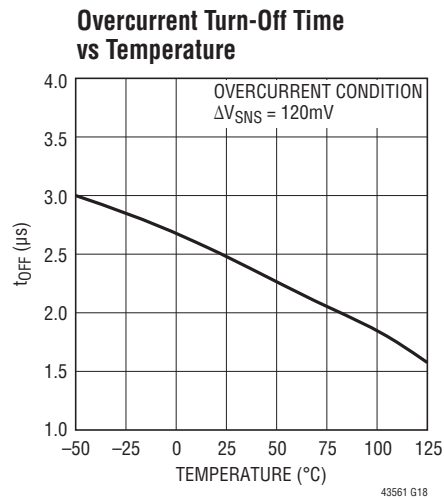
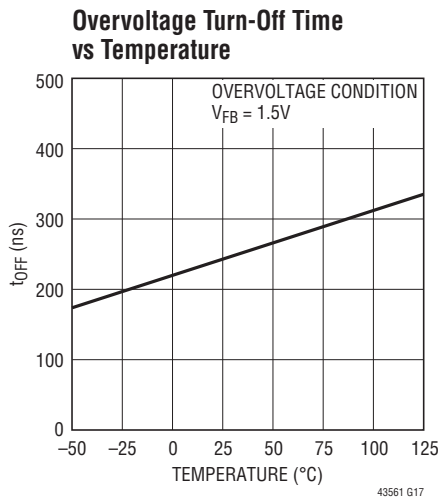
Specifications are at $V_{CC} = 12V$, $T_A = 25^\circ C$



TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at $V_{CC} = 12V$, $T_A = 25^\circ C$

unless otherwise noted.



PIN FUNCTIONS (DE/MS)

A_{OUT} (Pin 11 DE Only): Amplifier Output. Open collector output of the auxiliary amplifier. It is capable of sinking up to 2mA from 80V. The negative input of the amplifier is internally connected to a 1.25V reference.

EN (Pin 9/Pin 8): Open-Collector Enable Output. The EN pin goes high impedance when the voltage at the OUT pin is above ($V_{CC} - 0.7V$), indicating the external MOSFET is fully on. The state of the pin is latched until the OUT pin voltage resets at below 0.5V and goes back up above 2V. The internal NPN is capable of sinking up to 3mA of current from 80V to drive an LED or opto-coupler.

Exposed Pad (Pin 13 DE Only): Exposed pad may be left open or connected to device ground (GND).

FB (Pin 2/Pin 1): Voltage Regulator Feedback Input. Connect this pin to the center tap of the output resistive divider connected between the OUT pin and ground. During an overvoltage condition, the GATE pin is servoed to maintain a 1.25V threshold at the FB pin. This pin is clamped internally to 7V. Tie to GND to disable the OV clamp.

FLT (Pin 8/Pin 7): Open-Collector Fault Output. This pin pulls low after the voltage at the TMR pin has reached the fault threshold of 1.25V. It indicates the pass transistor is about to turn off because either the supply voltage has stayed at an elevated level for an extended period of time (voltage fault) or the device is in an overcurrent

condition (current fault). The internal NPN is capable of sinking up to 3mA of current from 80V to drive an LED or opto-coupler.

GATE (Pin 4/Pin 3): N-Channel MOSFET Gate Drive Output. The GATE pin is pulled up by an internal charge pump current source and clamped to 14V above the OUT pin. Both voltage and current amplifiers control the GATE pin to regulate the output voltage and limit the current through the MOSFET.

GND (Pin 10/Pin 9): Device Ground.

IN⁺ (Pin 12 DE Only): Positive Input of the Auxiliary Amplifier. This amplifier can be used as a level detection comparator with external hysteresis or linear regulator controlling an external PNP transistor. This pin is clamped internally to 7V. Connect to ground if unused.

OUT (Pin 3/Pin 2): Output Voltage Sense Input. This pin senses the voltage at the source of the N-channel MOSFET and sets the fault timer current. When the OUT pin voltage reaches 0.7V away from V_{CC} , the EN pin goes high impedance.

SHDN (Pin 7/Pin 6): Shutdown Control Input. The LT4356-1 can be shutdown to a low current mode by pulling the SHDN pin below the shutdown threshold of 0.6V. Pull this pin above 1.7V or disconnect it and allow the inter-

nal current source to turn the part back on. The leakage current to ground at the pin should be limited to no more than $1\mu\text{A}$ if no pull up device is used to turn the part on. The $\overline{\text{SHDN}}$ pin can be pulled up to 100V or below GND by 60V without damage.

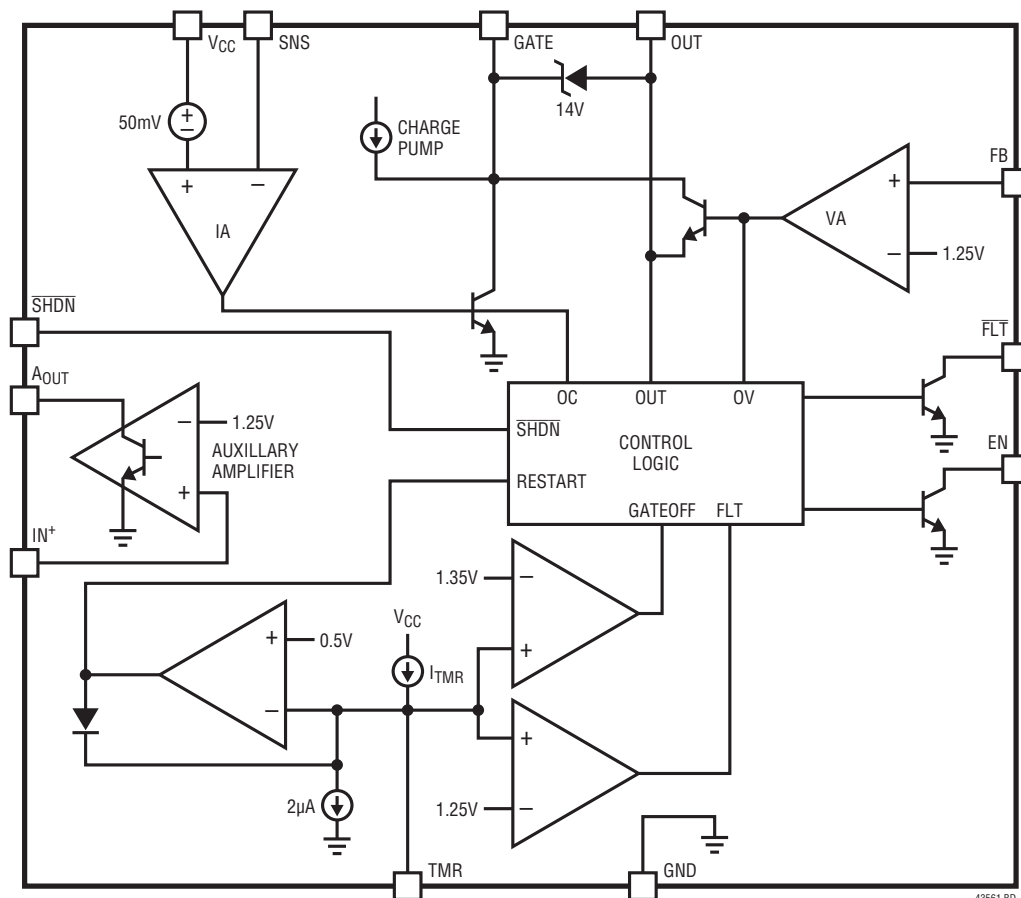
SNS (Pin 5/Pin 4): Current Sense Input. Connect this pin to the output of the current sense resistor. The current limit circuit controls the GATE pin to limit the sense voltage between V_{CC} and SNS pins to 50mV. At the same time the sense amplifier also starts a current source to charge up the TMR pin. This pin can be pulled below GND by up to 60V, though the voltage difference with the V_{CC} pin must be limited to less than 30V. Connect to V_{CC} if unused.

TMR (Pin 1/Pin 10): Fault Timer Input. Connect a capacitor between this pin and ground to set the times for early warning, fault and cool down periods. The current

charging up this pin during fault conditions depends on the voltage difference between the V_{CC} and OUT pins. When V_{TMR} reaches 1.25V, the $\overline{\text{FLT}}$ pin pulls low to indicate the detection of a fault condition. If the condition persists, the pass transistor turns off when V_{TMR} reaches the threshold of 1.35V. The pull up current stops and a $2\mu\text{A}$ current source starts to pull the TMR pin down as soon as the fault condition disappears. When V_{TMR} reaches the retry threshold of 0.5V, the GATE pin pulls high turning back on the pass transistor.

V_{CC} (Pin 6/Pin 5): Positive Supply Voltage Input. The positive supply input ranges from 4V to 80V for normal operation. It can also be pulled below ground potential by up to 60V during a reverse battery condition, without damaging the part. The supply current is reduced to $7\mu\text{A}$ with all the functional blocks off.

BLOCK DIAGRAM



43561 BD

43561fd

OPERATION

Some power systems must cope with high voltage surges of short duration such as those in automobiles. Load circuitry must be protected from these transients, yet high availability systems must continue operating during these events.

The LT4356-1 is an overvoltage protection regulator that drives an external N-channel MOSFET as the pass transistor. It operates from a wide supply voltage range of 4V to 80V. It can also be pulled below ground potential by up to 60V without damage. The low power supply requirement of 4V allows it to operate even during cold cranking conditions in automotive applications. The internal charge pump turns on the N-channel MOSFET to supply current to the loads with very little power loss. Two MOSFETs can be connected back to back to replace an inline Schottky diode for reverse input protection. This improves the efficiency and increases the available supply voltage level to the load circuitry during cold crank.

Normally, the pass transistor is fully on, powering the loads with very little voltage drop. When the supply voltage surges too high, the voltage amplifier (VA) controls the gate of the MOSFET and regulates the voltage at the source pin to a level that is set by the external resistor divider from the OUT pin to ground and the internal 1.25V reference. A current source starts charging up the capacitor connected at the TMR pin to ground. If the voltage at the TMR pin, V_{TMR} , reaches 1.25V, the $\overline{FLT}$ pin pulls low to indicate impending turn-off due to the overvoltage condition. The pass transistor stays on until the TMR pin reaches 1.35V, at which point the GATE pin pulls low turning off the MOSFET.

The potential at the TMR pin starts decreasing as soon as the overvoltage condition disappears. When the voltage at the TMR pin reaches 0.5V the GATE pin begins rising, turning on the MOSFET. The $\overline{FLT}$ pin will then go to a high impedance state.

The fault timer allows the loads to continue functioning during short transient events while protecting the MOSFET from being damaged by a long period of supply overvoltage, such as a load dump in automobiles. The timer period varies with the voltage across the MOSFET. A higher voltage corresponds to a shorter fault timer period, ensuring the MOSFET operates within its safe operating area (SOA).

The LT4356-1 senses an overcurrent condition by monitoring the voltage across an optional sense resistor placed between the V_{CC} and SNS pins. An active current limit circuit (IA) controls the GATE pin to limit the sense voltage to 50mV. A current is also generated to start charging up the TMR pin. This current is about 5 times the current generated during an overvoltage event. The $\overline{FLT}$ pin pulls low when the voltage at the TMR pin reaches 1.25V and the MOSFET is turned off when it reaches 1.35V.

A spare amplifier (SA) is provided with the negative input connected to an internal 1.25V reference. The output pull down device is capable of sinking up to 2mA of current allowing it to drive an LED or opto coupler. This amplifier can be configured as a linear regulator controller driving an external PNP transistor or a comparator function to monitor voltages.

A shutdown pin turns off the pass transistor and reduces the supply current to less than 7 μ A.

APPLICATIONS INFORMATION

The LT4356-1 can limit the voltage and current to the load circuitry during supply transients or overcurrent events. The total fault timer period should be set to ride through short overvoltage transients while not causing damage to the pass transistor. The selection of this N-channel MOSFET pass transistor is critical for this application. It must stay on and provide a low impedance path from the input supply to the load during normal operation and then dissipate power during overvoltage or overcurrent conditions.

The following sections describe the overcurrent and the overvoltage faults, and the selection of the timer capacitor value based on the required warning time. The selection of the N-channel MOSFET pass transistor is discussed next. Auxiliary amplifier, reverse input, and the shutdown functions are covered after the MOSFET selection. External component selection is discussed in detail in the Design Example section.

Overvoltage Fault

The LTC4356-1 limits the voltage at the OUT pin during an overvoltage situation. An internal voltage amplifier regulates the GATE pin voltage to maintain a 1.25V threshold at the FB pin. During this period of time, the power MOSFET is still on and continues to supply current to the load. This allows uninterrupted operation during short overvoltage transient events.

When the voltage regulation loop is engaged for longer than the time-out period, set by the timer capacitor connected from the TMR pin to ground, an overvoltage fault is detected. The GATE pin is pulled down to the OUT pin by a 150mA current. After the fault condition has disappeared and a cool down period has transpired, the GATE pin starts to pull high again. This prevents the power MOSFET from being damaged during a long period of overvoltage, such as during load dump in automobiles.

Overcurrent Fault

The LT4356-1 features an adjustable current limit that protects against short circuits or excessive load current. During an overcurrent event, the GATE pin is regulated to limit the current sense voltage across the V_{CC} and SNS pins to 50mV.

An overcurrent fault occurs when the current limit circuitry has been engaged for longer than the time-out delay set by the timer capacitor. The GATE pin is then immediately pulled low by a 10mA current to GND turning off the MOSFET. After the fault condition has disappeared and a cool down period has transpired, the GATE pin is allowed to pull back up and turn on the pass transistor.

Fault Timer

The LT4356-1 includes an adjustable fault timer pin. Connecting a capacitor from the TMR pin to ground sets the delay timer period before the MOSFET is turned off. The same capacitor also sets the cool down period before the MOSFET is allowed to turn back on after the fault condition has disappeared.

Once a fault condition, either overvoltage or overcurrent, is detected, a current source charges up the TMR pin. The current level varies depending on the voltage drop across the drain and source terminals of the power MOSFET (V_{DS}), which is typically from the V_{CC} pin to the OUT pin. This scheme takes better advantage of the available Safe Operating Area (SOA) of the MOSFET than would a fixed timer current. The timer function operates down to $V_{CC} = 5V$ across the whole temperature range.

Fault Timer Current

The timer current starts at around 2 μA with 0.5V or less of V_{DS} , increasing linearly to 50 μA with 75V of V_{DS} during an overvoltage fault (Figure 1). During an overcurrent fault, it starts at 4 μA with 0.5V or less of V_{DS} but increases to 260 μA with 80V across the MOSFET (Figure 2). This arrangement allows the pass transistor to turn off faster during an overcurrent event, since more power is dissipated during this condition. Refer to the Typical Performance Characteristics section for the timer current at different V_{DS} in both overvoltage and overcurrent events.

When the voltage at the TMR pin, V_{TMR} , reaches the 1.25V threshold, the $\overline{FLT}$ pin pulls low to indicate the detection of a fault condition and provide warning to the load of the impending power loss. In the case of an overvoltage fault, the timer current then switches to a fixed 5 μA .

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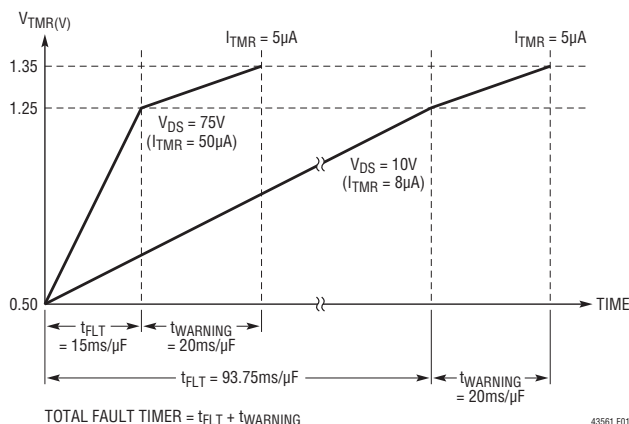


Figure 1. Overvoltage Fault Timer Current

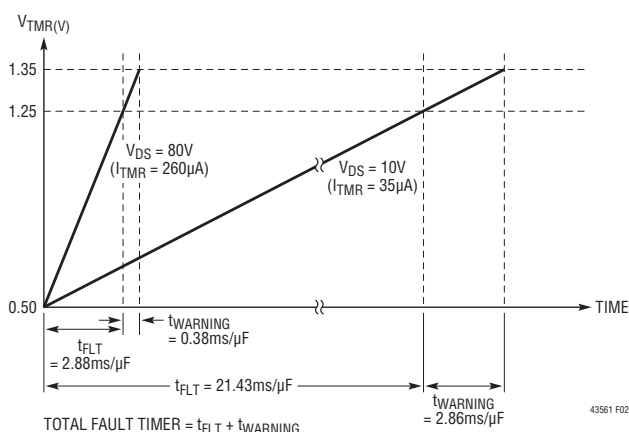


Figure 2. Overcurrent Fault Timer Current

The interval between $\overline{\text{FLT}}$ asserting low and the MOSFET turning off is given by:

$$t_{\text{WARNING}} = \frac{C_{\text{TMR}} \cdot 100\text{mV}}{5\mu\text{A}}$$

This fixed early warning period allows the systems to perform necessary backup or house keeping functions before the power supply is cut off. After V_{TMR} crosses the 1.35V threshold, the pass transistor turns off immediately. Note that during an overcurrent event, the timer current is not reduced to 5µA after V_{TMR} has reached 1.25V threshold, since it would lengthen the overall fault timer period and cause more stress on the power MOSFET.

As soon as the fault condition has disappeared, a 2µA current starts to discharge the timer capacitor to ground. When V_{TMR} reaches the 0.5V threshold, the internal charge pump starts to pull the GATE pin high, turning on the

MOSFET. The TMR pin is then actively regulated to 0.5V until the next fault condition appears. The total cool down timer period is given by:

$$t_{\text{COOL}} = \frac{C_{\text{TMR}} \cdot 0.85\text{V}}{2\mu\text{A}}$$

MOSFET Selection

The LT4356-1 drives an N-channel MOSFET to conduct the load current. The important features of the MOSFET are on-resistance $R_{\text{DS(ON)}}$, the maximum drain-source voltage $V_{(\text{BR})\text{DSS}}$, the threshold voltage, and the SOA.

The maximum allowable drain-source voltage must be higher than the supply voltage. If the output is shorted to ground or during an overvoltage event, the full supply voltage will appear across the MOSFET.

The gate drive for the MOSFET is guaranteed to be more than 10V and less than 18V for those applications with V_{CC} higher than 8V. This allows the use of standard threshold voltage N-channel MOSFETs. For systems with V_{CC} less than 8V, a logic level MOSFET is required since the gate drive can be as low as 4.5V.

The SOA of the MOSFET must encompass all fault conditions. In normal operation the pass transistor is fully on, dissipating very little power. But during either overvoltage or overcurrent faults, the GATE pin is servoed to regulate either the output voltage or the current through the MOSFET. Large current and high voltage drop across the MOSFET can coexist in these cases. The SOA curves of the MOSFET must be considered carefully along with the selection of the fault timer capacitor.

Transient Stress in the MOSFET

During an overvoltage event, the LT4356-1 drives a series pass MOSFET to regulate the output voltage at an acceptable level. The load circuitry may continue operating throughout this interval, but only at the expense of dissipation in the MOSFET pass device. MOSFET dissipation or stress is a function of the input voltage waveform, regulation voltage and load current. The MOSFET must be sized to survive this stress.

Most transient event specifications use the model shown in Figure 3. The idealized waveform comprises a linear

43561fd

APPLICATIONS INFORMATION

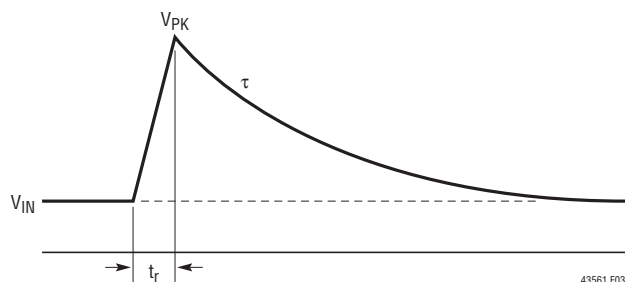


Figure 3. Prototypical Transient Waveform

ramp of rise time t_r , reaching a peak voltage of V_{PK} and exponentially decaying back to V_{IN} with a time constant of t . A common automotive transient specification has constants of $t_r = 10\mu\text{s}$, $V_{PK} = 80\text{V}$ and $\tau = 1\text{ms}$. A surge condition known as “load dump” has constants of $t_r = 5\text{ms}$, $V_{PK} = 60\text{V}$ and $\tau = 200\text{ms}$.

MOSFET stress is the result of power dissipated within the device. For long duration surges of 100ms or more, stress is increasingly dominated by heat transfer; this is a matter of device packaging and mounting, and heatsink thermal mass. For short duration transients of less than 100ms, MOSFET survival is increasingly a matter of safe operating area (SOA), an intrinsic property of the MOSFET.

SOA quantifies the time required at any given condition of V_{DS} and I_D to raise the junction temperature of the MOSFET to its rated maximum. MOSFET SOA is expressed in units of watt-squared-seconds (P^2t). This figure is essentially constant for intervals of less than 100ms for any given device type, and rises to infinity under DC operating conditions. Destruction mechanisms other than bulk die temperature distort the lines of an accurately drawn SOA graph so that P^2t is not the same for all combinations of I_D and V_{DS} . In particular P^2t tends to degrade as V_{DS} approaches the maximum rating, rendering some devices useless for absorbing energy above a certain voltage.

Calculating Transient Stress

To select a MOSFET suitable for any given application, the SOA stress must be calculated for each input transient which shall not interrupt operation. It is then a simple matter to choose a device which has adequate SOA to survive the maximum calculated stress. P^2t for a prototypical transient waveform is calculated as follows (Figure 4).

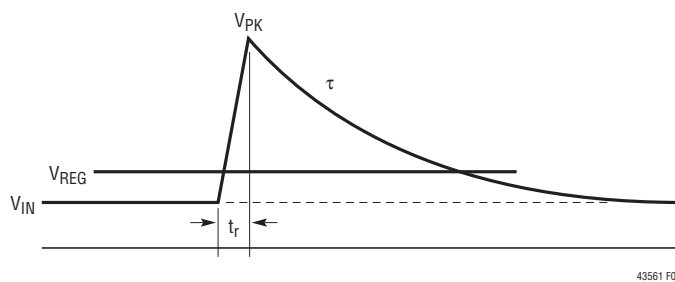


Figure 4. Safe Operating Area Required to Survive Prototypical Transient Waveform

Let

$$\begin{aligned} a &= V_{REG} - V_{IN} \\ b &= V_{PK} - V_{IN} \\ (V_{IN} &= \text{Nominal Input Voltage}) \end{aligned}$$

Then

$$P^2t = I_{LOAD}^2 \left[\frac{1}{3} t_r \frac{(b-a)^3}{b} + \frac{1}{2} \tau \left(2a^2 \ln \frac{b}{a} + 3a^2 + b^2 - 4ab \right) \right]$$

Typically $V_{REG} \approx V_{IN}$ and $\tau \gg t_r$ simplifying the above to

$$P^2t = \frac{1}{2} I_{LOAD}^2 (V_{PK} - V_{REG})^2 \tau \quad (W^2s)$$

For the transient conditions of $V_{PK} = 80\text{V}$, $V_{IN} = 12\text{V}$, $V_{REG} = 16\text{V}$, $t_r = 10\mu\text{s}$ and $\tau = 1\text{ms}$, and a load current of 3A, P^2t is $16.7\text{W}^2\text{s}$ —easily handled by a MOSFET in a D-pak package. The P^2t of other transient waveshapes is evaluated by integrating the square of MOSFET power versus time.

Calculating Short Circuit Stress

SOA stress must also be calculated for short circuit conditions. Short circuit P^2t is given by:

$$P^2t = (V_{IN} \bullet \Delta V_{SNS} / R_{SNS})^2 \bullet t_{TMR} \quad (W^2s)$$

where, ΔV_{SNS} is the SENSE pin threshold, and t_{TMR} is the overcurrent timer interval.

For $V_{IN} = 14.7\text{V}$, $V_{SNS} = 50\text{mV}$, $R_{SNS} = 12\text{m}\Omega$ and $C_{TMR} = 100\text{nF}$, P^2t is $6.6\text{W}^2\text{s}$ —less than the transient SOA calculated in the previous example. Nevertheless, to ac-

APPLICATIONS INFORMATION

count for circuit tolerances this figure should be doubled to $13.2W^2s$.

Limiting Inrush Current and GATE Pin Compensation

The LT4356-1 limits the inrush current to any load capacitance by controlling the GATE pin voltage slew rate. An external capacitor can be connected from GATE to ground to slow down the inrush current further at the expense of slower turn-off time.

The LT4356-1 does not need extra compensation components at the GATE pin for stability during an overvoltage or overcurrent event. However, with fast, high voltage transient steps at the input, a gate capacitor, C1, to ground is needed to prevent turn-on of the N-Channel MOSFET.

The extra gate capacitance slows down the turn off time during fault conditions and may allow excessive current during an output short event. An extra resistor, R1, in series with the gate capacitor can improve the turn off time. A diode, D1, should be placed across R1 with the cathode connected to C1 as shown in Figure 5.

Auxiliary Amplifier

An uncommitted amplifier is included in the LT4356-1 to provide flexibility in the system design. With the negative input connected internally to the 1.25V reference, the amplifier can be connected as a level detect comparator with external hysteresis. The open collector output pin, A_{OUT}, is capable of driving an opto or LED. It can also interface with the system via a pull-up resistor to a supply voltage up to 80V.

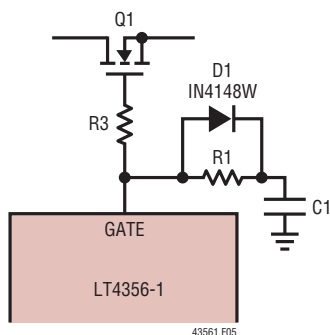


Figure 5

The amplifier can also be configured as a low dropout linear regulator controller. With an external PNP transistor, such as 2N2905A, it can supply up to 100mA of current with only a few hundred mV of dropout voltage. Current limit can be easily included by adding two diodes and one resistor (Figure 6).

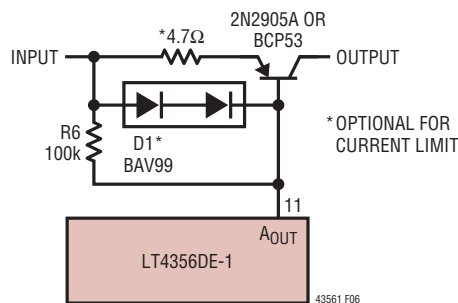


Figure 6. Auxiliary LDO Output with Optional Current Limit

Reverse Input Protection

A blocking diode is commonly employed when reverse input potential is possible, such as in automotive applications. This diode causes extra power loss, generates heat, and reduces the available supply voltage range. During cold crank, the extra voltage drop across the diode is particularly undesirable.

The LT4356-1 is designed to withstand reverse voltage without damage to itself or the load. The V_{CC}, SNS, and SHDN pins can withstand up to 60V of DC voltage below the GND potential. Back-to-back MOSFETs must be used to eliminate the current path through their body diodes (Figure 7). Figure 8 shows the approach with a P-Channel MOSFET in place of Q2.

Shutdown

The LT4356-1 can be shut down to a low current mode when the voltage at the SHDN pin goes below the shutdown threshold of 0.6V. The quiescent current drops to 7μA.

The SHDN pin can be pulled up to V_{CC} or below GND by up to 60V without damaging the pin. Leaving the pin open allows an internal current source to pull it up and turn on the part while clamping the pin to 2.5V. The leakage current at the pin should be limited to no more than 1μA if no pull up device is used to help turn it on.

APPLICATIONS INFORMATION

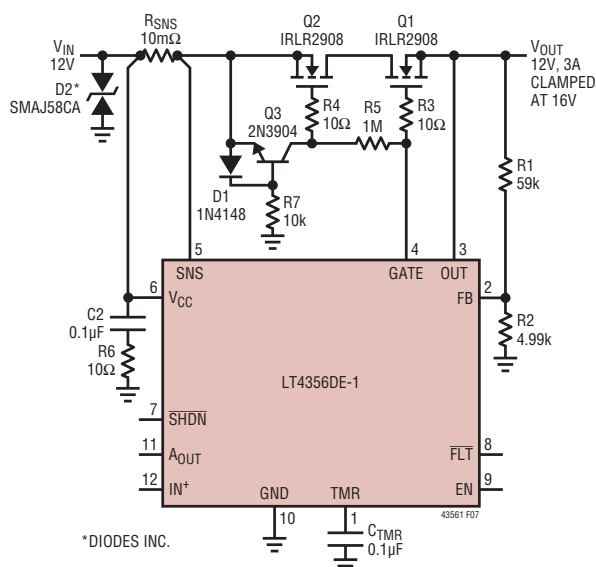


Figure 7. Overvoltage Regulator with N-Channel MOSFET Reverse Input Protection

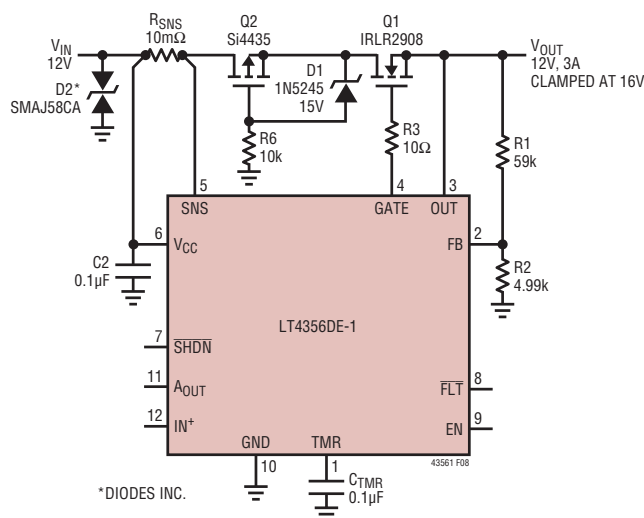


Figure 8. Overvoltage Regulator with P-Channel MOSFET Reverse Input Protection

Supply Transient Protection

The LT4356-1 is 100% tested and guaranteed to be safe from damage with supply voltages up to 80V. Nevertheless, voltage transients above 100V may cause permanent damage. During a short-circuit condition, the large change in current flowing through power supply traces and associated wiring can cause inductive voltage transients which could exceed 100V. To minimize the voltage transients, the

power trace parasitic inductance should be minimized by using wide traces. A snubber circuit dampens the ringing associated with voltage spikes. A 10Ω resistor in series with a $0.1\mu\text{F}$ capacitor between V_{CC} and GND is effective with up to $1\mu\text{H}$ feed point inductance. A surge suppressor, D2, in Figure 9, at the input will clamp the voltage spikes.

A $1\mu\text{F}$ ceramic capacitor, C_L , is needed at the OUT pin to clamp the voltage spike if the input voltage rise time is

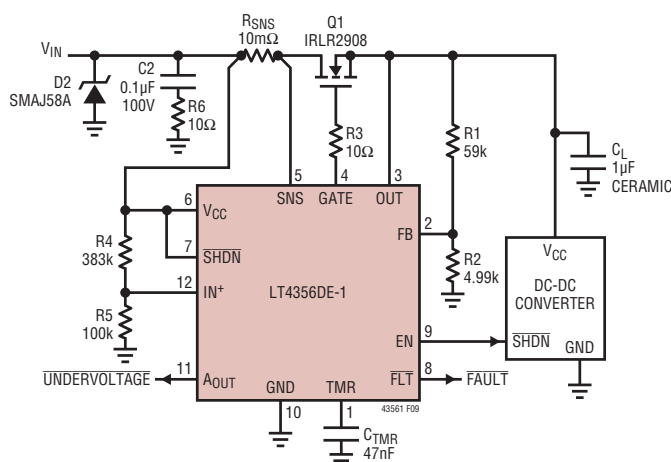


Figure 9. Overvoltage Regulator with Low Battery Detection

faster than $10\mu\text{s}$. A total bulk capacitance in the range of $22\mu\text{F}$ is also required close to the V_{CC} pin of the DC/DC converter, if not already provided by the converter.

Layout Considerations

To achieve accurate current sensing, Kelvin connection to the current sense resistor (R_{SNS} in Figure 9) is recommended. The minimum trace width for 1oz copper foil is $0.02''$ per amp to ensure the trace stays at a reasonable temperature. $0.03''$ per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about $530\mu\Omega/\text{square}$. Small resistances can cause large errors in high current applications. Noise immunity will be improved significantly by locating resistive dividers close to the pins with short V_{CC} and GND traces.

APPLICATIONS INFORMATION

Design Example

As a design example, take an application with the following specifications: $V_{CC} = 8V$ to $14V$ DC with transient up to $80V$, $V_{OUT} \leq 16V$, current limit (I_{LIM}) at $5A$, low battery detection at $6V$, and $1ms$ of overvoltage early warning (Figure 9).

First, calculate the resistive divider value to limit V_{OUT} to $16V$ during an overvoltage event:

$$V_{REG} = \frac{1.25V \cdot (R1 + R2)}{R2} = 16V$$

Set the current through $R1$ and $R2$ during the overvoltage condition to $250\mu A$.

$$R2 = \frac{1.25V}{250\mu A} = 5k\Omega$$

Choose $4.99k\Omega$ for $R2$.

$$R1 = \frac{(16V - 1.25V) \cdot R2}{1.25V} = 58.88k\Omega$$

The closest standard value for $R1$ is $59k\Omega$.

Next calculate the sense resistor, R_{SNS} , value:

$$R_{SNS} = \frac{50mV}{I_{LIM}} = \frac{50mV}{5A} = 10m\Omega$$

C_{TMR} is then chosen for $1ms$ of early warning time:

$$C_{TMR} = \frac{1ms \cdot 5\mu A}{100mV} = 50nF$$

The closest standard value for C_{TMR} is $47nF$.

Finally, calculate $R4$ and $R5$ for the $6V$ low battery threshold detection:

$$6V = \frac{1.25V \cdot (R4 + R5)}{R5}$$

Choose $100k\Omega$ for $R5$.

$$R4 = \frac{(6V - 1.25V) \cdot R5}{1.25V} = 380k\Omega$$

Select $383k\Omega$ for $R4$.

The pass transistor, $Q1$, should be chosen to withstand the output short condition with $V_{CC} = 14V$.

The total overcurrent fault time is:

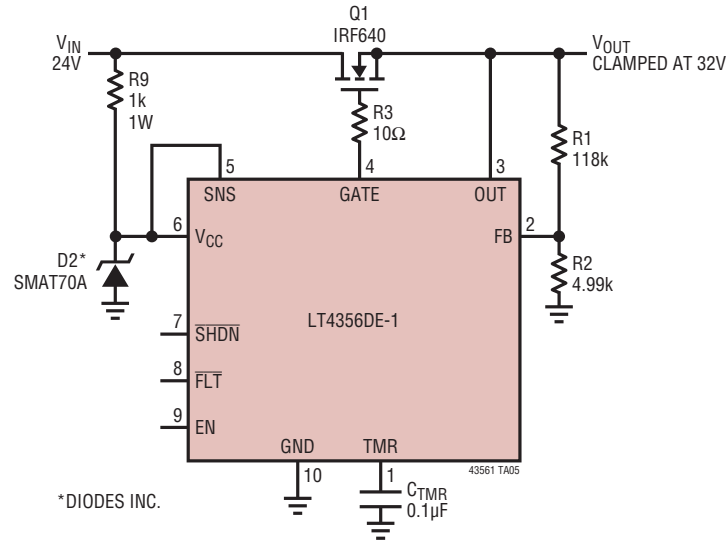
$$t_{OC} = \frac{47nF \cdot 0.85V}{45.5\mu A} = 0.878ms$$

The power dissipation on $Q1$ equals to:

$$P = \frac{14V \cdot 50mV}{10m\Omega} = 70W$$

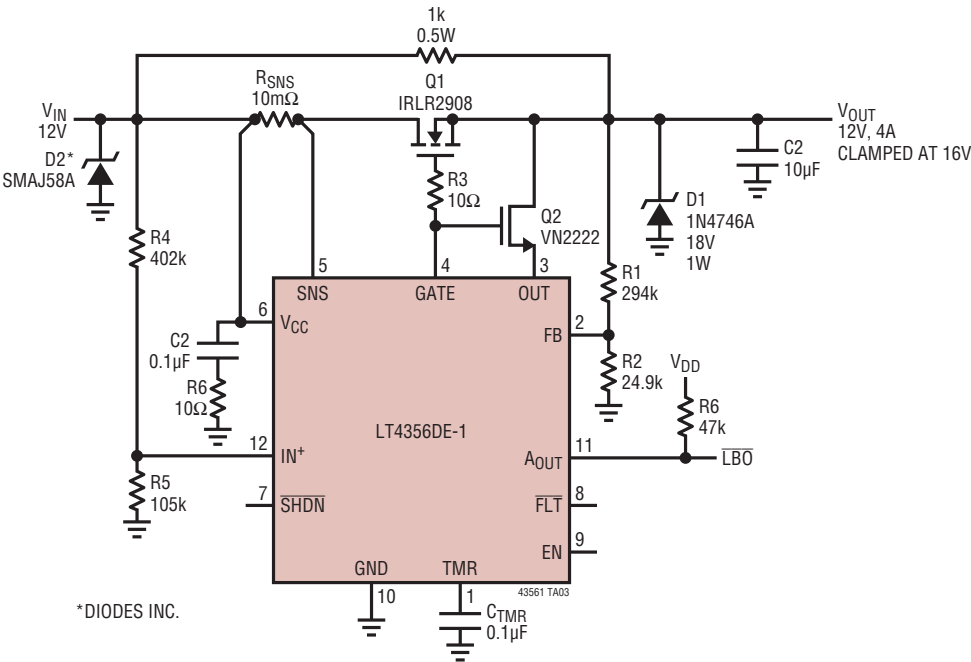
These conditions are well within the Safe Operating Area of IRLR2908.

TYPICAL APPLICATIONS

24V Overvoltage Regulator Withstands 150V at V_{IN} 

TYPICAL APPLICATIONS

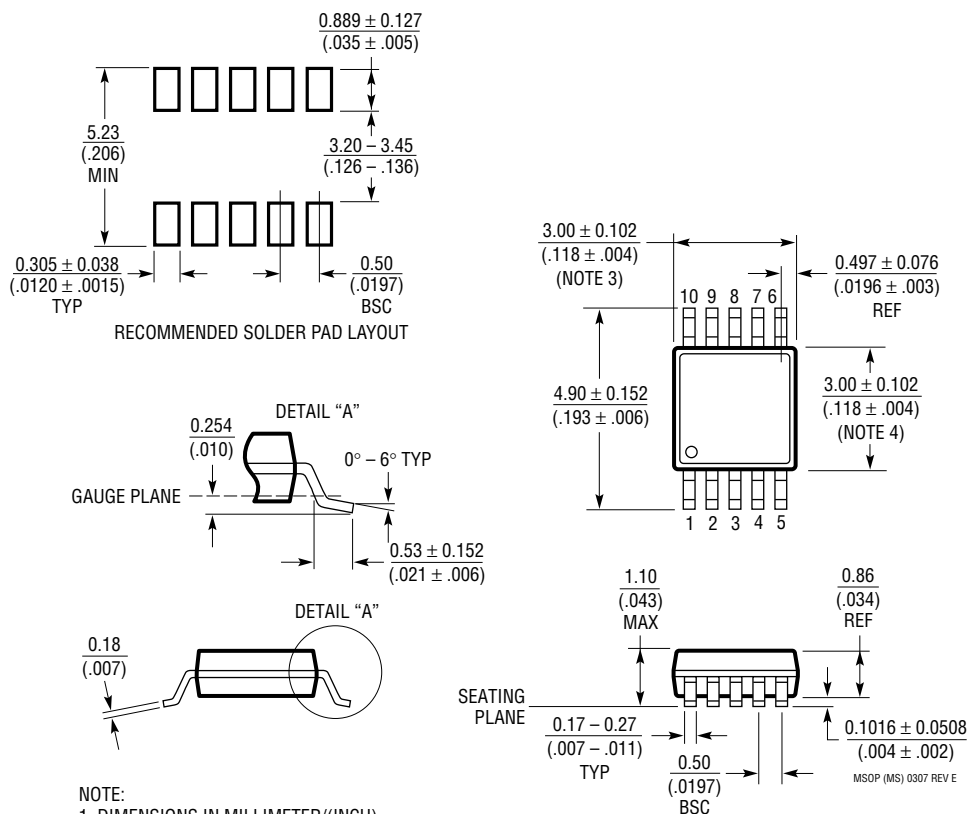
Overvoltage Regulator with Low Battery Detection and Output Keep Alive During Shutdown



[illegible]

PACKAGE DESCRIPTION

MS Package 10-Lead Plastic MSOP (Reference LTC DWG # 05-08-1661)

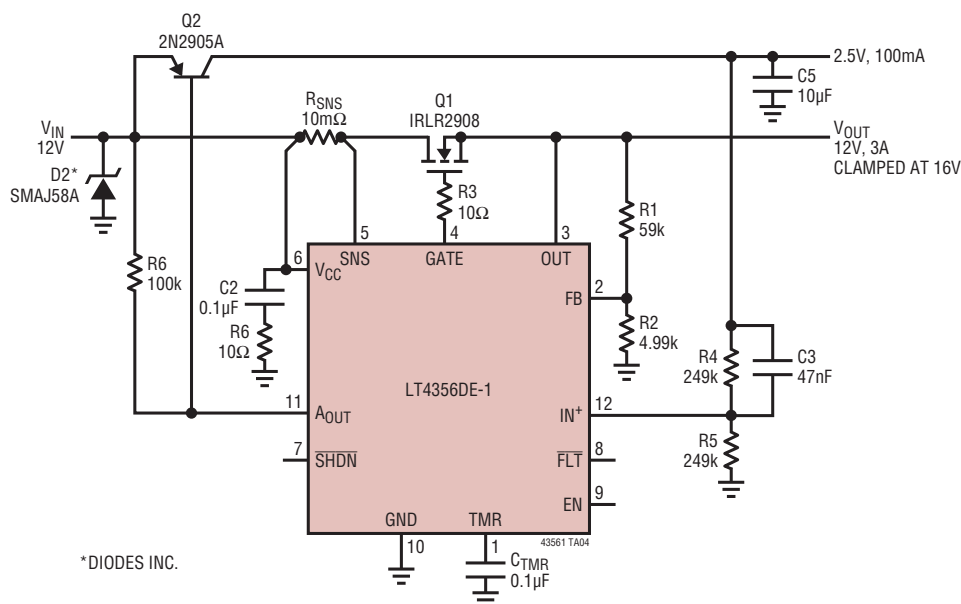


NOTE:

- DIMENSIONS IN MILLIMETER/(INCH)
- DRAWING NOT TO SCALE
- DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
- DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
- LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

Overvoltage Regulator with Linear Regulator Up to 100mA



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1641-1/LT1641-2	Positive High Voltage Hot Swap™ Controllers	Active Current Limiting, Supplies From 9V to 80V
LTC1696	Overvoltage Protection Controller	ThinSOT™ Package, 2.7V to 28V
LTC1735	High Efficiency Synchronous Step-Down Switching Regulator	Output Fault Protection, 16-Pin SSOP
LTC1778	No R _{SENSE} ™ Wide Input Range Synchronous Step-Down Controller	Up to 97% Efficiency, $4V \leq V_{IN} \leq 36V$, $0.8V \leq V_{OUT} \leq (0.9)(V_{IN})$, I _{OUT} Up to 20A
LTC2909	Triple/Dual Inputs UV/OV Negative Monitor	Pin Selectable Input Polarity Allows Negative and OV Monitoring
LTC2912/LTC2913	Single/Dual UV/OV Voltage Monitor	Ads UV and OV Trip Values, $\pm 1.5\%$ Threshold Accuracy
LTC2914	Quad UV/OV Monitor	For Positive and Negative Supplies
LTC3727/LTC3727-1	2-Phase, Dual, Synchronous Controller	$4V \leq V_{IN} \leq 36V$, $0.8V \leq V_{OUT} \leq 14V$
LTC3827/LTC3827-1	Low I _Q , Dual, Synchronous Controller	$4V \leq V_{IN} \leq 36V$, $0.8V \leq V_{OUT} \leq 10V$, 80μA Quiescent Current
LTC3835/LTC3835-1	Low I _Q , Synchronous Step-Down Controller	Single Channel LTC3827/LTC3827-1
LT3845	Low I _Q , Synchronous Step-Down Controller	$4V \leq V_{IN} \leq 60V$, $1.23V \leq V_{OUT} \leq 36V$, 120μA Quiescent Current
LT3850	Dual, 550kHz, 2-Phase Synchronous Step-Down Controller	Dual 180° Phased Controllers, V _{IN} 4V to 24V, 97% Duty Cycle, 4mm × 4mm QFN-28, SSOP-28 Packages
LT4256	Positive 48V Hot Swap Controller with Open-Circuit Detect	Foldback Current Limiting, Open-Circuit and Overcurrent Fault Output, Up to 80V Supply
LTC4260	Positive High Voltage Hot Swap Controller with ADC and I ² C	Wide Operating Range 8.5V to 80V
LT4351	Ideal MOSFET ORing Diode	External N-channel MOSFETs Replace ORing Diodes, 1.2V to 20V
LTC4354	Negative Voltage Diode-OR Controller	Controls Two N-Channel MOSFETs, 1μs Turn-Off, 80V Operation
LTC4355	Positive Voltage Diode-OR Controller	Controls Two N-Channel MOSFETs, 0.5μs Turn-Off, 80V Operation

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