Wide Input Range, No R_{SENSE}™ Current Mode Boost, Flyback and SEPIC Controller

FEATURES

- **High Efficiency (No Sense Resistor Required)**
- **Wide Input Voltage Range: 2.5V to 36V**
- **Current Mode Control Provides Excellent Transient Response**
- **High Maximum Duty Cycle (92% Typ)**
- **±2% RUN Pin Threshold with 100mV Hysteresis**
- **±1% Internal Voltage Reference**
- Micropower Shutdown: I_Q = 10µA
- Programmable Operating Frequency (50kHz to 1MHz) with One External Resistor
- Synchronizable to an External Clock Up to 1.3 × f_{OSC}
- User-Controlled Pulse Skip or Burst Mode® Operation
- Internal 5.2V Low Dropout Voltage Regulator
- Output Overvoltage Protection
- Capable of Operating with a Sense Resistor for High Output Voltage Applications
- Small 10-Lead MSOP Package

APPLICATIONS

- Telecom Power Supplies
- Portable Electronic Equipment

DESCRIPTION

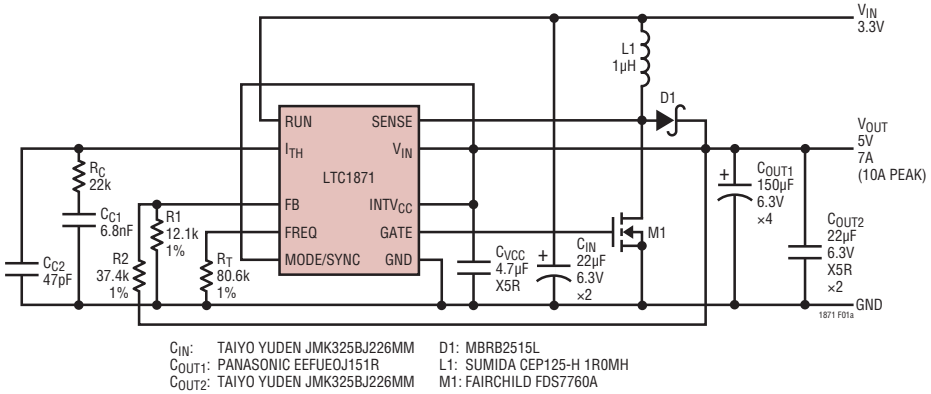
The LTC®1871 is a wide input range, current mode, boost, flyback or SEPIC controller that drives an N-channel power MOSFET and requires very few external components. Intended for low to medium power applications, it eliminates the need for a current sense resistor by utilizing the power MOSFET's on-resistance, thereby maximizing efficiency.

The IC's operating frequency can be set with an external resistor over a 50kHz to 1MHz range, and can be synchronized to an external clock using the MODE/SYNC pin. Burst Mode operation at light loads, a low minimum operating supply voltage of 2.5V and a low shutdown quiescent current of 10µA make the LTC1871 ideally suited for battery-operated systems.

For applications requiring constant frequency operation, Burst Mode operation can be defeated using the MODE/SYNC pin. Higher output voltage boost, SEPIC and flyback applications are possible with the LTC1871 by connecting the SENSE pin to a resistor in the source of the power MOSFET.

The LTC1871 is available in the 10-lead MSOP package.

TYPICAL APPLICATION



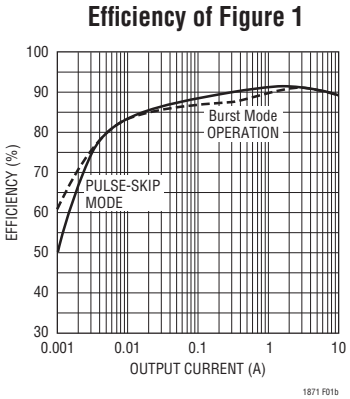


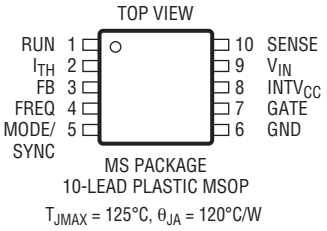
Figure 1. High Efficiency 3.3V Input, 5V Output Boost Converter (Bootstrapped)

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Voltage ..... –0.3V to 36V
$INTV_{CC}$ Voltage..... –0.3V to 7V
$INTV_{CC}$ Output Current..... 50mA
GATE Voltage ..... –0.3V to V_{INTVCC} + 0.3V
I_{TH}, FB Voltages ..... –0.3V to 2.7V
RUN, MODE/SYNC Voltages ..... –0.3V to 7V
FREQ Voltage ..... –0.3V to 1.5V
SENSE Pin Voltage..... –0.3V to 36V
Operating Temperature Range (Note 2)
LTC1871E.....–40°C to 85°C
LTC1871I.....–40°C to 125°C
LTC1871H .....–40°C to 150°C
Junction Temperature (Note 3)
LTC1871E/LTC1871I..... 125°C
LTC1871H .....150°C
Storage Temperature Range.....–65°C to 150°C
Lead Temperature (Soldering, 10 sec) .....300°C

PIN CONFIGURATION



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 120°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1871EMS#PBF	LTC1871EMS#TRPBF	LTSX	10-Lead Plastic MSOP	–40°C to 85°C
LTC1871IMS#PBF	LTC1871IMS#TRPBF	LTBFC	10-Lead Plastic MSOP	–40°C to 125°C
LTC1871HMS#PBF	LTC1871HMS#TRPBF	LTCXS	10-Lead Plastic MSOP	–40°C to 150°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC1871EMS	LTC1871EMS#TR	LTSX	10-Lead Plastic MSOP	–40°C to 85°C
LTC1871IMS	LTC1871IMS#TR	LTBFC	10-Lead Plastic MSOP	–40°C to 125°C
LTC1871HMS	LTC1871HMS#TR	LTCXS	10-Lead Plastic MSOP	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{INTVCC} = 5V, V_{RUN} = 1.5V, R_{FREQ} = 80k, $V_{MODE/SYNC}$ = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
$V_{IN(MIN)}$	Minimum Input Voltage			2.5			V
		I-Grade or H-Grade (Note 2)	●	2.5			V
I_Q	Input Voltage Supply Current	(Note 4)					
	Continuous Mode	$V_{MODE/SYNC}$ = 5V, V_{FB} = 1.4V, V_{ITH} = 0.75V			550	1000	µA
		$V_{MODE/SYNC}$ = 5V, V_{FB} = 1.4V, V_{ITH} = 0.75V, I-Grade or H-Grade (Note 2)	●		550	1000	µA
	Burst Mode Operation, No Load	$V_{MODE/SYNC}$ = 0V, V_{ITH} = 0.2V (Note 5)			250	500	µA
		$V_{MODE/SYNC}$ = 0V, V_{ITH} = 0.2V (Note 5), I-Grade or H-Grade (Note 2)	●		250	500	µA
	Shutdown Mode	V_{RUN} = 0V			10	20	µA
		V_{RUN} = 0V, I-Grade or H-Grade (Note 2)	●		10	20	µA
V_{RUN}^+	Rising RUN Input Threshold Voltage				1.348		V
V_{RUN}^-	Falling RUN Input Threshold Voltage		 ●	1.223 1.198	1.248	1.273 1.298	V V
		H-Grade (Note 2)	●	1.179		1.315	V
$V_{RUN(HYST)}$	RUN Pin Input Threshold Hysteresis			50	100	150	mV
		I-Grade (Note 2)	●	35	100	175	mV
		H-Grade (Note 2)	●	35		300	mV
I_{RUN}	RUN Input Current				1	60	nA
V_{FB}	Feedback Voltage	V_{ITH} = 0.2V (Note 5)	 ●	1.218 1.212	1.230	1.242 1.248	V V
		V_{ITH} = 0.2V (Note 5), I-Grade or H-Grade (Note 2)	●	1.205		1.255	V
I_{FB}	FB Pin Input Current	V_{ITH} = 0.2V (Note 5)			18	60	nA
$\frac{\Delta V_{FB}}{\Delta V_{IN}}$	Line Regulation	2.5V ≤ V_{IN} ≤ 30V			0.002	0.02	%/V
		2.5V ≤ V_{IN} ≤ 30V, I-Grade or H-Grade (Note 2)	●		0.002	0.02	%/V
$\frac{\Delta V_{FB}}{\Delta V_{ITH}}$	Load Regulation	$V_{MODE/SYNC}$ = 0V, V_{ITH} = 0.5V to 0.9V (Note 5)	●	–1	–0.1		%
		$V_{MODE/SYNC}$ = 0V, V_{ITH} = 0.5V to 0.9V (Note 5) I-Grade or H-Grade (Note 2)	●	–1	–0.1		%
$\Delta V_{FB(OV)}$	ΔFB Pin, Overvoltage Lockout	$V_{FB(OV)}$ – $V_{FB(NOM)}$ in Percent		2.5	6	10	%
g_m	Error Amplifier Transconductance	I_{TH} Pin Load = ±5µA (Note 5)			650		µmho
$V_{ITH(BURST)}$	Burst Mode Operation I_{TH} Pin Voltage	Falling I_{TH} Voltage (Note 5)			0.3		V
$V_{SENSE(MAX)}$	Maximum Current Sense Input Threshold	Duty Cycle < 20%		120	150	180	mV
		Duty Cycle < 20%, I-Grade or H-Grade (Note 2)	●	100		200	mV
$I_{SENSE(ON)}$	SENSE Pin Current (GATE High)	V_{SENSE} = 0V			35	50	µA
$I_{SENSE(OFF)}$	SENSE Pin Current (GATE Low)	V_{SENSE} = 30V			0.1	5	µA
Oscillator							
f_{OSC}	Oscillator Frequency	R_{FREQ} = 80k		250	300	350	kHz
		R_{FREQ} = 80k, I-Grade (Note 2)	●	250	300	350	kHz
		R_{FREQ} = 80k, H-Grade (Note 2)	●	240	300	360	kHz
	Oscillator Frequency Range			50		1000	kHz
		I-Grade or H-Grade (Note 2)	●	50		1000	kHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{INTVCC} = 5V, V_{RUN} = 1.5V, R_{FREQ} = 80k, $V_{MODE/SYNC}$ = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
D_{MAX}	Maximum Duty Cycle			87	92	97	%
		I-Grade or H-Grade (Note 2)	●	87	92	97	%
f_{SYNC}/f_{OSC}	Recommended Maximum Synchronized Frequency Ratio	f_{OSC} = 300kHz (Note 6)			1.25	1.30	
		f_{OSC} = 300kHz (Note 6), I-Grade or H-Grade (Note 2)	●		1.25	1.30	
$t_{SYNC(MIN)}$	MODE/SYNC Minimum Input Pulse Width	V_{SYNC} = 0V to 5V			25		ns
$t_{SYNC(MAX)}$	MODE/SYNC Maximum Input Pulse Width	V_{SYNC} = 0V to 5V			0.8/f_{OSC}		ns
$V_{IL(MODE)}$	Low Level MODE/SYNC Input Voltage					0.3	V
		I-Grade or H-Grade (Note 2)	●			0.3	V
$V_{IH(MODE)}$	High Level MODE/SYNC Input Voltage			1.2			V
		I-Grade or H-Grade (Note 2)	●	1.2			V
$R_{MODE/SYNC}$	MODE/SYNC Input Pull-Down Resistance				50		kΩ
V_{FREQ}	Nominal FREQ Pin Voltage				0.62		V
Low Dropout Regulator							
V_{INTVCC}	$INTV_{CC}$ Regulator Output Voltage	V_{IN} = 7.5V		5.0	5.2	5.4	V
		V_{IN} = 7.5V, I-Grade (Note 2)	●	5.0	5.2	5.4	V
		V_{IN} = 7.5V, H-Grade (Note 2)	●	4.95	5.2	5.45	V
$\frac{\Delta V_{INTVCC}}{\Delta V_{IN1}}$	$INTV_{CC}$ Regulator Line Regulation	7.5V ≤ V_{IN} ≤ 15V			8	25	mV
$\frac{\Delta V_{INTVCC}}{\Delta V_{IN2}}$	$INTV_{CC}$ Regulator Line Regulation	15V ≤ V_{IN} ≤ 30V			70	200	mV
$V_{LDO(LOAD)}$	$INTV_{CC}$ Load Regulation	0 ≤ I_{INTVCC} ≤ 20mA, V_{IN} = 7.5V		–2	–0.2		%
$V_{DROPOUT}$	$INTV_{CC}$ Regulator Dropout Voltage	V_{IN} = 5V, $INTV_{CC}$ Load = 20mA			280		mV
I_{INTVCC}	Bootstrap Mode $INTV_{CC}$ Supply Current in Shutdown	RUN = 0V, SENSE = 5V			10	20	µA
		I-Grade (Note 2)	●			30	µA
		H-Grade (Note 2)	●			50	µA
GATE Driver							
t_r	GATE Driver Output Rise Time	C_L = 3300pF (Note 7)			17	100	ns
t_f	GATE Driver Output Fall Time	C_L = 3300pF (Note 7)			8	100	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC1871E is guaranteed to meet performance specifications from 0°C to 85°C operating temperature. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC1871I is guaranteed over the full –40°C to 125°C operating temperature range and the LTC1871H is guaranteed over the full –40°C to 150°C operating temperature range.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$T_J = T_A + (P_D \bullet 110°C/W)$

Note 4: The dynamic input supply current is higher due to power MOSFET gate charging ($Q_G \bullet f_{OSC}$). See Applications Information.

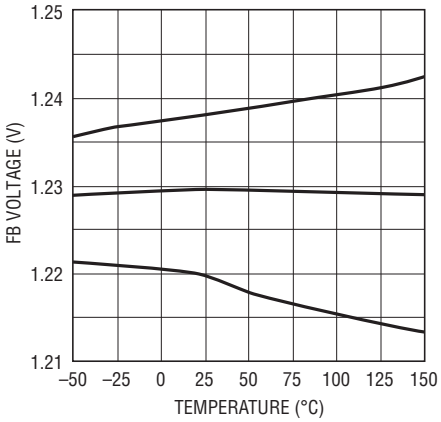
Note 5: The LTC1871 is tested in a feedback loop which servos V_{FB} to the reference voltage with the I_{TH} pin forced to the midpoint of its voltage range (0.3V ≤ V_{ITH} ≤ 1.2V, midpoint = 0.75V).

Note 6: In a synchronized application, the internal slope compensation gain is increased by 25%. Synchronizing to a significantly higher ratio will reduce the effective amount of slope compensation, which could result in subharmonic oscillation for duty cycles greater than 50%.

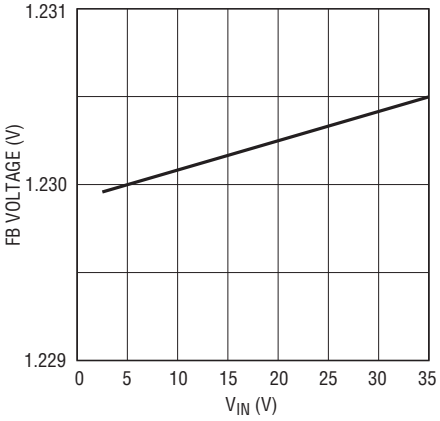
Note 7: Rise and fall times are measured at 10% and 90% levels.

TYPICAL PERFORMANCE CHARACTERISTICS

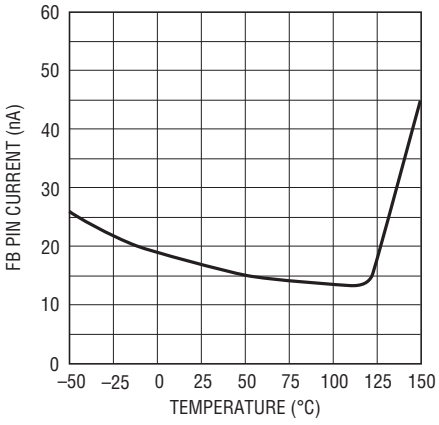
FB Voltage vs Temp



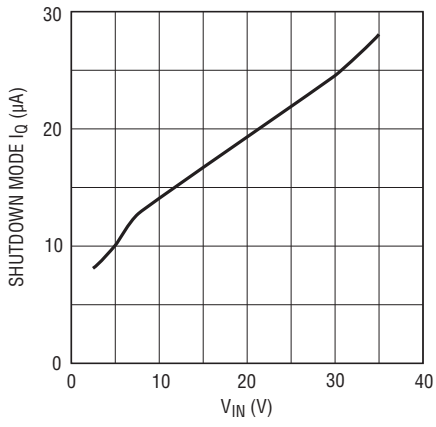
FB Voltage Line Regulation



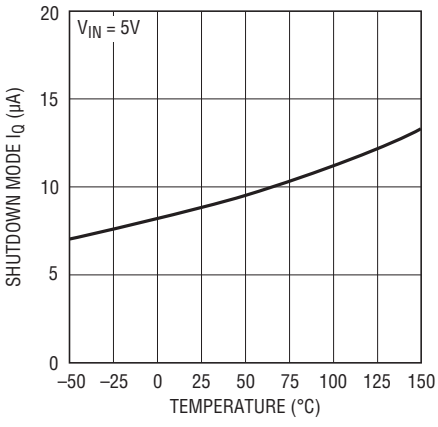
FB Pin Current vs Temperature



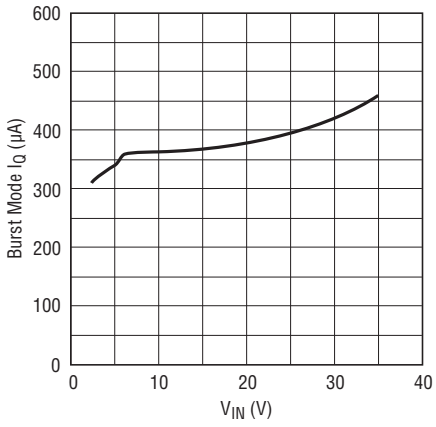
Shutdown Mode I_Q vs V_{IN}



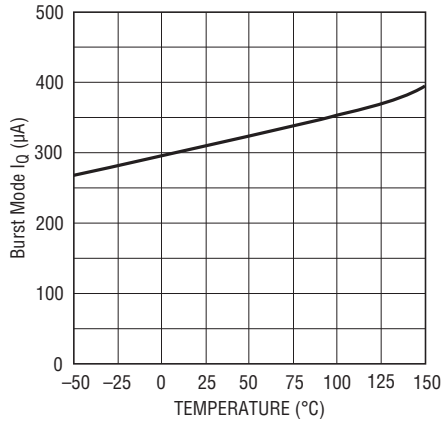
Shutdown Mode I_Q vs Temperature



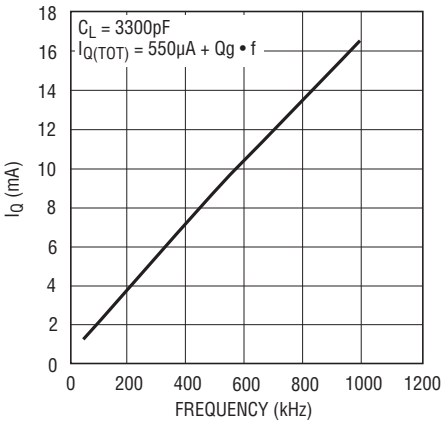
Burst Mode I_Q vs V_{IN}



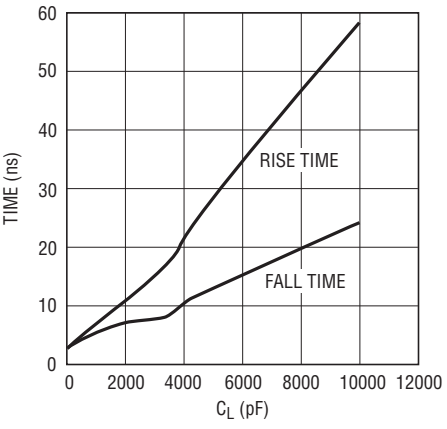
Burst Mode I_Q vs Temperature



Dynamic I_Q vs Frequency

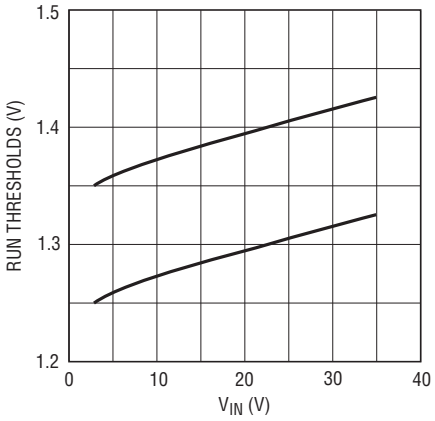


Gate Drive Rise and Fall Time vs C_L

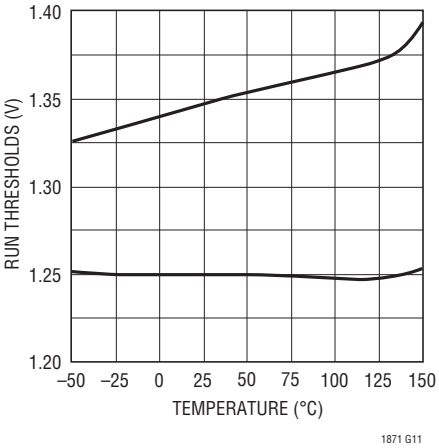


TYPICAL PERFORMANCE CHARACTERISTICS

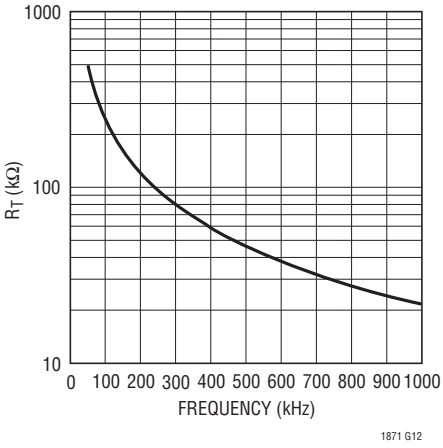
RUN Thresholds vs V_{IN}



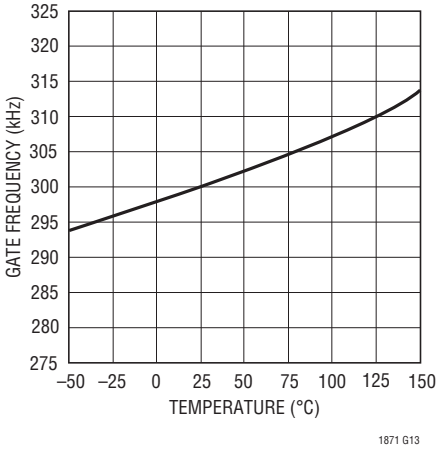
RUN Thresholds vs Temperature



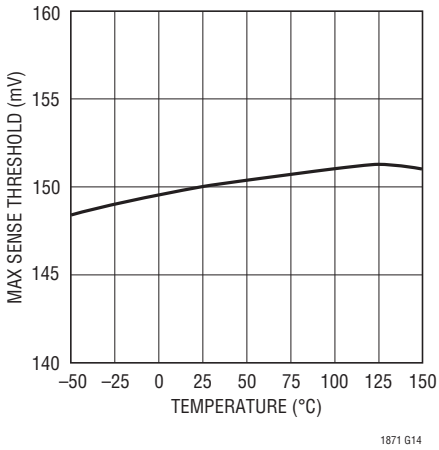
R_T vs Frequency



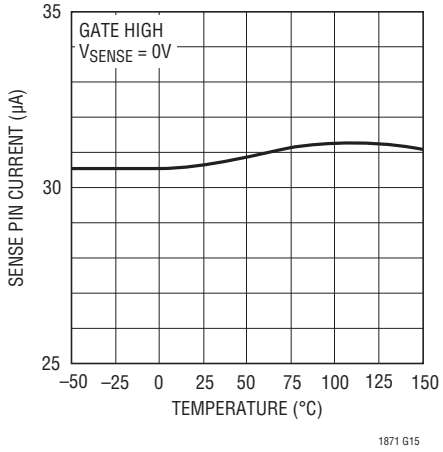
Frequency vs Temperature



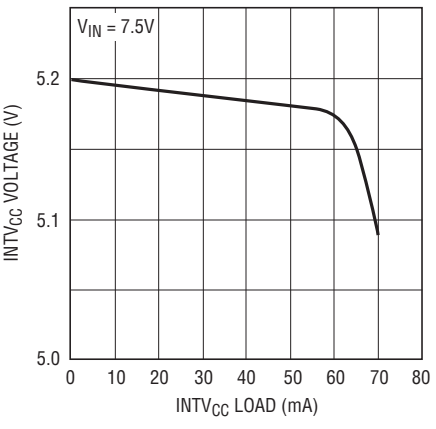
Maximum Sense Threshold vs Temperature



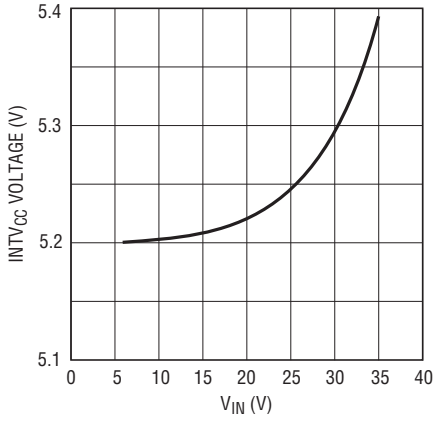
SENSE Pin Current vs Temperature



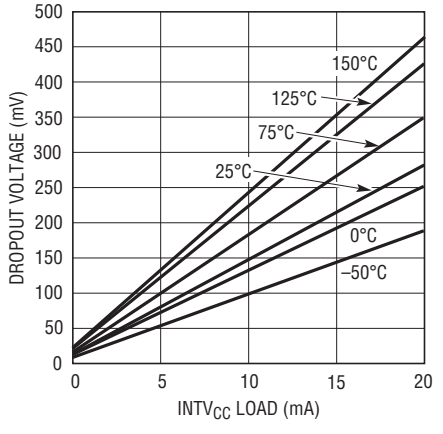
$INTV_{CC}$ Load Regulation



$INTV_{CC}$ Line Regulation



$INTV_{CC}$ Dropout Voltage vs Current, Temperature



PIN FUNCTIONS

RUN (Pin 1): The RUN pin provides the user with an accurate means for sensing the input voltage and programming the start-up threshold for the converter. The falling RUN pin threshold is nominally 1.248V and the comparator has 100mV of hysteresis for noise immunity. When the RUN pin is below this input threshold, the IC is shut down and the V_{IN} supply current is kept to a low value (typ 10µA). The Absolute Maximum Rating for the voltage on this pin is 7V.

I_{TH} (Pin 2): Error Amplifier Compensation Pin. The current comparator input threshold increases with this control voltage. Nominal voltage range for this pin is 0V to 1.40V.

FB (Pin 3): Receives the feedback voltage from the external resistor divider across the output. Nominal voltage for this pin in regulation is 1.230V.

FREQ (Pin 4): A resistor from the FREQ pin to ground programs the operating frequency of the chip. The nominal voltage at the FREQ pin is 0.6V.

MODE/SYNC (Pin 5): This input controls the operating mode of the converter and allows for synchronizing the operating frequency to an external clock. If the MODE/SYNC pin is connected to ground, Burst Mode operation is enabled. If the MODE/SYNC pin is connected to $INTV_{CC}$, or if an external logic-level synchronization signal is applied to this input, Burst Mode operation is disabled and the IC operates in a continuous mode.

GND (Pin 6): Ground Pin.

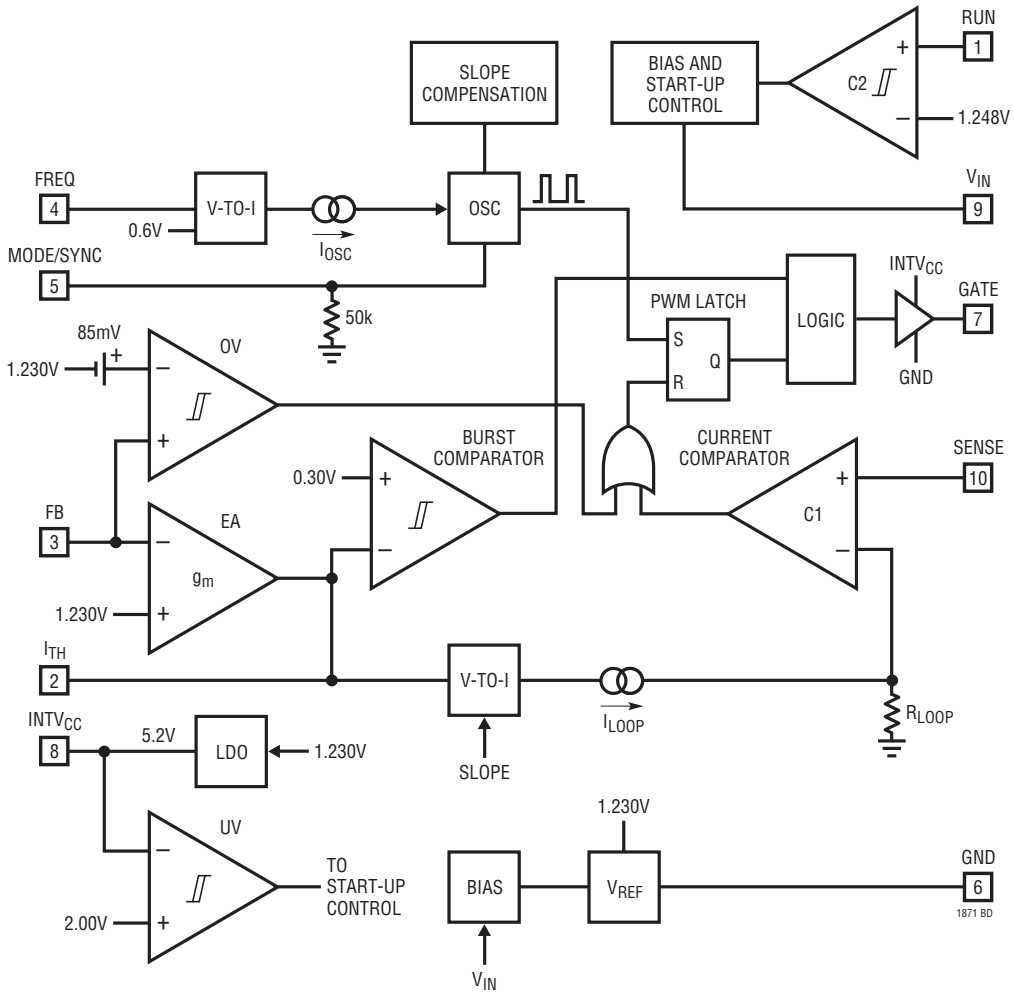
GATE (Pin 7): Gate Driver Output.

$INTV_{CC}$ (Pin 8): The Internal 5.20V Regulator Output. The gate driver and control circuits are powered from this voltage. Decouple this pin locally to the IC ground with a minimum of 4.7µF low ESR tantalum or ceramic capacitor.

V_{IN} (Pin 9): Main Supply Pin. Must be closely decoupled to ground.

SENSE (Pin 10): The Current Sense Input for the Control Loop. Connect this pin to the drain of the power MOSFET for V_{DS} sensing and highest efficiency. Alternatively, the SENSE pin may be connected to a resistor in the source of the power MOSFET. Internal leading edge blanking is provided for both sensing methods.

BLOCK DIAGRAM



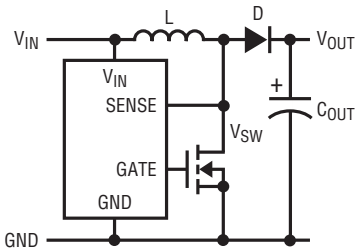
OPERATION

Main Control Loop

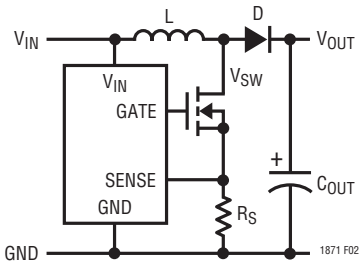
The LTC1871 is a constant frequency, current mode controller for DC/DC boost, SEPIC and flyback converter applications. The LTC1871 is distinguished from conventional current mode controllers because the current control loop can be closed by sensing the voltage drop across the power MOSFET switch instead of across a discrete sense resistor, as shown in Figure 2. This sensing technique improves efficiency, increases power density, and reduces the cost of the overall solution.

For circuit operation, please refer to the Block Diagram of the IC and Figure 1. In normal operation, the power MOSFET is turned on when the oscillator sets the PWM latch and is turned off when the current comparator C1 resets the latch. The divided-down output voltage is compared to an internal 1.230V reference by the error amplifier EA, which outputs an error signal at the I_{TH} pin. The voltage on the I_{TH} pin sets the current comparator C1 input threshold. When the load current increases, a fall in the FB voltage relative to the reference voltage causes the I_{TH} pin to rise, which causes the current comparator C1 to trip at a higher peak inductor current value. The average inductor current will therefore rise until it equals the load current, thereby maintaining output regulation.

OPERATION



2a. SENSE Pin Connection for Maximum Efficiency (V_{SW} < 36V)



2b. SENSE Pin Connection for Precise Control of Peak Current or for V_{SW} > 36V

Figure 2. Using the SENSE Pin On the LTC1871

The nominal operating frequency of the LTC1871 is programmed using a resistor from the FREQ pin to ground and can be controlled over a 50kHz to 1000kHz range. In addition, the internal oscillator can be synchronized to an external clock applied to the MODE/SYNC pin and can be locked to a frequency between 100% and 130% of its nominal value. When the MODE/SYNC pin is left open, it is pulled low by an internal 50k resistor and Burst Mode operation is enabled. If this pin is taken above 2V or an external clock is applied, Burst Mode operation is disabled and the IC operates in continuous mode. With no load (or an extremely light load), the controller will skip pulses in order to maintain regulation and prevent excessive output ripple.

The RUN pin controls whether the IC is enabled or is in a low current shutdown state. A micropower 1.248V reference and comparator C2 allow the user to program the supply voltage at which the IC turns on and off (comparator C2 has 100mV of hysteresis for noise immunity). With the RUN pin below 1.248V, the chip is off and the input supply current is typically only 10µA.

An overvoltage comparator OV senses when the FB pin exceeds the reference voltage by 6.5% and provides a reset pulse to the main RS latch. Because this RS latch is reset-dominant, the power MOSFET is actively held off for the duration of an output overvoltage condition.

The LTC1871 can be used either by sensing the voltage drop across the power MOSFET or by connecting the SENSE pin to a conventional shunt resistor in the source of the power MOSFET, as shown in Figure 2. Sensing the voltage across the power MOSFET maximizes converter efficiency and minimizes the component count, but limits the output voltage to the maximum rating for this pin (36V). By connecting the SENSE pin to a resistor in the source of the power MOSFET, the user is able to program output voltages significantly greater than 36V.

Programming the Operating Mode

For applications where maximizing the efficiency at very light loads (e.g., <100µA) is a high priority, the current in the output divider could be decreased to a few microamps and Burst Mode operation should be applied (i.e., the MODE/SYNC pin should be connected to ground). In applications where fixed frequency operation is more critical than low current efficiency, or where the lowest output ripple is desired, pulse-skip mode operation should be used and the MODE/SYNC pin should be connected to the $INTV_{CC}$ pin. This allows discontinuous conduction mode (DCM) operation down to near the limit defined by the chip's minimum on-time (about 175ns). Below this output current level, the converter will begin to skip cycles in order to maintain output regulation. Figures 3 and 4 show the light load switching waveforms for Burst Mode and pulse-skip mode operation for the converter in Figure 1.

Burst Mode Operation

Burst Mode operation is selected by leaving the MODE/SYNC pin unconnected or by connecting it to ground. In normal operation, the range on the I_{TH} pin corresponding to no load to full load is 0.30V to 1.2V. In Burst Mode operation, if the error amplifier EA drives the I_{TH} voltage below 0.525V, the buffered I_{TH} input to the current comparator C1 will be clamped at 0.525V (which corresponds to 25% of maximum load current). The inductor current peak is then held at approximately 30mV divided by the power

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MOSFET $R_{DS(ON)}$. If the I_{TH} pin drops below 0.30V, the Burst Mode comparator B1 will turn off the power MOSFET and scale back the quiescent current of the IC to 250µA (sleep mode). In this condition, the load current will be supplied by the output capacitor until the I_{TH} voltage rises above the 50mV hysteresis of the burst comparator. At light loads, short bursts of switching (where the average inductor current is 20% of its maximum value) followed by long periods of sleep will be observed, thereby greatly improving converter efficiency. Oscilloscope waveforms illustrating Burst Mode operation are shown in Figure 3.

Pulse-Skip Mode Operation

With the MODE/SYNC pin tied to a DC voltage above 2V, Burst Mode operation is disabled. The internal, 0.525V buffered I_{TH} burst clamp is removed, allowing the I_{TH} pin to directly control the current comparator from no load to full load. With no load, the I_{TH} pin is driven below 0.30V, the power MOSFET is turned off and sleep mode is invoked. Oscilloscope waveforms illustrating this mode of operation are shown in Figure 4.

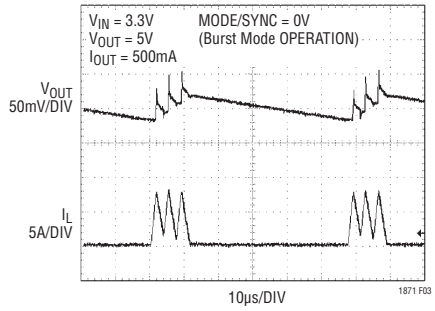

Figure 3. LTC1871 Burst Mode Operation (MODE/SYNC = 0V) at Low Output Current

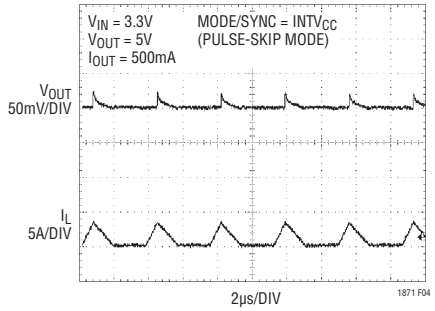

Figure 4. LTC1871 Low Output Current Operation with Burst Mode Operation Disabled (MODE/SYNC = $INTV_{CC}$)

When an external clock signal drives the MODE/SYNC pin at a rate faster than the chip's internal oscillator, the oscillator will synchronize to it. In this synchronized mode, Burst Mode operation is disabled. The constant frequency associated with synchronized operation provides a more controlled noise spectrum from the converter, at the expense of overall system efficiency of light loads.

When the oscillator's internal logic circuitry detects a synchronizing signal on the MODE/SYNC pin, the internal oscillator ramp is terminated early and the slope compensation is increased by approximately 30%. As a result, in applications requiring synchronization, it is recommended that the nominal operating frequency of the IC be programmed to be about 75% of the external clock frequency. Attempting to synchronize to too high an external frequency (above $1.3f_O$) can result in inadequate slope compensation and possible subharmonic oscillation (or jitter).

The external clock signal must exceed 2V for at least 25ns, and should have a maximum duty cycle of 80%, as shown in Figure 5. The MOSFET turn on will synchronize to the rising edge of the external clock signal.

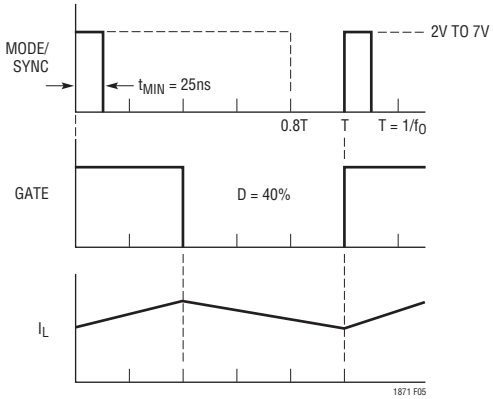

Figure 5. MODE/SYNC Clock Input and Switching Waveforms for Synchronized Operation

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Programming the Operating Frequency

The choice of operating frequency and inductor value is a tradeoff between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET and diode switching losses. However, lower frequency operation requires more inductance for a given amount of load current.

The LTC1871 uses a constant frequency architecture that can be programmed over a 50kHz to 1000kHz range with a single external resistor from the FREQ pin to ground, as shown in Figure 1. The nominal voltage on the FREQ pin is 0.6V, and the current that flows into the FREQ pin is used to charge and discharge an internal oscillator capacitor. A graph for selecting the value of R_T for a given operating frequency is shown in Figure 6.

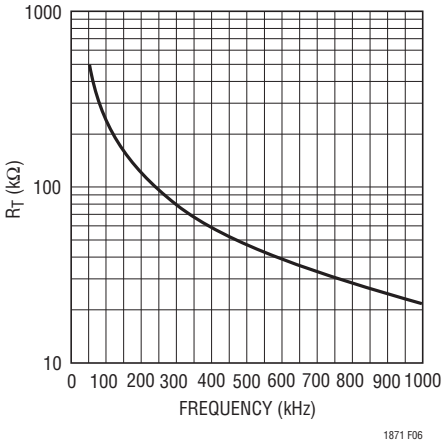

Figure 6. Timing Resistor (R_T) Value

$INTV_{CC}$ Regulator Bypassing and Operation

An internal, P-channel low dropout voltage regulator produces the 5.2V supply which powers the gate driver and logic circuitry within the LTC1871, as shown in Figure 7. The $INTV_{CC}$ regulator can supply up to 50mA and must be bypassed to ground immediately adjacent to the IC pins with a minimum of 4.7µF tantalum or ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate driver.

For input voltages that don't exceed 7V (the absolute maximum rating for this pin), the internal low dropout regulator in the LTC1871 is redundant and the $INTV_{CC}$ pin can be shorted directly to the V_{IN} pin. With the $INTV_{CC}$ pin shorted to V_{IN}, however, the divider that programs the regulated $INTV_{CC}$ voltage will draw 10µA of current from the input supply, even in shutdown mode. For applications that require the lowest shutdown mode input supply current, do not connect the $INTV_{CC}$ pin to V_{IN}. Regardless of whether the $INTV_{CC}$ pin is shorted to V_{IN} or not, **it is always necessary to have the driver circuitry bypassed with a 4.7µF tantalum or low ESR ceramic capacitor to ground immediately adjacent to the $INTV_{CC}$ and GND pins.**

In an actual application, most of the IC supply current is used to drive the gate capacitance of the power MOSFET. As a result, high input voltage applications in which a large power MOSFET is being driven at high frequencies can cause the LTC1871 to exceed its maximum junction

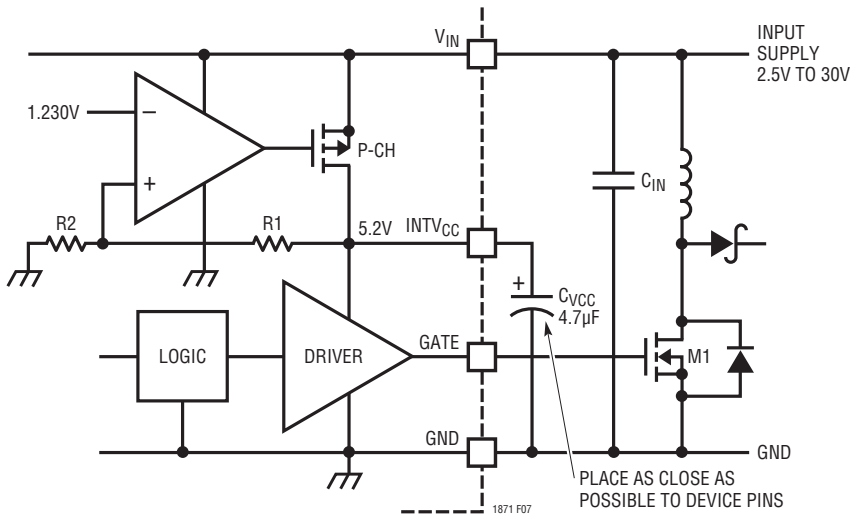

Figure 7. Bypassing the LDO Regulator and Gate Driver Supply

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temperature rating. The junction temperature can be estimated using the following equations:

$I_{Q(TOT)} \approx I_Q + f \bullet Q_G$

$P_{IC} = V_{IN} \bullet (I_Q + f \bullet Q_G)$

$T_J = T_A + P_{IC} \bullet R_{TH(JA)}$

The total quiescent current $I_{Q(TOT)}$ consists of the static supply current (I_Q) and the current required to charge and discharge the gate of the power MOSFET. The 10-pin MSOP package has a thermal resistance of $R_{TH(JA)} = 120°C/W$.

As an example, consider a power supply with $V_{IN} = 5V$ and $V_O = 12V$ at $I_O = 1A$. The switching frequency is 500kHz, and the maximum ambient temperature is 70°C. The power MOSFET chosen is the IRF7805, which has a maximum $R_{DS(ON)}$ of 11mΩ (at room temperature) and a maximum total gate charge of 37nC (the temperature coefficient of the gate charge is low).

$I_{Q(TOT)} = 600\mu A + 37nC \bullet 500kHz = 19.1mA$

$P_{IC} = 5V \bullet 19.1mA = 95mW$

$T_J = 70°C + 120°C/W \bullet 95mW = 81.4°C$

This demonstrates how significant the gate charge current can be when compared to the static quiescent current in the IC.

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked when operating in a continuous mode at high V_{IN}. A tradeoff between the operating frequency and the size of the power MOSFET may need to be made in order to maintain a reliable IC junction temperature. Prior to lowering the operating frequency, however, be sure to check with power MOSFET manufacturers for their latest-and-greatest low Q_G, low $R_{DS(ON)}$ devices. Power MOSFET manufacturing technologies are continually improving, with newer and better performance devices being introduced almost yearly.

Output Voltage Programming

The output voltage is set by a resistor divider according to the following formula:

$$V_O = 1.230V \bullet \left(1 + \frac{R2}{R1}\right)$$

The external resistor divider is connected to the output as shown in Figure 1, allowing remote voltage sensing. The resistors R1 and R2 are typically chosen so that the error caused by the current flowing into the FB pin during normal operation is less than 1% (this translates to a maximum value of R1 of about 250k).

Programming Turn-On and Turn-Off Thresholds with the RUN Pin

The LTC1871 contains an independent, micropower voltage reference and comparator detection circuit that remains active even when the device is shut down, as shown in Figure 8. This allows users to accurately program an input voltage at which the converter will turn on and off. The falling threshold voltage on the RUN pin is equal to the internal reference voltage of 1.248V. The comparator has 100mV of hysteresis to increase noise immunity.

The turn-on and turn-off input voltage thresholds are programmed using a resistor divider according to the following formulas:

$$V_{IN(OFF)} = 1.248V \bullet \left(1 + \frac{R2}{R1}\right)$$

$$V_{IN(ON)} = 1.348V \bullet \left(1 + \frac{R2}{R1}\right)$$

The resistor R1 is typically chosen to be less than 1M.

For applications where the RUN pin is only to be used as a logic input, the user should be aware of the 7V Absolute Maximum Rating for this pin! The RUN pin can be connected to the input voltage through an external 1M resistor, as shown in Figure 8c, for "always on" operation.

Application Circuits

A basic LTC1871 application circuit is shown in Figure 1. External component selection is driven by the characteristics of the load and the input supply. The first topology to be analyzed will be the boost converter, followed by SEPIC (single ended primary inductance converter).

APPLICATIONS INFORMATION

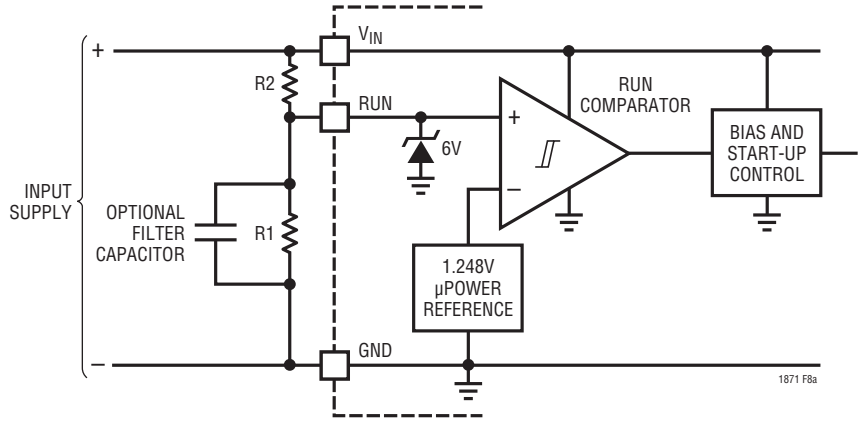

Figure 8a. Programming the Turn-On and Turn-Off Thresholds Using the RUN Pin

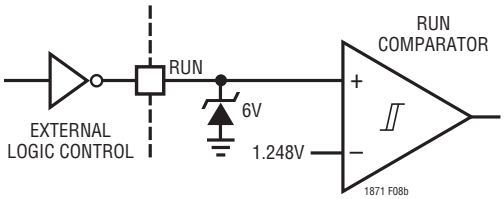

Figure 8b. On/Off Control Using External Logic

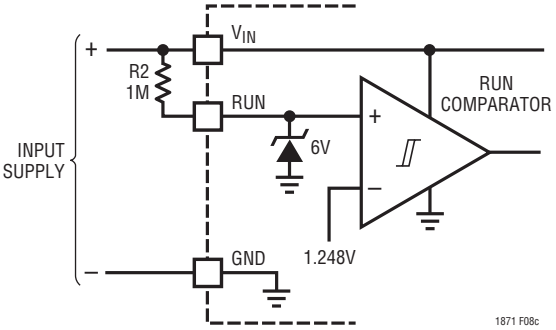

Figure 8c. External Pull-Up Resistor On RUN Pin for "Always On" Operation

Boost Converter: Duty Cycle Considerations

For a boost converter operating in a continuous conduction mode (CCM), the duty cycle of the main switch is:

$$D = \left(\frac{V_O + V_D - V_{IN}}{V_O + V_D} \right)$$

where V_D is the forward voltage of the boost diode. For converters where the input voltage is close to the output voltage, the duty cycle is low and for converters that develop a high output voltage from a low voltage input supply, the duty cycle is high. The maximum output voltage for a boost converter operating in CCM is:

$$V_{O(MAX)} = \frac{V_{IN(MIN)}}{(1 - D_{MAX})} - V_D$$

The maximum duty cycle capability of the LTC1871 is typically 92%. This allows the user to obtain high output voltages from low input supply voltages.

Boost Converter: The Peak and Average Input Currents

The control circuit in the LTC1871 is measuring the input current (either by using the $R_{DS(ON)}$ of the power MOSFET or by using a sense resistor in the MOSFET source), so the output current needs to be reflected back to the input in order to dimension the power MOSFET properly. Based on the fact that, ideally, the output power is equal to the input power, the maximum average input current is:

$$I_{IN(MAX)} = \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

The peak input current is:

$$I_{IN(PEAK)} = \left(1 + \frac{\chi}{2} \right) \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

The maximum duty cycle, D_{MAX}, should be calculated at minimum V_{IN}.

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Boost Converter: Ripple Current ΔI_L and the 'χ' Factor

The constant 'χ' in the equation above represents the percentage peak-to-peak ripple current in the inductor, relative to its maximum value. For example, if 30% ripple current is chosen, then χ = 0.30, and the peak current is 15% greater than the average.

For a current mode boost regulator operating in CCM, slope compensation must be added for duty cycles above 50% in order to avoid subharmonic oscillation. For the LTC1871, this ramp compensation is internal. Having an internally fixed ramp compensation waveform, however, does place some constraints on the value of the inductor and the operating frequency. If too large an inductor is used, the resulting current ramp (ΔI_L) will be small relative to the internal ramp compensation (at duty cycles above 50%), and the converter operation will approach voltage mode (ramp compensation reduces the gain of the current loop). If too small an inductor is used, but the converter is still operating in CCM (near critical conduction mode), the internal ramp compensation may be inadequate to prevent subharmonic oscillation. To ensure good current mode gain and avoid subharmonic oscillation, it is recommended that the ripple current in the inductor fall in the range of 20% to 40% of the maximum average current. For example, if the maximum average input current is 1A, choose a ΔI_L between 0.2A and 0.4A, and a value 'χ' between 0.2 and 0.4.

Boost Converter: Inductor Selection

Given an operating input voltage range, and having chosen the operating frequency and ripple current in the inductor, the inductor value can be determined using the following equation:

$$L = \frac{V_{IN(MIN)}}{\Delta I_L \bullet f} \bullet D_{MAX}$$

where:

$$\Delta I_L = \chi \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

Remember that boost converters are **not** short-circuit protected. Under a shorted output condition, the inductor current is limited only by the input supply capability. For applications requiring a step-up converter that is short-circuit protected, please refer to the applications section covering SEPIC converters.

The minimum required saturation current of the inductor can be expressed as a function of the duty cycle and the load current, as follows:

$$I_{L(SAT)} \geq \left(1 + \frac{\chi}{2}\right) \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

The saturation current rating for the inductor should be checked at the minimum input voltage (which results in the highest inductor current) and maximum output current.

Boost Converter: Operating in Discontinuous Mode

Discontinuous mode operation occurs when the load current is low enough to allow the inductor current to run out during the off-time of the switch, as shown in Figure 9. Once the inductor current is near zero, the switch and diode capacitances resonate with the inductance to form damped ringing at 1MHz to 10MHz. If the off-time is long enough, the drain voltage will settle to the input voltage.

Depending on the input voltage and the residual energy in the inductor, this ringing can cause the drain of the power MOSFET to go below ground where it is clamped by the body diode. This ringing is not harmful to the IC and it has not been shown to contribute significantly to EMI. Any attempt to damp it with a snubber will degrade the efficiency.

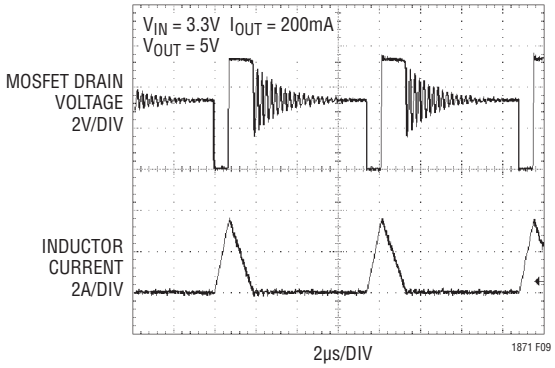

Figure 9. Discontinuous Mode Waveforms

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Boost Converter: Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore, copper losses will increase. Generally, there is a tradeoff between core losses and copper losses that needs to be balanced.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper losses and preventing saturation. Ferrite core material saturates "hard," meaning that the inductance collapses rapidly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequently, output voltage ripple. **Do not allow the core to saturate!**

Molypermalloy (from Magnetics, Inc.) is a very good, low cost core material for toroids, but is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ.

Boost Converter: Power MOSFET Selection

The power MOSFET serves two purposes in the LTC1871: it represents the main switching element in the power path, and its $R_{DS(ON)}$ represents the current sensing element for the control loop. Important parameters for the power MOSFET include the drain-to-source breakdown voltage (BV_{DSS}), the threshold voltage ($V_{GS(TH)}$), the on-resistance ($R_{DS(ON)}$) versus gate-to-source voltage, the gate-to-source and gate-to-drain charges (Q_{GS} and Q_{GD}, respectively), the maximum drain current ($I_{D(MAX)}$) and the MOSFET's thermal resistances ($R_{TH(JC)}$ and $R_{TH(JA)}$).

The gate drive voltage is set by the 5.2V $INTV_{CC}$ low drop regulator. Consequently, logic-level threshold MOSFETs should be used in most LTC1871 applications. If low input voltage operation is expected (e.g., supplying power from a lithium-ion battery or a 3.3V logic supply), then sublogic-level threshold MOSFETs should be used.

Pay close attention to the BV_{DSS} specifications for the MOSFETs relative to the maximum actual switch voltage in the application. Many logic-level devices are limited to 30V or less, and the switch node can ring during the turn-off of the MOSFET due to layout parasitics. Check the switching waveforms of the MOSFET directly across the drain and source terminals using the actual PC board layout (not just on a lab breadboard!) for excessive ringing.

During the switch on-time, the control circuit limits the maximum voltage drop across the power MOSFET to about 150mV (at low duty cycle). The peak inductor current is therefore limited to $150mV/R_{DS(ON)}$. The relationship between the maximum load current, duty cycle and the $R_{DS(ON)}$ of the power MOSFET is:

$$R_{DS(ON)} \leq V_{SENSE(MAX)} \bullet \frac{1-D_{MAX}}{\left(1+\frac{\chi}{2}\right) \bullet I_{O(MAX)} \bullet \rho_T}$$

The $V_{SENSE(MAX)}$ term is typically 150mV at low duty cycle, and is reduced to about 100mV at a duty cycle of 92% due to slope compensation, as shown in Figure 10. The ρ_T term accounts for the temperature coefficient of the $R_{DS(ON)}$ of the MOSFET, which is typically 0.4%/°C. Figure 11 illustrates the variation of normalized $R_{DS(ON)}$ over temperature for a typical power MOSFET.

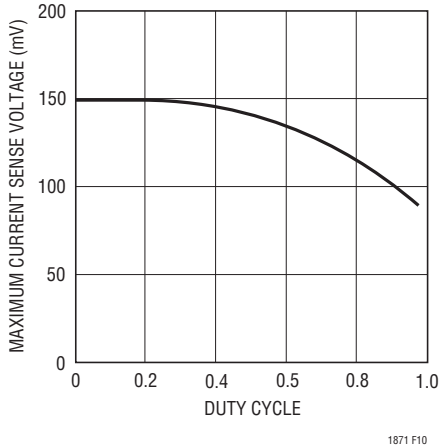

Figure 10. Maximum SENSE Threshold Voltage vs Duty Cycle

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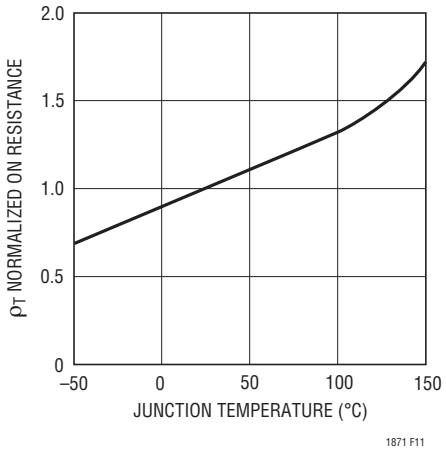

Figure 11. Normalized $R_{DS(ON)}$ vs Temperature

Another method of choosing which power MOSFET to use is to check what the maximum output current is for a given $R_{DS(ON)}$, since MOSFET on-resistances are available in discrete values.

$$I_{O(MAX)} = V_{SENSE(MAX)} \bullet \frac{1-D_{MAX}}{\left(1+\frac{\chi}{2}\right) \bullet R_{DS(ON)} \bullet \rho_T}$$

It is worth noting that the $1 – D_{MAX}$ relationship between $I_{O(MAX)}$ and $R_{DS(ON)}$ can cause boost converters with a wide input range to experience a dramatic range of maximum input and output current. This should be taken into consideration in applications where it is important to limit the maximum current drawn from the input supply.

Calculating Power MOSFET Switching and Conduction Losses and Junction Temperatures

In order to calculate the junction temperature of the power MOSFET, the power dissipated by the device must be known. This power dissipation is a function of the duty cycle, the load current and the junction temperature itself (due to the positive temperature coefficient of its $R_{DS(ON)}$). As a result, some iterative calculation is normally required to determine a reasonably accurate value. Since the controller is using the MOSFET as both a switching and a sensing element, care should be taken to ensure that the converter is capable of delivering the required load current over all operating conditions (line voltage and temperature), and for the worst-case specifications for $V_{SENSE(MAX)}$ and the $R_{DS(ON)}$ of the MOSFET listed in the manufacturer's data sheet.

The power dissipated by the MOSFET in a boost converter is:

$$P_{FET} = \left(\frac{I_{O(MAX)}}{1-D_{MAX}}\right)^2 \bullet R_{DS(ON)} \bullet D_{MAX} \bullet \rho_T + k \bullet V_O^{1.85} \bullet \frac{I_{O(MAX)}}{\left(1-D_{MAX}\right)} \bullet C_{RSS} \bullet f$$

The first term in the equation above represents the I^2R losses in the device, and the second term, the switching losses. The constant, $k = 1.7$, is an empirical factor inversely related to the gate drive current and has the dimension of 1/current.

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P_{FET} \bullet R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in this equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the case to the ambient temperature ($R_{TH(CA)}$). This value of T_J can then be compared to the original, assumed value used in the iterative calculation process.

Boost Converter: Output Diode Selection

To maximize efficiency, a fast switching diode with low forward drop and low reverse leakage is desired. The output diode in a boost converter conducts current during the switch off-time. The peak reverse voltage that the diode must withstand is equal to the regulator output voltage. The average forward current in normal operation is equal to the output current, and the peak current is equal to the peak inductor current.

$$I_{D(PEAK)} = I_{L(PEAK)} = \left(1+\frac{\chi}{2}\right) \bullet \frac{I_{O(MAX)}}{1-D_{MAX}}$$

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \bullet V_D$$

and the diode junction temperature is:

$$T_J = T_A + P_D \bullet R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in this equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the board to the ambient temperature in the enclosure.

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Remember to keep the diode lead lengths short and to observe proper switch-node layout (see Board Layout Checklist) to avoid excessive ringing and increased dissipation.

Boost Converter: Output Capacitor Selection

Contributions of ESR (equivalent series resistance), ESL (equivalent series inductance) and the bulk capacitance must be considered when choosing the correct component for a given output ripple voltage. The effects of these three parameters (ESR, ESL and bulk C) on the output voltage ripple waveform are illustrated in Figure 12e for a typical boost converter.

The choice of component(s) begins with the maximum acceptable ripple voltage (expressed as a percentage of the output voltage), and how this ripple should be divided between the ESR step and the charging/discharging ΔV. For the purpose of simplicity we will choose 2% for the maximum output ripple, to be divided equally between the ESR step and the charging/discharging ΔV. This percentage ripple will change, depending on the requirements of the application, and the equations provided below can easily be modified.

For a 1% contribution to the total ripple voltage, the ESR of the output capacitor can be determined using the following equation:

$$ESR_{COUT} \leq \frac{0.01 \bullet V_O}{I_{IN(PEAK)}}$$

where:

$$I_{IN(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

For the bulk C component, which also contributes 1% to the total ripple:

$$C_{OUT} \geq \frac{I_{O(MAX)}}{0.01 \bullet V_O \bullet f}$$

For many designs it is possible to choose a single capacitor type that satisfies both the ESR and bulk C requirements for the design. In certain demanding applications, however, the ripple voltage can be improved significantly by connecting two or more types of capacitors in parallel. For example, using a low ESR ceramic capacitor can minimize the ESR step, while an electrolytic capacitor can be used to supply the required bulk C.

Once the output capacitor ESR and bulk capacitance have been determined, the overall ripple voltage waveform should be verified on a dedicated PC board (see Board Layout section for more information on component placement). Lab breadboards generally suffer from excessive series inductance (due to inter-component wiring), and these parasitics can make the switching waveforms look significantly worse than they would be on a properly designed PC board.

The output capacitor in a boost regulator experiences high RMS ripple currents, as shown in Figure 12. The RMS output capacitor ripple current is:

$$I_{RMS(COUT)} \approx I_{O(MAX)} \bullet \sqrt{\frac{V_O - V_{IN(MIN)}}{V_{IN(MIN)}}}$$

Note that the ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be placed in parallel to meet size or height requirements in the design.

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest product of ESR and size of any aluminum electrolytic, at a somewhat higher price.

In surface mount applications, multiple capacitors may have to be placed in parallel in order to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount packages. In the case of tantalum, it is critical that the capacitors have been surge tested for use in switching power supplies. An excellent choice is AVX TPS series of surface mount tantalum. Also, ceramic capacitors are now available with extremely low ESR, ESL and high ripple current ratings.

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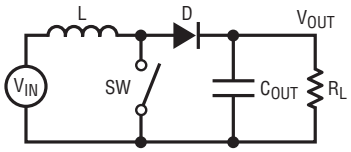
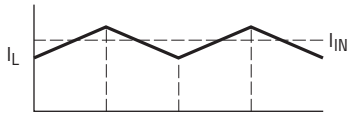
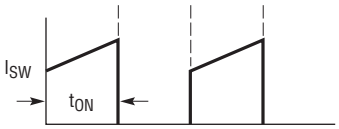


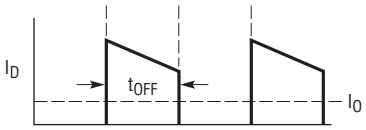
12a. Circuit Diagram



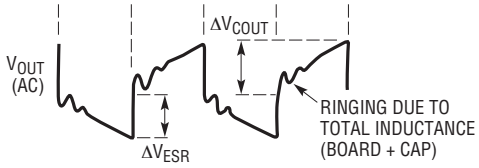
12b. Inductor and Input Currents



12c. Switch Current



12d. Diode and Output Currents



12e. Output Voltage Ripple Waveform

Figure 12. Switching Waveforms for a Boost Converter

Boost Converter: Input Capacitor Selection

The input capacitor of a boost converter is less critical than the output capacitor, due to the fact that the inductor is in series with the input and the input current waveform is continuous (see Figure 12b). The input voltage source impedance determines the size of the input capacitor, which is typically in the range of 10µF to 100µF. A low ESR capacitor is recommended, although it is not as critical as for the output capacitor.

The RMS input capacitor ripple current for a boost converter is:

$$I_{RMS(CIN)} = 0.3 \bullet \frac{V_{IN(MIN)}}{L \bullet f} \bullet D_{MAX}$$

Please note that the input capacitor can see a very high surge current when a battery is suddenly connected to the input of the converter and solid tantalum capacitors can fail catastrophically under these conditions. **Be sure to specify surge-tested capacitors!**

Burst Mode Operation and Considerations

The choice of MOSFET $R_{DS(ON)}$ and inductor value also determines the load current at which the LTC1871 enters Burst Mode operation. When bursting, the controller clamps the peak inductor current to approximately:

$$I_{BURST(PEAK)} = \frac{30mV}{R_{DS(ON)}}$$

which represents about 20% of the maximum 150mV SENSE pin voltage. The corresponding average current depends upon the amount of ripple current. Lower inductor values (higher ΔI_L) will reduce the load current at which Burst Mode operations begins, since it is the peak current that is being clamped.

The output voltage ripple can increase during Burst Mode operation if ΔI_L is substantially less than I_{BURST}. This can occur if the input voltage is very low or if a very large inductor is chosen. At high duty cycles, a skipped cycle causes the inductor current to quickly decay to zero. However, because ΔI_L is small, it takes multiple cycles for the current to ramp back up to $I_{BURST(PEAK)}$. During this inductor charging interval, the output capacitor must supply the load current and a significant droop in the output voltage can occur. Generally, it is a good idea to choose a value of inductor ΔI_L between 25% and 40% of $I_{IN(MAX)}$. The alternative is to either increase the value of the output capacitor or disable Burst Mode operation using the MODE/SYNC pin.

Burst Mode operation can be defeated by connecting the MODE/SYNC pin to a high logic-level voltage (either with a control input or by connecting this pin to $INTV_{CC}$). In this mode, the burst clamp is removed, and the chip can operate at constant frequency from continuous conduction mode (CCM) at full load, down into deep discontinuous conduction mode (DCM) at light load. Prior to skipping pulses at very light load (i.e., < 5% of full load), the controller will operate with a minimum switch on-time in DCM.

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Table 1. Recommended Component Manufacturers

VENDOR	COMPONENTS	TELEPHONE	WEB ADDRESS
AVX	Capacitors	(207) 282-5111	avxcorp.com
BH Electronics	Inductors, Transformers	(952) 894-9590	bhelectronics.com
Coilcraft	Inductors	(847) 639-6400	coilcraft.com
Coiltronics	Inductors	(407) 241-7876	coiltronics.com
Diodes, Inc	Diodes	(805) 446-4800	diodes.com
Fairchild	MOSFETs	(408) 822-2126	fairchildsemi.com
General Semiconductor	Diodes	(516) 847-3000	generalsemiconductor.com
International Rectifier	MOSFETs, Diodes	(310) 322-3331	irf.com
IRC	Sense Resistors	(361) 992-7900	irctt.com
Kemet	Tantalum Capacitors	(408) 986-0424	kemet.com
Magnetics Inc	Toroid Cores	(800) 245-3984	mag-inc.com
Microsemi	Diodes	(617) 926-0404	microsemi.com
Murata-Erie	Inductors, Capacitors	(770) 436-1300	murata.co.jp
Nichicon	Capacitors	(847) 843-7500	nichicon.com
On Semiconductor	Diodes	(602) 244-6600	onsemi.com
Panasonic	Capacitors	(714) 373-7334	panasonic.com
Sanyo	Capacitors	(619) 661-6835	sanyo.co.jp
Sumida	Inductors	(847) 956-0667	sumida.com
Taiyo Yuden	Capacitors	(408) 573-4150	t-yuden.com
TDK	Capacitors, Inductors	(562) 596-1212	component.tdk.com
Thermalloy	Heat Sinks	(972) 243-4321	aavidthermalloy.com
Tokin	Capacitors	(408) 432-8020	nec-tokinamerica.com
Toko	Inductors	(847) 699-3430	tokoam.com
United Chemicon	Capacitors	(847) 696-2000	chemi-com.com
Vishay/Dale	Resistors	(605) 665-9301	vishay.com
Vishay/Siliconix	MOSFETs	(800) 554-5565	vishay.com
Vishay/Sprague	Capacitors	(207) 324-4140	vishay.com
Zetex	Small-Signal Discretes	(631) 543-7100	zetex.com

Pulse skipping prevents a loss of control of the output at very light loads and reduces output voltage ripple.

Efficiency Considerations: How Much Does V_{DS} Sensing Help?

The efficiency of a switching regulator is equal to the output power divided by the input power (×100%). Percent efficiency can be expressed as:

% Efficiency = 100% – (L1 + L2 + L3 + …),

where L1, L2, etc. are the individual loss components as a percentage of the input power. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, four main sources usually account for the majority of the losses in LTC1871 application circuits:

1. The supply current into V_{IN}. The V_{IN} current is the sum of the DC supply current I_Q (given in the Electrical Characteristics) and the MOSFET driver and control currents. The DC supply current into the V_{IN} pin is typically about 550µA and represents a small power loss (much less than 1%) that increases with V_{IN}. The driver current results from switching the gate capacitance of the power MOSFET; this current is typically much larger than the DC current. Each time the MOSFET is switched on and

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then off, a packet of gate charge Q_G is transferred from $INTV_{CC}$ to ground. The resulting dQ/dt is a current that must be supplied to the $INTV_{CC}$ capacitor through the V_{IN} pin by an external supply. If the IC is operating in CCM:

$$I_{Q(TOT)} \approx I_Q = f \bullet Q_G$$

$$P_{IC} = V_{IN} \bullet (I_Q + f \bullet Q_G)$$

2. Power MOSFET switching and conduction losses. The technique of using the voltage drop across the power MOSFET to close the current feedback loop was chosen because of the increased efficiency that results from not having a sense resistor. The losses in the power MOSFET are equal to:

$$P_{FET} = \left(\frac{I_{O(MAX)}}{1-D_{MAX}}\right)^2 \bullet R_{DS(ON)} \bullet D_{MAX} \bullet \rho_T$$

$$+k \bullet V_O^{1.85} \bullet \frac{I_{O(MAX)}}{(1-D_{MAX})} \bullet C_{RSS} \bullet f$$

The I^2R power savings that result from not having a discrete sense resistor can be calculated almost by inspection.

$$P_{R(SENSE)} = \left(\frac{I_{O(MAX)}}{1-D_{MAX}}\right)^2 \bullet R_{SENSE} \bullet D_{MAX}$$

To understand the magnitude of the improvement with this V_{DS} sensing technique, consider the 3.3V input, 5V output power supply shown in Figure 1. The maximum load current is 7A (10A peak) and the duty cycle is 39%. Assuming a ripple current of 40%, the peak inductor current is 13.8A and the average is 11.5A. With a maximum sense voltage of about 140mV, the sense resistor value would be 10mΩ, and the power dissipated in this resistor would be 514mW at maximum output current. Assuming an efficiency of 90%, this sense resistor power dissipation represents 1.3% of the overall input power. In other words, for this application, the use of V_{DS} sensing would increase the efficiency by approximately 1.3%.

For more details regarding the various terms in these equations, please refer to the section Boost Converter: Power MOSFET Selection.

3. The losses in the inductor are simply the DC input current squared times the winding resistance. Expressing this loss as a function of the output current yields:

$$P_{R(WINDING)} = \left(\frac{I_{O(MAX)}}{1-D_{MAX}}\right)^2 \bullet R_W$$

4. Losses in the boost diode. The power dissipation in the boost diode is:

$$P_{DIODE} = I_{O(MAX)} \bullet V_D$$

The boost diode can be a major source of power loss in a boost converter. For the 3.3V input, 5V output at 7A example given above, a Schottky diode with a 0.4V forward voltage would dissipate 2.8W, which represents 7% of the input power. Diode losses can become significant at low output voltages where the forward voltage is a significant percentage of the output voltage.

5. Other losses, including C_{IN} and C_O ESR dissipation and inductor core losses, generally account for less than 2% of the total additional loss.

Checking Transient Response

The regulator loop response can be verified by looking at the load transient response. Switching regulators generally take several cycles to respond to an instantaneous step in resistive load current. When the load step occurs, V_O immediately shifts by an amount equal to $(\Delta I_{LOAD})(ESR)$, and then C_O begins to charge or discharge (depending on the direction of the load step) as shown in Figure 13. The regulator feedback loop acts on the resulting error amp output signal to return V_O to its steady-state value. During this recovery time, V_O can be monitored for overshoot or ringing that would indicate a stability problem.

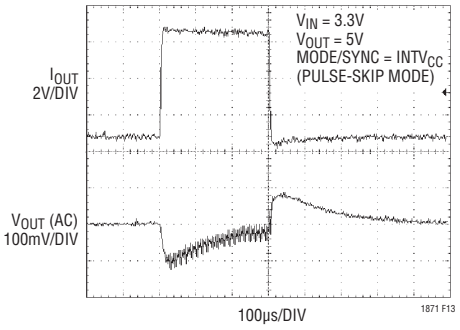

Figure 13. Load Transient Response for a 3.3V Input, 5V Output Boost Converter Application, 0.7A to 7A Step

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A second, more severe transient can occur when connecting loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_O, causing a nearly instantaneous drop in V_O. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive in order to limit the inrush current di/dt to the load.

Boost Converter Design Example

The design example given here will be for the circuit shown in Figure 1. The input voltage is 3.3V, and the output is 5V at a maximum load current of 7A (10A peak).

1. The duty cycle is:

$$D = \left(\frac{V_O + V_D - V_{IN}}{V_O + V_D}\right) = \frac{5 + 0.4 - 3.3}{5 + 0.4} = 38.9\%$$

2. Pulse-skip operation is chosen so the MODE/SYNC pin is shorted to $INTV_{CC}$.

3. The operating frequency is chosen to be 300kHz to reduce the size of the inductor. From Figure 5, the resistor from the FREQ pin to ground is 80k.

4. An inductor ripple current of 40% of the maximum load current is chosen, so the peak input current (which is also the minimum saturation current) is:

$$I_{IN(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}} = 1.2 \bullet \frac{7}{1 - 0.39} = 13.8A$$

The inductor ripple current is:

$$\Delta I_L = \chi \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}} = 0.4 \bullet \frac{7}{1 - 0.39} = 4.6A$$

And so the inductor value is:

$$L = \frac{V_{IN(MIN)}}{\Delta I_L \bullet f} \bullet D_{MAX} = \frac{3.3V}{4.6A \bullet 300kHz} \bullet 0.39 = 0.93\mu H$$

The component chosen is a 1µH inductor made by Sumida (part number CEP125-H 1ROMH) which has a saturation current of greater than 20A.

5. With the input voltage to the IC bootstrapped to the output of the power supply (5V), a logic-level MOSFET can be used. Because the duty cycle is 39%, the maximum SENSE pin threshold voltage is reduced from its low duty cycle typical value of 150mV to approximately 140mV. Assuming a MOSFET junction temperature of 125°C, the room temperature MOSFET $R_{DS(ON)}$ should be less than:

$$R_{DS(ON)} \le V_{SENSE(MAX)} \bullet \frac{1 - D_{MAX}}{\left(1 + \frac{\chi}{2}\right) \bullet I_{O(MAX)} \bullet \rho_T}$$

$$= 0.140V \bullet \frac{1 - 0.39}{\left(1 + \frac{0.4}{2}\right) \bullet 7A \bullet 1.5} = 6.8m\Omega$$

The MOSFET used was the Fairchild FDS7760A, which has a maximum $R_{DS(ON)}$ of 8mΩ at 4.5V V_{GS}, a BV_{DSS} of greater than 30V, and a gate charge of 37nC at 5V V_{GS}.

6. The diode for this design must handle a maximum DC output current of 10A and be rated for a minimum reverse voltage of V_{OUT}, or 5V. A 25A, 15V diode from On Semiconductor (MBRB2515L) was chosen for its high power dissipation capability.

7. The output capacitor usually consists of a high valued bulk C connected in parallel with a lower valued, low ESR ceramic. Based on a maximum output ripple voltage of 1%, or 50mV, the bulk C needs to be greater than:

$$C_{OUT} \ge \frac{I_{OUT(MAX)}}{0.01 \bullet V_{OUT} \bullet f} =$$

$$\frac{7A}{0.01 \bullet 5V \bullet 300kHz} = 466\mu F$$

The RMS ripple current rating for this capacitor needs to exceed:

$$I_{RMS(COUT)} \ge I_{O(MAX)} \bullet \sqrt{\frac{V_O - V_{IN(MIN)}}{V_{IN(MIN)}}} =$$

$$7A \bullet \sqrt{\frac{5V - 3.3V}{3.3V}} = 5A$$

To satisfy this high RMS current demand, four 150µF Panasonic capacitors (EEFUEOJ151R) are required. In parallel with these bulk capacitors, two 22µF, low ESR (X5R) Taiyo Yuden ceramic capacitors

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(JMK325BJ226MM) are added for HF noise reduction. Check the output ripple with a single oscilloscope probe connected directly across the output capacitor terminals, where the HF switching currents flow.

8. The choice of an input capacitor for a boost converter depends on the impedance of the source supply and the amount of input ripple the converter will safely tolerate. For this particular design and lab setup a 100µF Sanyo Poscap (6TPC 100M), in parallel with two 22µF Taiyo Yuden ceramic capacitors (JMK325BJ226MM) is required (the input and return lead lengths are kept to a few inches, but the peak input current is close to 20A!). As with the output node, check the input ripple with a single oscilloscope probe connected across the input capacitor terminals.

PC Board Layout Checklist

1. In order to minimize switching noise and improve output load regulation, the GND pin of the LTC1871 should be connected directly to 1) the negative terminal of the $INTV_{CC}$ decoupling capacitor, 2) the negative terminal of the output decoupling capacitors, 3) the source of the power MOSFET or the bottom terminal of the sense resistor, 4) the negative terminal of the input capacitor and 5) at least one via to the ground plane immediately adjacent to Pin 6. The ground trace on the top layer of the PC board should be as wide and short as possible to minimize series resistance and inductance.

2. Beware of ground loops in multiple layer PC boards. Try to maintain one central ground node on the board and use the input capacitor to avoid excess input ripple for high output current power supplies. If the ground plane is to be used for high DC currents, choose a path away from the small-signal components.

3. Place the C_{VCC} capacitor immediately adjacent to the $INTV_{CC}$ and GND pins on the IC package. This capacitor carries high di/dt MOSFET gate drive currents. A low ESR and ESL 4.7µF ceramic capacitor works well here.

4. The high di/dt loop from the bottom terminal of the output capacitor, through the power MOSFET, through the boost diode and back through the output capacitors should be kept as tight as possible to reduce inductive ringing. Excess inductance can cause increased stress on the power MOSFET and increase HF noise on the output. If low ESR ceramic capacitors are used on the output to reduce output noise, place these capacitors close to the boost diode in order to keep the series inductance to a minimum.

5. Check the stress on the power MOSFET by measuring its drain-to-source voltage directly across the device terminals (reference the ground of a single scope probe directly to the source pad on the PC board). Beware of inductive ringing which can exceed the maximum specified voltage rating of the MOSFET. If this ringing cannot be avoided and exceeds the maximum rating of the device, either choose a higher voltage device or specify an avalanche-rated power MOSFET. Not all MOSFETs are created equal (some are more equal than others).

6. Place the small-signal components away from high frequency switching nodes. In the layout shown in Figure 14, all of the small-signal components have been placed on one side of the IC and all of the power components have been placed on the other. This also allows the use of a pseudo-Kelvin connection for the signal ground, where high di/dt gate driver currents flow out of the IC ground pin in one direction (to the bottom plate of the $INTV_{CC}$ decoupling capacitor) and small-signal currents flow in the other direction.

7. If a sense resistor is used in the source of the power MOSFET, minimize the capacitance between the SENSE pin trace and any high frequency switching nodes. The LTC1871 contains an internal leading edge blanking time of approximately 180ns, which should be adequate for most applications.

8. For optimum load regulation and true remote sensing, the top of the output resistor divider should connect independently to the top of the output capacitor (Kelvin connection), staying away from any high dV/dt traces. Place the divider resistors near the LTC1871 in order to keep the high impedance FB node short.

9. For applications with multiple switching power converters connected to the same input supply, make sure

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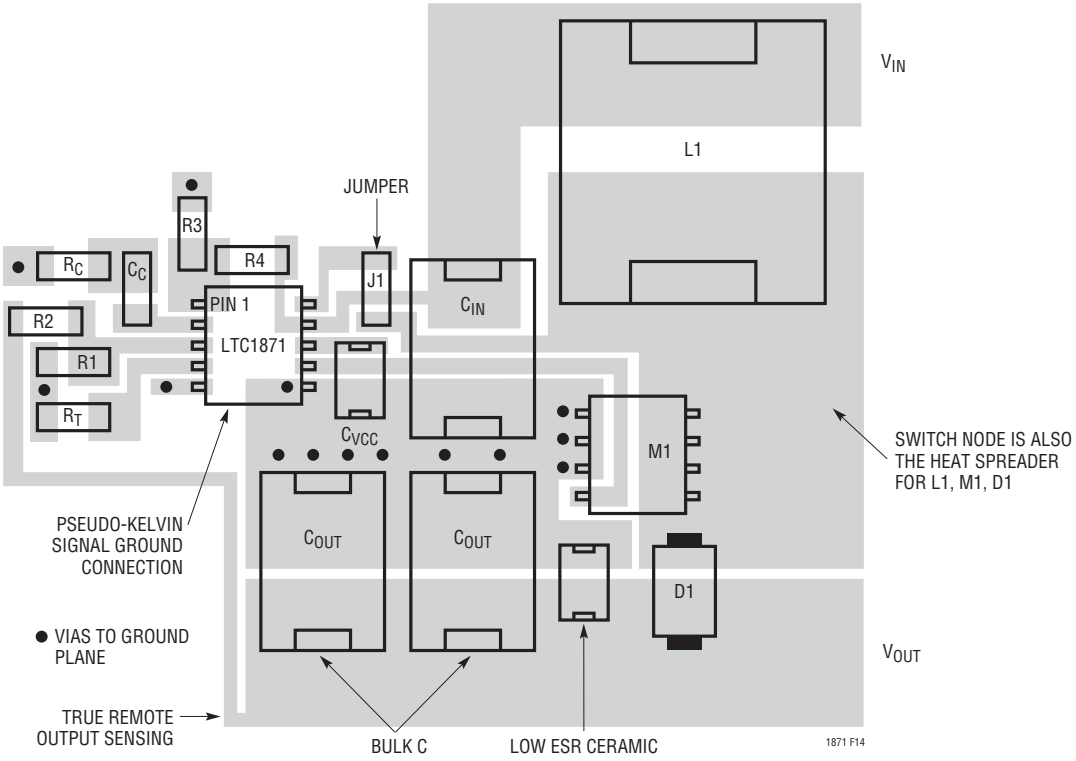

Figure 14. LTC1871 Boost Converter Suggested Layout

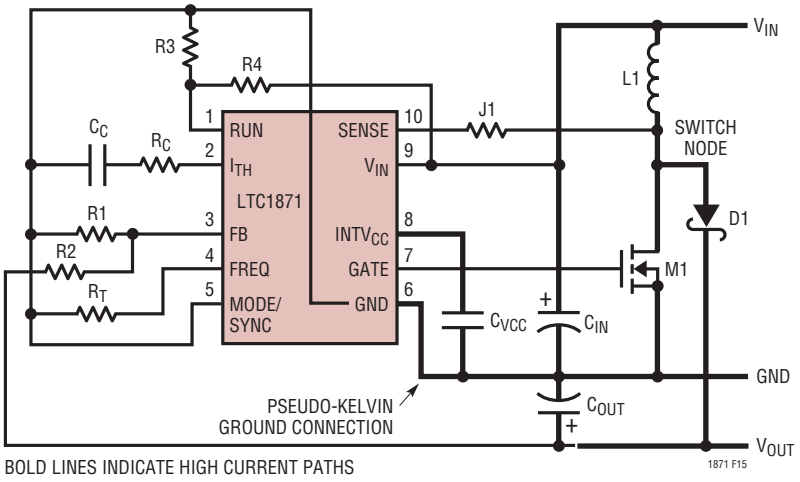

Figure 15. LTC1871 Boost Converter Layout Diagram

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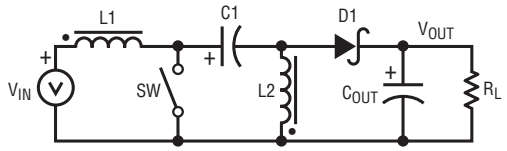
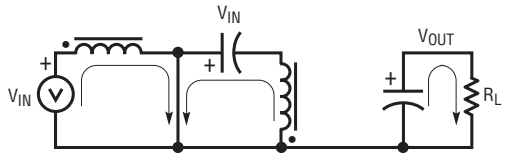
that the input filter capacitor for the LTC1871 is not shared with other converters. AC input current from another converter could cause substantial input voltage ripple, and this could interfere with the operation of the LTC1871. A few inches of PC trace or wire (L ≈ 100nH) between the C_{IN} of the LTC1871 and the actual source V_{IN} should be sufficient to prevent current sharing problems.

SEPIC Converter Applications

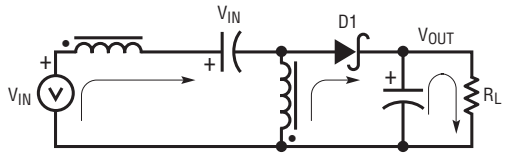
The LTC1871 is also well suited to SEPIC (single-ended primary inductance converter) converter applications. The SEPIC converter shown in Figure 16 uses two inductors. The advantage of the SEPIC converter is the input voltage may be higher or lower than the output voltage, and the output is short-circuit protected.



16a. SEPIC Topology



16b. Current Flow During Switch On-Time



16c. Current Flow During Switch Off-Time

Figures 16. SEPIC Topology and Current Flow

The first inductor, L1, together with the main switch, resembles a boost converter. The second inductor, L2, together with the output diode D1, resembles a flyback or buck-boost converter. The two inductors L1 and L2 can be independent but can also be wound on the same core since identical voltages are applied to L1 and L2 throughout the switching cycle. By making L1 = L2 and winding them on the same core the input ripple is reduced along with cost and size. All of the SEPIC applications information that follows assumes L1 = L2 = L.

SEPIC Converter: Duty Cycle Considerations

For a SEPIC converter operating in a continuous conduction mode (CCM), the duty cycle of the main switch is:

$$D = \left(\frac{V_O + V_D}{V_{IN} + V_O + V_D} \right)$$

where V_D is the forward voltage of the diode. For converters where the input voltage is close to the output voltage the duty cycle is near 50%.

The maximum output voltage for a SEPIC converter is:

$$V_{O(MAX)} = (V_{IN} + V_D) \frac{D_{MAX}}{1 - D_{MAX}} - V_D \frac{1}{1 - D_{MAX}}$$

The maximum duty cycle of the LTC1871 is typically 92%.

SEPIC Converter: The Peak and Average Input Currents

The control circuit in the LTC1871 is measuring the input current (either using the $R_{DS(ON)}$ of the power MOSFET or by means of a sense resistor in the MOSFET source), so the output current needs to be reflected back to the input in order to dimension the power MOSFET properly. Based on the fact that, ideally, the output power is equal to the input power, the maximum input current for a SEPIC converter is:

$$I_{IN(MAX)} = I_{O(MAX)} \bullet \frac{D_{MAX}}{1 - D_{MAX}}$$

The peak input current is:

$$I_{IN(PEAK)} = \left(1 + \frac{\chi}{2} \right) \bullet I_{O(MAX)} \bullet \frac{D_{MAX}}{1 - D_{MAX}}$$

The maximum duty cycle, D_{MAX}, should be calculated at minimum V_{IN}.

The constant 'χ' represents the fraction of ripple current in the inductor relative to its maximum value. For example, if 30% ripple current is chosen, then χ = 0.30 and the peak current is 15% greater than the average.

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It is worth noting here that SEPIC converters that operate at high duty cycles (i.e., that develop a high output voltage from a low input voltage) can have very high input currents, relative to the output current. Be sure to check that the maximum load current will not overload the input supply.

SEPIC Converter: Inductor Selection

For most SEPIC applications the equal inductor values will fall in the range of 10µH to 100µH. Higher values will reduce the input ripple voltage and reduce the core loss. Lower inductor values are chosen to reduce physical size and improve transient response.

Like the boost converter, the input current of the SEPIC converter is calculated at full load current and minimum input voltage. The peak inductor current can be significantly higher than the output current, especially with smaller inductors and lighter loads. The following formulas assume CCM operation and calculate the maximum peak inductor currents at minimum V_{IN}:

$$I_{L1(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet I_{O(MAX)} \bullet \frac{V_O + V_D}{V_{IN(MIN)}}$$

$$I_{L2(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet I_{O(MAX)} \bullet \frac{V_{IN(MIN)} + V_D}{V_{IN(MIN)}}$$

The ripple current in the inductor is typically 20% to 40% (i.e., a range of 'χ' from 0.20 to 0.40) of the maximum average input current occurring at $V_{IN(MIN)}$ and $I_{O(MAX)}$ and $\Delta I_{L1} = \Delta I_{L2}$. Expressing this ripple current as a function of the output current results in the following equations for calculating the inductor value:

$$L = \frac{V_{IN(MIN)}}{\Delta I_L \bullet f} \bullet D_{MAX}$$

where:

$$\Delta I_L = \chi \bullet I_{O(MAX)} \bullet \frac{D_{MAX}}{1 - D_{MAX}}$$

By making L1 = L2 and winding them on the same core, the value of inductance in the equation above is replace by 2L due to mutual inductance. Doing this maintains the same ripple current and energy storage in the inductors. For example, a Coiltronix CTX10-4 is a 10µH inductor with two windings. With the windings in parallel, 10µH inductance is obtained with a current rating of 4A (the number of turns hasn't changed, but the wire diameter has doubled). Splitting the two windings creates two 10µH inductors with a current rating of 2A each. Therefore, substituting 2L yields the following equation for coupled inductors:

$$L1 = L2 = \frac{V_{IN(MIN)}}{2 \bullet \Delta I_L \bullet f} \bullet D_{MAX}$$

Specify the maximum inductor current to safely handle $I_{L(PK)}$ specified in the equation above. The saturation current rating for the inductor should be checked at the minimum input voltage (which results in the highest inductor current) and maximum output current.

SEPIC Converter: Power MOSFET Selection

The power MOSFET serves two purposes in the LTC1871: it represents the main switching element in the power path, and its $R_{DS(ON)}$ represents the current sensing element for the control loop. Important parameters for the power MOSFET include the drain-to-source breakdown voltage (BV_{DSS}), the threshold voltage ($V_{GS(TH)}$), the on-resistance ($R_{DS(ON)}$) versus gate-to-source voltage, the gate-to-source and gate-to-drain charges (Q_{GS} and Q_{GD}, respectively), the maximum drain current ($I_{D(MAX)}$) and the MOSFET's thermal resistances ($R_{TH(JC)}$ and $R_{TH(JA)}$).

The gate drive voltage is set by the 5.2V $INTV_{CC}$ low dropout regulator. Consequently, logic-level threshold MOSFETs should be used in most LTC1871 applications. If low input voltage operation is expected (e.g., supplying power from a lithium-ion battery), then sublogic-level threshold MOSFETs should be used.

The maximum voltage that the MOSFET switch must sustain during the off-time in a SEPIC converter is equal to the sum of the input and output voltages ($V_O + V_{IN}$). As a result, careful attention must be paid to the BV_{DSS} specifications for the MOSFETs relative to the maximum actual switch voltage in the application. Many logic-level devices are limited to 30V or less. Check the switching waveforms directly across the drain and source terminals of the power MOSFET to ensure the V_{DS} remains below the maximum rating for the device.

APPLICATIONS INFORMATION

During the MOSFET's on-time, the control circuit limits the maximum voltage drop across the power MOSFET to about 150mV (at low duty cycle). The peak inductor current is therefore limited to $150mV/R_{DS(ON)}$. The relationship between the maximum load current, duty cycle and the $R_{DS(ON)}$ of the power MOSFET is:

$$R_{DS(ON)} \le \frac{V_{SENSE(MAX)}}{I_{O(MAX)}} \bullet \frac{1}{\left(1+\frac{\chi}{2}\right)\bullet\rho_T} \bullet \frac{1}{\left(\frac{V_O+V_D}{V_{IN(MIN)}}\right)+1}$$

The $V_{SENSE(MAX)}$ term is typically 150mV at low duty cycle and is reduced to about 100mV at a duty cycle of 92% due to slope compensation, as shown in Figure 8. The constant 'χ' in the denominator represents the ripple current in the inductors relative to their maximum current. For example, if 30% ripple current is chosen, then $\chi = 0.30$. The ρ_T term accounts for the temperature coefficient of the $R_{DS(ON)}$ of the MOSFET, which is typically 0.4%/°C. Figure 9 illustrates the variation of normalized $R_{DS(ON)}$ over temperature for a typical power MOSFET.

Another method of choosing which power MOSFET to use is to check what the maximum output current is for a given $R_{DS(ON)}$ since MOSFET on-resistances are available in discrete values.

$$I_{O(MAX)} \le \frac{V_{SENSE(MAX)}}{R_{DS(ON)}} \bullet \frac{1}{\left(1+\frac{\chi}{2}\right)\bullet\rho_T} \bullet \frac{1}{\left(\frac{V_O+V_D}{V_{IN(MIN)}}\right)+1}$$

Calculating Power MOSFET Switching and Conduction Losses and Junction Temperatures

In order to calculate the junction temperature of the power MOSFET, the power dissipated by the device must be known. This power dissipation is a function of the duty cycle, the load current and the junction temperature itself. As a result, some iterative calculation is normally required to determine a reasonably accurate value. Since the controller is using the MOSFET as both a switching and a sensing element, care should be taken to ensure that the converter is capable of delivering the required load current over all operating conditions (load, line and temperature) and for the worst-case specifications for $V_{SENSE(MAX)}$ and the $R_{DS(ON)}$ of the MOSFET listed in the manufacturer's data sheet.

The power dissipated by the MOSFET in a SEPIC converter is:

$$P_{FET} = \left(I_{O(MAX)} \bullet \frac{D_{MAX}}{1-D_{MAX}}\right)^2 \bullet R_{DS(ON)} \bullet D_{MAX} \bullet \rho_T$$

$$+ k \bullet \left(V_{IN(MIN)} + V_O\right)^{1.85} \bullet I_{O(MAX)} \bullet \frac{D_{MAX}}{1-D_{MAX}} \bullet C_{RSS} \bullet f$$

The first term in the equation above represents the I^2R losses in the device and the second term, the switching losses. The constant $k = 1.7$ is an empirical factor inversely related to the gate drive current and has the dimension of 1/current.

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P_{FET} \bullet R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in this equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the board to the ambient temperature in the enclosure. This value of T_J can then be used to check the original assumption for the junction temperature in the iterative calculation process.

SEPIC Converter: Output Diode Selection

To maximize efficiency, a fast-switching diode with low forward drop and low reverse leakage is desired. The output diode in a SEPIC converter conducts current during the switch off-time. The peak reverse voltage that the diode must withstand is equal to $V_{IN(MAX)} + V_O$. The average forward current in normal operation is equal to the output current, and the peak current is equal to:

$$I_{D(PEAK)} = \left(1+\frac{\chi}{2}\right)\bullet I_{O(MAX)} \bullet \left(\frac{V_O+V_D}{V_{IN(MIN)}}+1\right)$$

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \bullet V_D$$

and the diode junction temperature is:

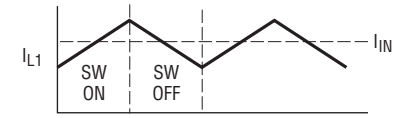
$$T_J = T_A + P_D \bullet R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in this equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the board to the ambient temperature in the enclosure.

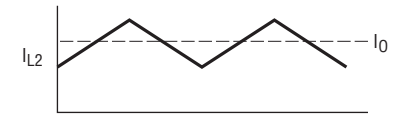
APPLICATIONS INFORMATION

SEPIC Converter: Output Capacitor Selection

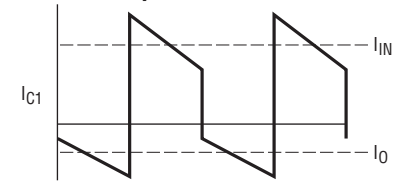
Because of the improved performance of today's electrolytic, tantalum and ceramic capacitors, engineers need to consider the contributions of ESR (equivalent series resistance), ESL (equivalent series inductance) and the bulk capacitance when choosing the correct component for a given output ripple voltage. The effects of these three parameters (ESR, ESL, and bulk C) on the output voltage ripple waveform are illustrated in Figure 17 for a typical coupled-inductor SEPIC converter.



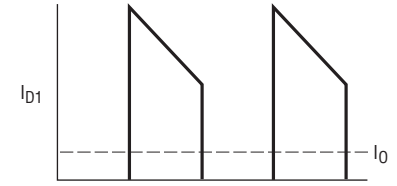
17a. Input Inductor Current



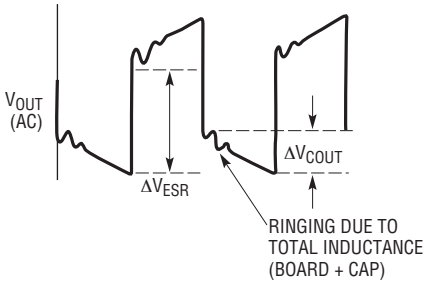
17b. Output Inductor Current



17c. DC Coupling Capacitor Current



17d. Diode Current



17e. Output Ripple Voltage

Figure 17. SEPIC Converter Switching Waveforms

The choice of component(s) begins with the maximum acceptable ripple voltage (expressed as a percentage of the output voltage), and how this ripple should be divided between the ESR step and the charging/discharging ΔV. For the purpose of simplicity we will choose 2% for the maximum output ripple, to be divided equally between the ESR step and the charging/discharging ΔV. This percentage ripple will change, depending on the requirements of the application, and the equations provided below can easily be modified.

For a 1% contribution to the total ripple voltage, the ESR of the output capacitor can be determined using the following equation:

$$ESR_{COUT} \leq \frac{0.01 \bullet V_O}{I_{D(PEAK)}}$$

where:

$$I_{D(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet I_{O(MAX)} \bullet \left(\frac{V_O + V_D}{V_{IN(MIN)}} + 1\right)$$

For the bulk C component, which also contributes 1% to the total ripple:

$$C_{OUT} \geq \frac{I_{O(MAX)}}{0.01 \bullet V_O \bullet f}$$

For many designs it is possible to choose a single capacitor type that satisfies both the ESR and bulk C requirements for the design. In certain demanding applications, however, the ripple voltage can be improved significantly by connecting two or more types of capacitors in parallel. For example, using a low ESR ceramic capacitor can minimize the ESR step, while an electrolytic or tantalum capacitor can be used to supply the required bulk C.

Once the output capacitor ESR and bulk capacitance have been determined, the overall ripple voltage waveform should be verified on a dedicated PC board (see Board Layout section for more information on component placement). Lab breadboards generally suffer from excessive series inductance (due to inter-component wiring), and these parasitics can make the switching waveforms look significantly worse than they would be on a properly designed PC board.

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The output capacitor in a SEPIC regulator experiences high RMS ripple currents, as shown in Figure 17. The RMS output capacitor ripple current is:

$$I_{RMS(COUT)} = I_{O(MAX)} \bullet \sqrt{\frac{V_O}{V_{IN(MIN)}}}$$

Note that the ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be placed in parallel to meet size or height requirements in the design.

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest product of ESR and size of any aluminum electrolytic, at a somewhat higher price.

In surface mount applications, multiple capacitors may have to be placed in parallel in order to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount packages. In the case of tantalum, it is critical that the capacitors have been surge tested for use in switching power supplies. An excellent choice is AVX TPS series of surface mount tantalum. Also, ceramic capacitors are now available with extremely low ESR, ESL and high ripple current ratings.

SEPIC Converter: Input Capacitor Selection

The input capacitor of a SEPIC converter is less critical than the output capacitor due to the fact that an inductor is in series with the input and the input current waveform is triangular in shape. The input voltage source impedance determines the size of the input capacitor which is typically in the range of 10µF to 100µF. A low ESR capacitor is recommended, although it is not as critical as for the output capacitor.

The RMS input capacitor ripple current for a SEPIC converter is:

$$I_{RMS(CIN)} = \frac{1}{\sqrt{12}} \bullet \Delta I_L$$

Please note that the input capacitor can see a very high surge current when a battery is suddenly connected to the input of the converter and solid tantalum capacitors can fail catastrophically under these conditions. **Be sure to specify surge-tested capacitors!**

SEPIC Converter: Selecting the DC Coupling Capacitor

The coupling capacitor C1 in Figure 16 sees nearly a rectangular current waveform as shown in Figure 17. During the switch off-time the current through C1 is $I_O(V_O/V_{IN})$ while approximately $-I_O$ flows during the on-time. This current waveform creates a triangular ripple voltage on C1:

$$\Delta V_{C1(P-P)} = \frac{I_{O(MAX)}}{C1 \bullet f} \bullet \frac{V_O}{V_{IN} + V_O + V_D}$$

The maximum voltage on C1 is then:

$$V_{C1(MAX)} = V_{IN} + \frac{\Delta V_{C1(P-P)}}{2}$$

which is typically close to $V_{IN(MAX)}$. The ripple current through C1 is:

$$I_{RMS(C1)} = I_{O(MAX)} \bullet \sqrt{\frac{V_O + V_D}{V_{IN(MIN)}}}$$

The value chosen for the DC coupling capacitor normally starts with the minimum value that will satisfy 1) the RMS current requirement and 2) the peak voltage requirement (typically close to V_{IN}). Low ESR ceramic and tantalum capacitors work well here.

SEPIC Converter Design Example

The design example given here will be for the circuit shown in Figure 18. The input voltage is 5V to 15V and the output is 12V at a maximum load current of 1.5A (2A peak).

1. The duty cycle range is:

$$D = \left(\frac{V_O + V_D}{V_{IN} + V_O + V_D} \right) = 45.5\% \text{ to } 71.4\%$$

2. The operating mode chosen is pulse skipping, so the MODE/SYNC pin is shorted to $INTV_{CC}$.

APPLICATIONS INFORMATION

3. The operating frequency is chosen to be 300kHz to reduce the size of the inductors; the resistor from the FREQ pin to ground is 80k.

4. An inductor ripple current of 40% is chosen, so the peak input current (which is also the minimum saturation current) is:

$$I_{L1(PEAK)} = \left(1+\frac{\chi}{2}\right)\bullet I_{O(MAX)} \bullet \frac{V_O + V_D}{V_{IN(MIN)}}$$

$$= \left(1+\frac{0.4}{2}\right)\bullet 1.5 \bullet \frac{12+0.5}{5} = 4.5A$$

The inductor ripple current is:

$$\Delta I_L = \chi \bullet I_{O(MAX)} \bullet \frac{D_{MAX}}{1-D_{MAX}}$$

$$= 0.4 \bullet 1.5 \bullet \frac{0.714}{1-0.714} = 1.5A$$

And so the inductor value is:

$$L = \frac{V_{IN(MIN)}}{2 \bullet \Delta I_L \bullet f} \bullet D_{MAX} = \frac{5}{2 \bullet 1.5 \bullet 300k} \bullet 0.714 = 4\mu H$$

The component chosen is a BH Electronics BH510-1007, which has a saturation current of 8A.

5. With an minimum input voltage of 5V, only logic-level power MOSFETs should be considered. Because the maximum duty cycle is 71.4%, the maximum SENSE pin threshold voltage is reduced from its low duty cycle typical value of 150mV to approximately 120mV. Assuming a MOSFET junction temperature of 125°C, the room temperature MOSFET $R_{DS(ON)}$ should be less than:

$$R_{DS(ON)} \le \frac{V_{SENSE(MAX)}}{I_{O(MAX)}} \bullet \frac{1}{\left(1+\frac{\chi}{2}\right)\bullet \rho_T} \bullet \frac{1}{\left(\frac{V_O + V_D}{V_{IN(MIN)}}\right)+1}$$

$$= \frac{0.12}{1.5} \bullet \frac{1}{1.2 \bullet 1.5} \bullet \frac{1}{\left(\frac{12.5}{5}\right)+1} = 12.7m\Omega$$

For a SEPIC converter, the switch BV_{DSS} rating must be greater than $V_{IN(MAX)} + V_O$, or 27V. This comes close to an IRF7811W, which is rated to 30V, and has a maximum room temperature $R_{DS(ON)}$ of 12mΩ at V_{GS} = 4.5V.

6. The diode for this design must handle a maximum DC output current of 2A and be rated for a minimum reverse voltage of $V_{IN} + V_{OUT}$, or 27V. A 3A, 40V diode from International Rectifier (30BQ040) is chosen for its small size, relatively low forward drop and acceptable reverse leakage at high temp.

7. The output capacitor usually consists of a high valued bulk C connected in parallel with a lower valued, low ESR ceramic. Based on a maximum output ripple voltage of 1%, or 120mV, the bulk C needs to be greater than:

$$C_{OUT} \ge \frac{I_{OUT(MAX)}}{0.01 \bullet V_{OUT} \bullet f} =$$

$$\frac{1.5A}{0.01 \bullet 12V \bullet 300kHz} = 41\mu F$$

The RMS ripple current rating for this capacitor needs to exceed:

$$I_{RMS(COUT)} \ge I_{O(MAX)} \bullet \sqrt{\frac{V_O}{V_{IN(MIN)}}} =$$

$$1.5A \bullet \sqrt{\frac{12V}{5V}} = 2.3A$$

To satisfy this high RMS current demand, two 47µF Kemet capacitors (T495X476K020AS) are required. As a result, the output ripple voltage is a low 50mV to 60mV. In parallel with these tantalums, two 10µF, low ESR (X5R) Taiyo Yuden ceramic capacitors (TMK432BJ106MM) are added for HF noise reduction. Check the output ripple with a single oscilloscope probe connected directly across the output capacitor terminals, where the HF switching currents flow.

8. The choice of an input capacitor for a SEPIC converter depends on the impedance of the source supply and the amount of input ripple the converter will safely tolerate. For this particular design and lab setup, a single 47µF Kemet tantalum capacitor (T495X476K020AS) is adequate. As with the output node, check the input ripple with a single oscilloscope probe connected across the input capacitor terminals. If any HF switching noise is observed it is a good idea to decouple the input with a low ESR, X5R ceramic capacitor as close to the V_{IN} and GND pins as possible.

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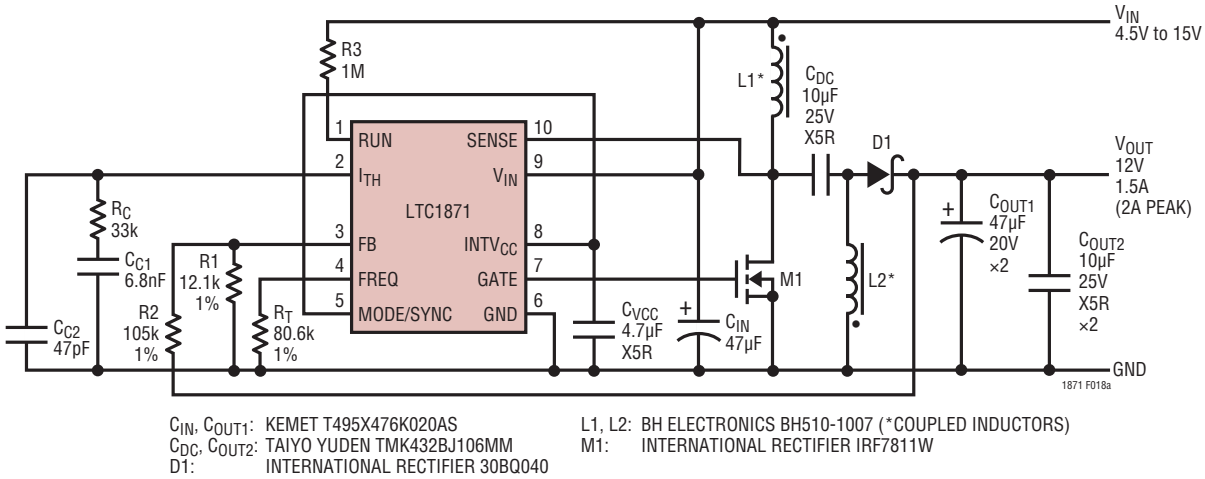
9. The DC coupling capacitor in a SEPIC converter is chosen based on its RMS current requirement and must be rated for a minimum voltage of V_{IN} plus the AC ripple voltage. Start with the minimum value which satisfies the RMS current requirement and then check the ripple voltage to ensure that it doesn't exceed the DC rating.

$$I_{RMS(CI)} \geq I_{O(MAX)} \bullet \sqrt{\frac{V_O + V_D}{V_{IN(MIN)}}}$$

$$= 1.5A \bullet \sqrt{\frac{12V + 0.5V}{5V}} = 2.4A$$

For this design a single 10µF, low ESR (X5R) Taiyo Yuden ceramic capacitor (TMK432BJ106MM) is adequate.



CIN, COUT1: KEMET T495X476K020AS
CDC, COUT2: TAIYO YUDEN TMK432BJ106MM
D1: INTERNATIONAL RECTIFIER 30BQ040
L1, L2: BH ELECTRONICS BH510-1007 (*COUPLED INDUCTORS)
M1: INTERNATIONAL RECTIFIER IRF7811W

Figure 18a. 4.5V to 15V Input, 12V/2A Output SEPIC Converter

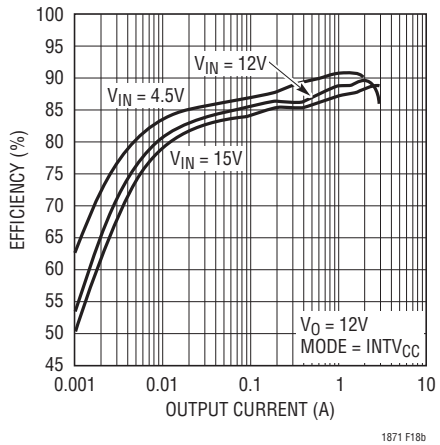


Figure 18b. SEPIC Efficiency vs Output Current

APPLICATIONS INFORMATION

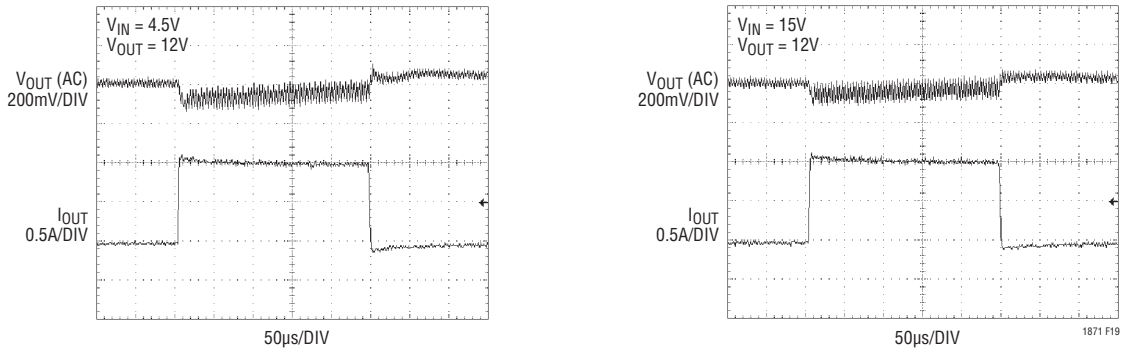
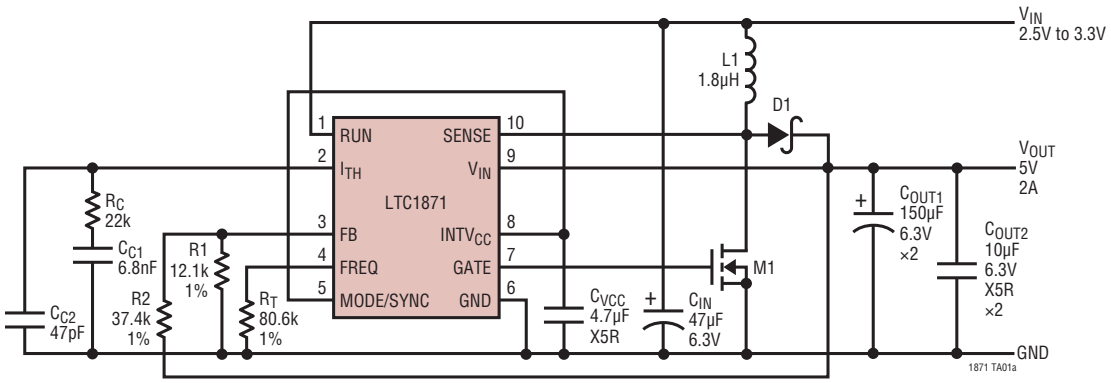


Figure 19. LTC1871 SEPIC Converter Load Step Response

TYPICAL APPLICATIONS

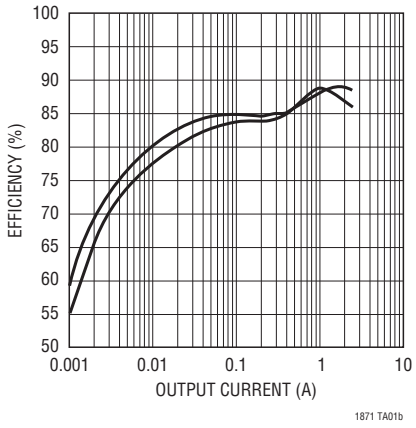
2.5V to 3.3V Input, 5V/2A Output Boost Converter



C_{IN}: SANYO POSCAP 6TPA47M
C_{OUT1}: SANYO POSCAP 6TPB150M
C_{OUT2}: TAIYO YUDEN JMK316BJ106ML
C_{VCC}: TAIYO YUDEN LMK316BJ475ML

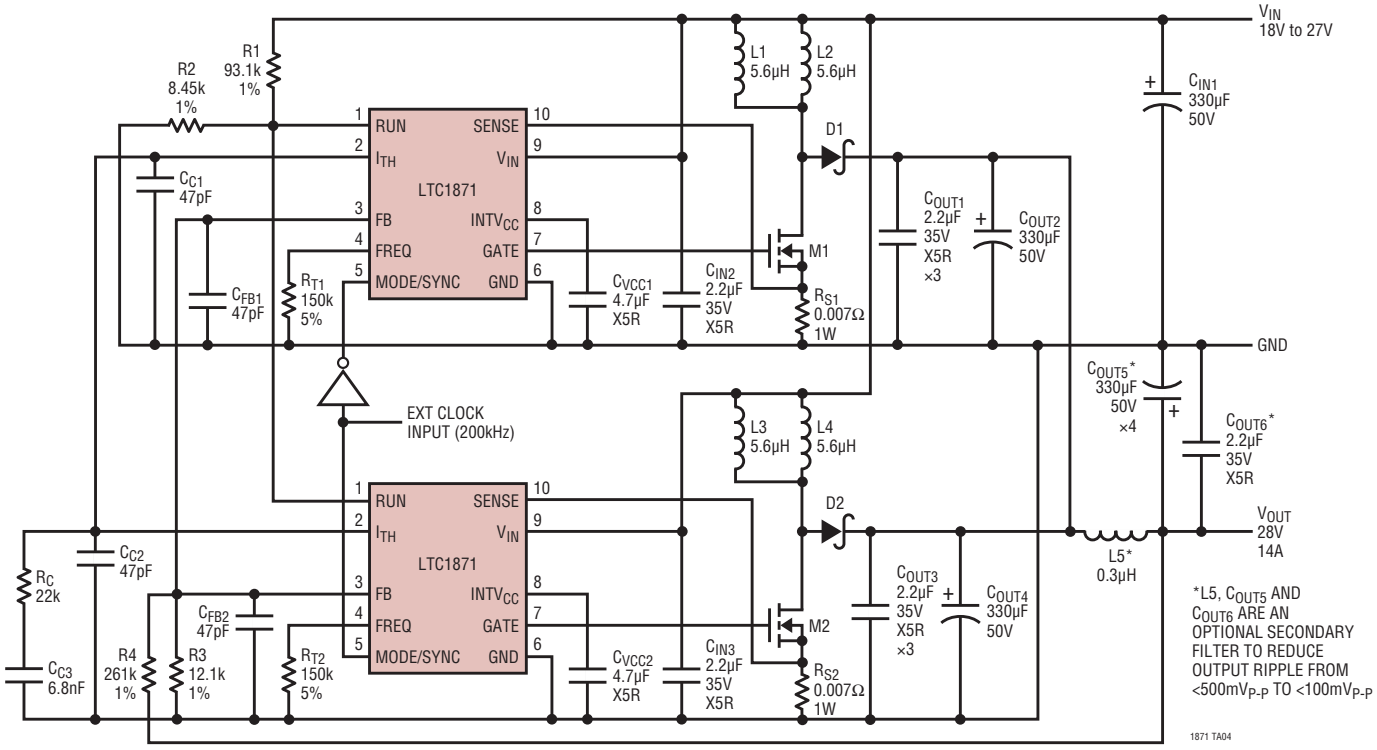
D1: INTERNATIONAL RECTIFIER 30BQ015
L1: TOKO DS104C2 B952AS-1R8N
M1: SILICONIX/VISHAY Si9426

Output Efficiency at 2.5V and 3.3V Input



TYPICAL APPLICATIONS

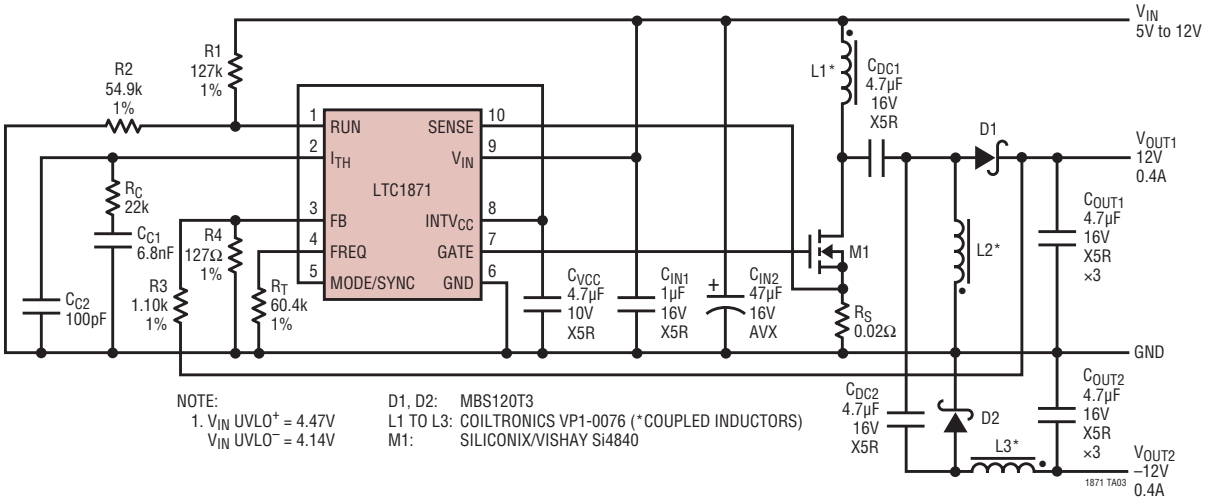
18V to 27V Input, 28V Output, 400W 2-Phase, Low Ripple, Synchronized RF Base Station Power Supply (Boost)



CIN1: SANYO 50MV330AX
CIN2, 3: TAIYO YUDEN GMK325BJ225MN
COUT2, 4, 5: SANYO 50MV330AX
COUT1, 3, 6: TAIYO YUDEN GMK325BJ225MN
VCC1, 2: TAIYO YUDEN LMK316BJ475ML

L1 TO L4: SUMIDA CEP125-5R6MC-HD
L5: SUMIDA CEP125-0R3NC-ND
D1, D2: ON SEMICONDUCTOR MBR2045CT
M1, M2: INTERNATIONAL RECTIFIER IRLZ44NS

5V to 12V Input, ±12V/0.2A Output SEPIC Converter with Undervoltage Lockout

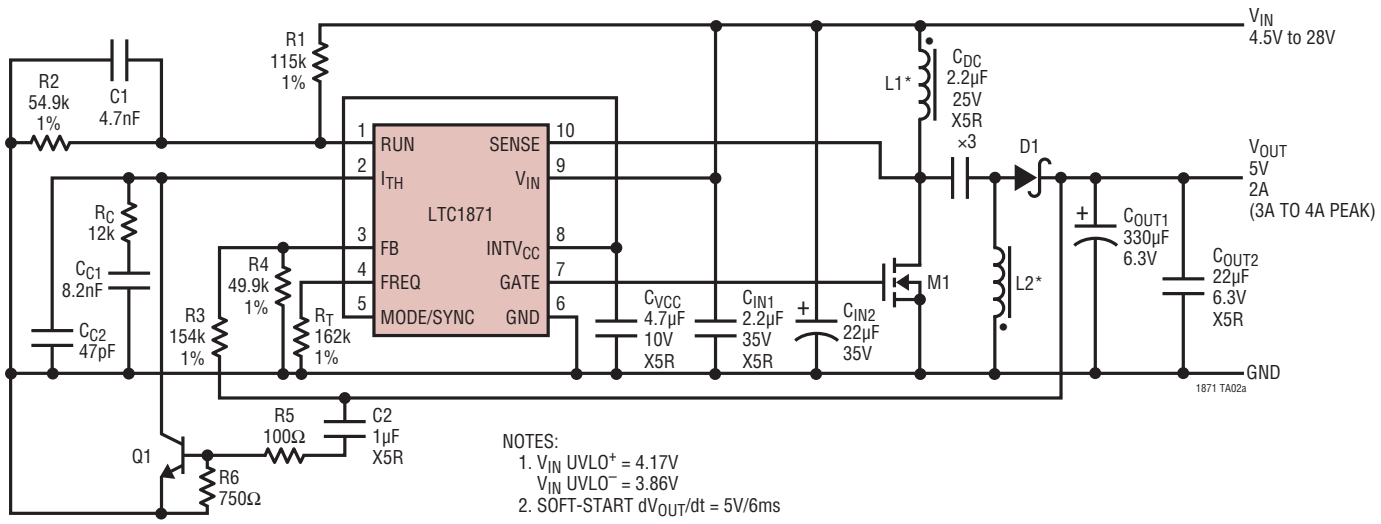


NOTE:
1. V_{IN} UVLO+ = 4.47V
V_{IN} UVLO− = 4.14V

D1, D2: MBS120T3
L1 TO L3: COILTRONICS VP1-0076 (*COUPLED INDUCTORS)
M1: SILICONIX/VISHAY Si4840

TYPICAL APPLICATIONS

4.5V to 28V Input, 5V/2A Output SEPIC Converter with Undervoltage Lockout and Soft-Start

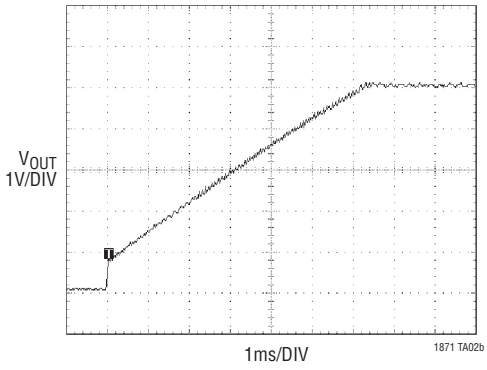


NOTES:
1. V_{IN} UVLO$^+$ = 4.17V
   V_{IN} UVLO$^-$ = 3.86V
2. SOFT-START dV_{OUT}/dt = 5V/6ms

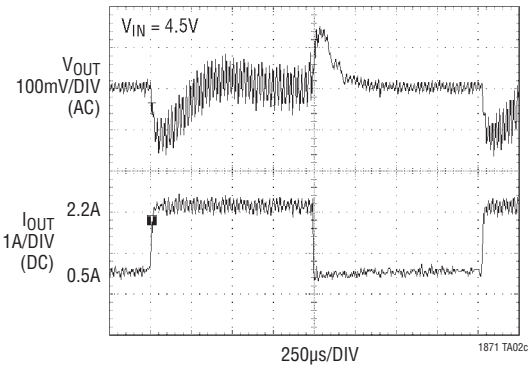
C_{IN1}, C_{DC}: TAIYO YUDEN GMK325BJ225MN
C_{IN2}: AVX TPSE226M035R0300
C_{OUT1}: SANYO 6TPB330M
C_{OUT2}: TAIYO YUDEN JMK325BJ226MN
C_{VCC}: LMK316BJ475ML

D1: INTERNATIONAL RECTIFIER 30BQ040
L1, L2: BH ELECTRONICS BH510-1007 (*COUPLED INDUCTORS)
M1: SILICONIX/VISHAY Si4840
Q1: PHILIPS BC847BF

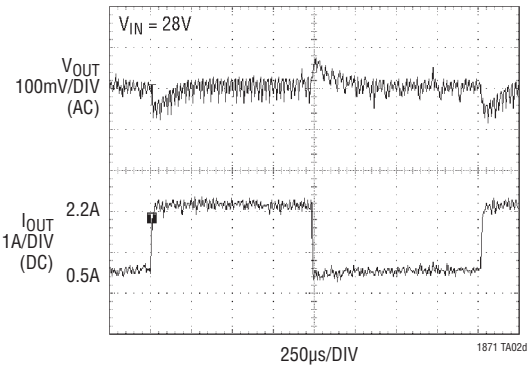
Soft-Start



Load Step Response at V_{IN} = 4.5V

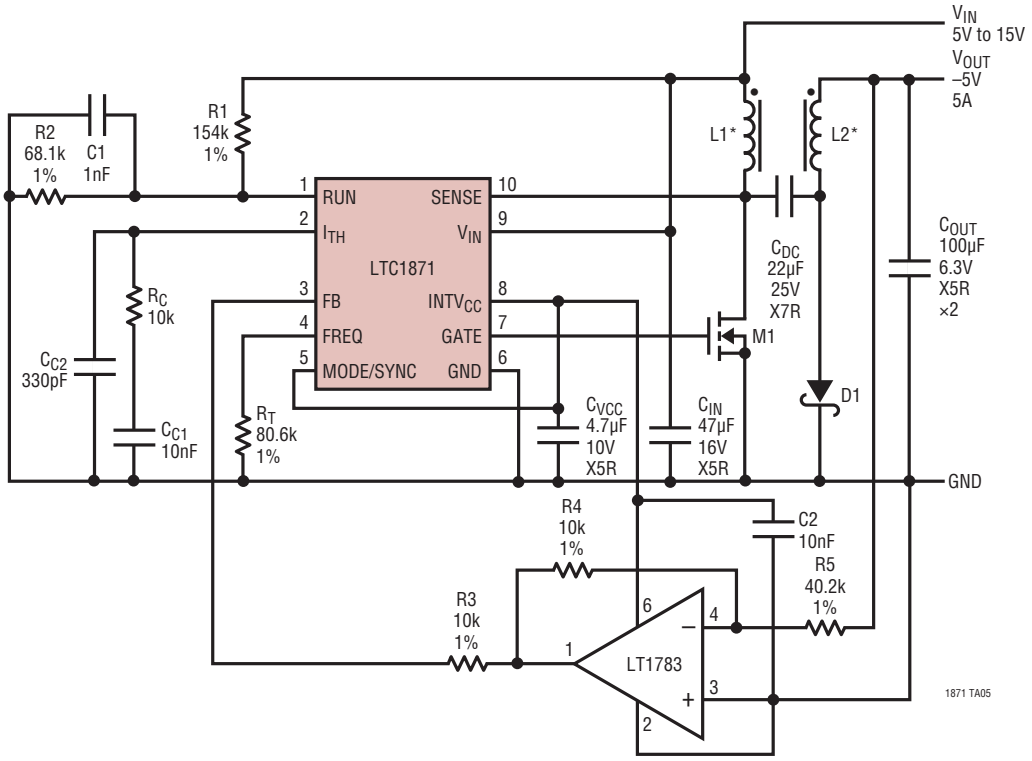


Load Step Response at V_{IN} = 28V



TYPICAL APPLICATIONS

5V to 15V Input, –5V/5A Output Positive-to-Negative Converter with Undervoltage Lockout and Level-Shifted Feedback

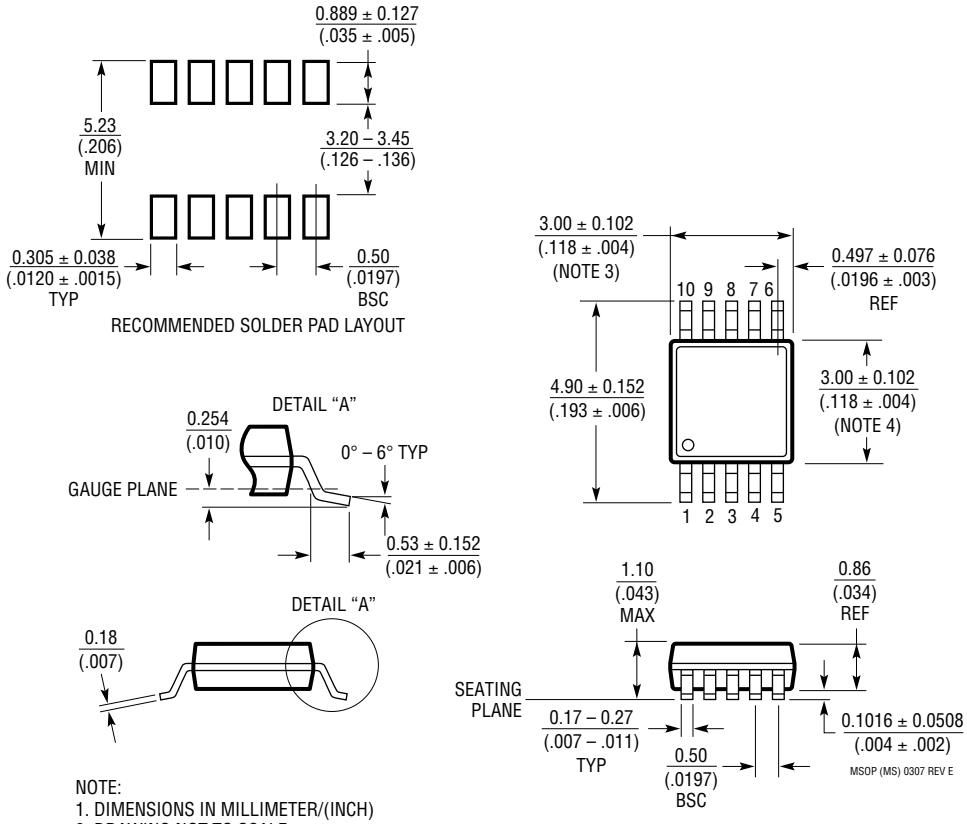


C_{IN}: TDK C5750X5R1C476M
C_{DC}: TDK C5750X7R1E226M
C_{OUT}: TDK C5750X5R0J107M
C_{VCC}: TAIYO YUDEN LMK316BJ475ML

D1: ON SEMICONDUCTOR MBRB2035CT
L1, L2: COILTRONICS VP5-0053 (*3 WINDINGS IN PARALLEL FOR THE PRIMARY, 3 IN PARALLEL FOR SECONDARY)
M1: INTERNATIONAL RECTIFIER IRF7822

PACKAGE DESCRIPTION

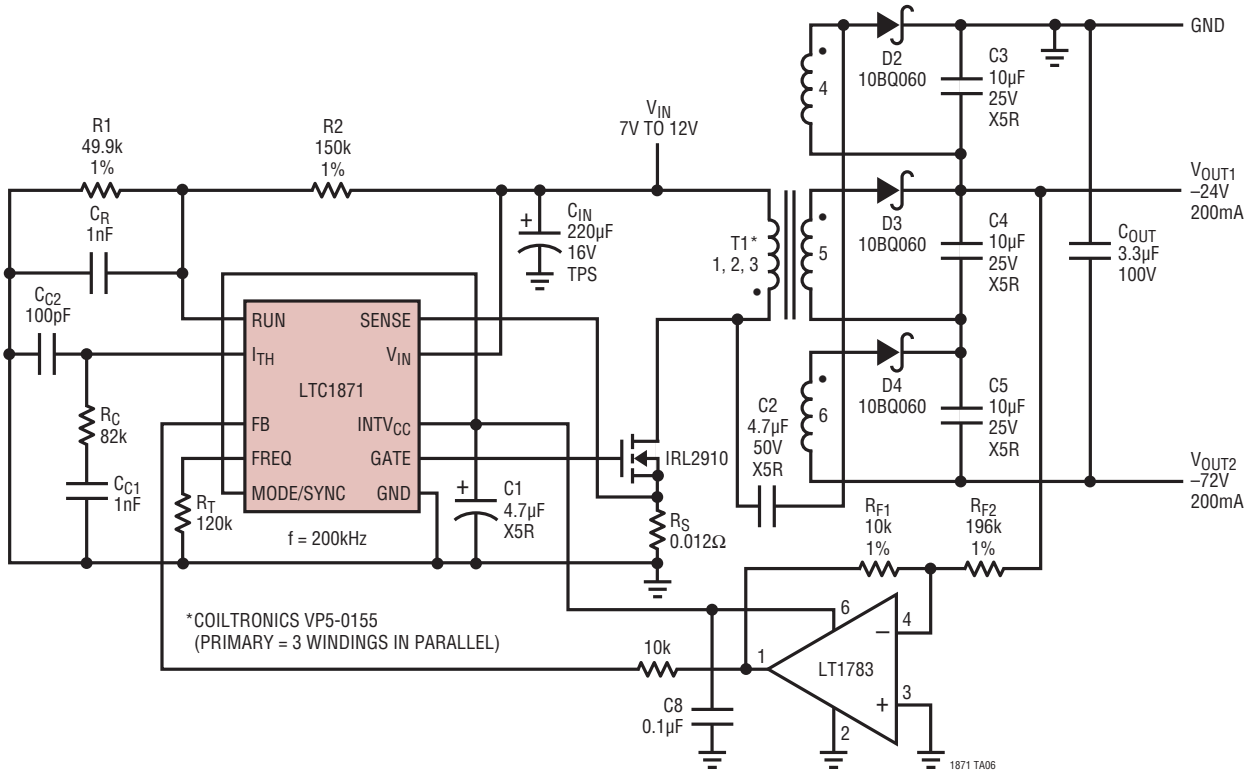
MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661 Rev E)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

High Power SLIC Supply with Undervoltage Lockout
(Also See the LTC3704 Data Sheet)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1619	Current Mode PWM Controller	300kHz Fixed Frequency, Boost, SEPIC, Flyback Topology
LTC1624	Current Mode DC/DC Controller	SO-8; 300kHz Operating Frequency; Buck, Boost, SEPIC Design; V_{IN} Up to 36V
LTC1700	No R_{SENSE} Synchronous Step-Up Controller	Up to 95% Efficiency, Operation as Low as 0.9V Input
LTC1871-7	Wide Input Range Controller	No R_{SENSE}, 7V Gate Drive, Current Mode Control
LTC1872	SOT-23 Boost Controller	Delivers Up to 5A, 550kHz Fixed Frequency, Current Mode
LT1930	1.2MHz, SOT-23 Boost Converter	Up to 34V Output, 2.6V ≤ V_{IN} ≤ 16V, Miniature Design
LT1931	Inverting 1.2MHz, SOT-23 Converter	Positive-to-Negative DC/DC Conversion, Miniature Design
LTC3401/LTC3402	1A/2A 3MHz Synchronous Boost Converters	Up to 97% Efficiency, Very Small Solution, 0.5V ≤ V_{IN} ≤ 5V
LTC3704	Positive-to-Negative DC/DC Controller	No R_{SENSE}, Current Mode Control, 50kHz to 1MHz
LT3782	2-Phase Step-Up DC/DC Controller	6V ≤ V_{IN} ≤ 40V; 4A Gate Drive, 150kHz to 500kHz

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