

## FEATURES

- Allows Safe Board Insertion into Live Backplane
- Small Footprint
- 4mΩ MOSFET Including R<sub>SENSE</sub>
- Guaranteed Safe Operating Area: 81W, 30ms
- Wide Operating Voltage Range: 2.9V to 15V
- Adjustable, 11% Accurate Current Limit
- Current and Temperature Monitor Outputs
- Overtemperature Protection
- Adjustable Current Limit Timer Before Fault
- Power Good and Fault Outputs
- Adjustable Inrush Current Control
- 2.5% Accurate Undervoltage and Overvoltage Protection
- Available in a 38-Pin (5mm × 9mm) QFN Package

## APPLICATIONS

- High Availability Servers
- Solid State Drives
- Industrial
- 240W, 12V Systems

## DESCRIPTION

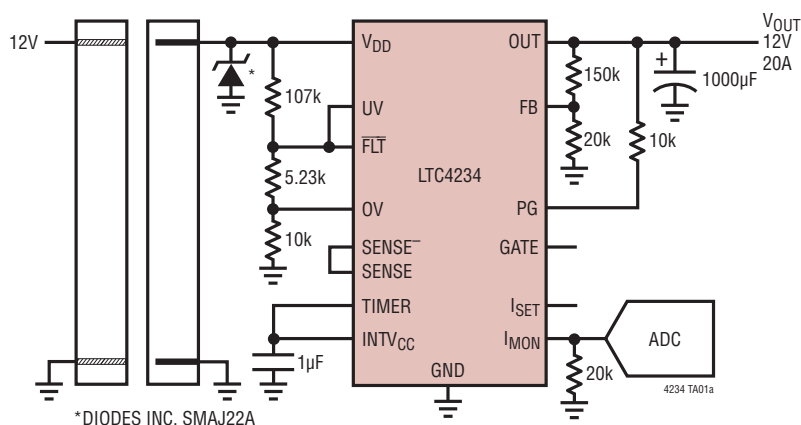
The LTC<sup>®</sup>4234 is an integrated solution for Hot Swap™ applications that allows a board to be safely inserted and removed from a live backplane. The part integrates a Hot Swap controller, power MOSFET and current sense resistor in a single package for small form factor applications. The MOSFET Safe Operating Area is production tested and guaranteed for the stresses in Hot Swap applications.

The LTC4234 provides separate inrush current control and a 11% accurate 22.5A current limit with output dependent foldback. The current limit threshold can be adjusted dynamically using the I<sub>SET</sub> pin. Additional features include a current monitor output that amplifies the sense resistor voltage for ground referenced current sensing and a MOSFET temperature monitor output. Thermal limit, overvoltage, undervoltage and power good monitoring are also provided.

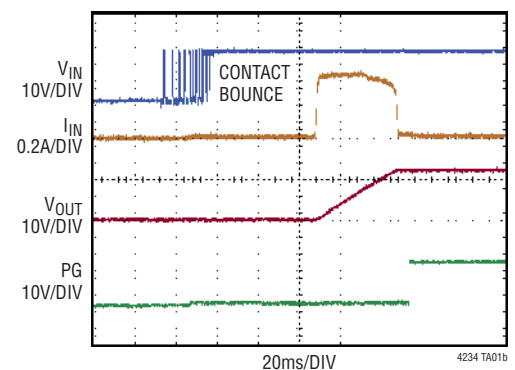
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## TYPICAL APPLICATION

12V, 20A Card Resident Application with Auto-Retry



Power-Up Waveform



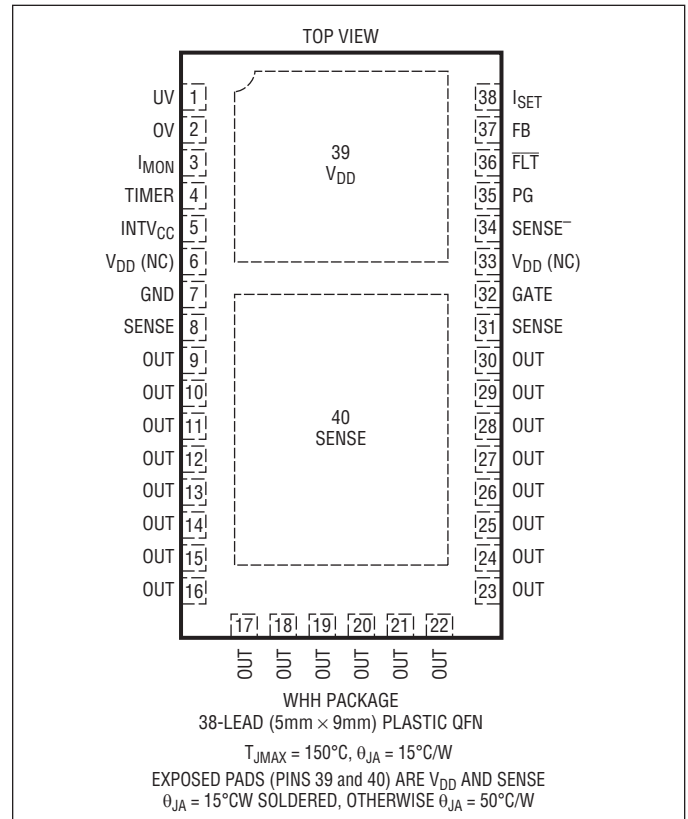
# LTC4234

## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage ( $V_{DD}$ ) .....	-0.3V to 28V
Input Voltages	
FB, OV, UV .....	-0.3V to 12V
TIMER .....	-0.3V to 3.5V
SENSE <sup>-</sup> , SENSE .....	$V_{DD} - 10V$ or $-0.3V$ to $V_{DD} + 0.3V$
Output Voltages	
I <sub>SET</sub> , I <sub>MON</sub> .....	-0.3V to 3V
PG, FLT .....	-0.3V to 35V
OUT .....	-0.3V to $V_{DD} + 0.3V$
INTV <sub>CC</sub> .....	-0.3V to 3.5V
GATE (Note 3) .....	-0.3V to 33V
Operating Ambient Temperature Range	
LTC4234C .....	0°C to 70°C
LTC4234I .....	-40°C to 85°C
LTC4234H .....	-40°C to 125°C
Junction Temperature (Notes 4, 5) .....	150°C
Storage Temperature Range .....	-65°C to 150°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4234CW4H#PBF	LTC4234CW4H#TRPBF	4234	38-Lead (5mm × 9mm) Plastic QFN	0°C to 70°C
LTC4234IW4H#PBF	LTC4234IW4H#TRPBF	4234	38-Lead (5mm × 9mm) Plastic QFN	-40°C to 85°C
LTC4234HW4H#PBF	LTC4234HW4H#TRPBF	4234	38-Lead (5mm × 9mm) Plastic QFN	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{DD} = 12\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>DC Characteristics</b>							
$V_{DD}$	Input Supply Range		●	2.9		15	V
$I_{DD}$	Input Supply Current	MOSFET On, No Load	●		1.6	3	mA
$V_{DD(UVL)}$	Input Supply Undervoltage Lockout	$V_{DD}$ Rising	●	2.63	2.73	2.85	V
$I_{OUT}$	OUT Pin Leakage Current	$V_{OUT} = V_{GATE} = 0\text{V}$ , $V_{DD} = 15\text{V}$	●		0	$\pm 700$	$\mu\text{A}$
		$V_{OUT} = V_{GATE} = 12\text{V}$	●	1	2	4	$\mu\text{A}$
$\Delta V_{GATE}/\Delta t$	OUT Pin Turn-On Ramp Rate	GATE Open	●	0.15	0.35	0.6	V/ms
$R_{ON}$	MOSFET + Sense Resistor On-Resistance	C-Grade, I-Grade	●	2.3	4.0	7.2	$\text{m}\Omega$
		H-Grade	●	2.3	4.0	8.2	$\text{m}\Omega$
$I_{LIM(TH)}$	Current Limit Threshold	$V_{FB} = 1.35\text{V}$ , $I_{SET}$ Open	●	20	22.5	25	A
		$V_{FB} = 0\text{V}$ , $I_{SET}$ Open	●	4	5.7	7.4	A
		$V_{FB} = 1.35\text{V}$ , $R_{SET} = 20\text{k}$	●	9.4	11.1	12.8	A
SOA	MOSFET Safe Operating Area	13.5V, 6A Folded Back		30	90		ms
		7.5V, 22A Onset of Foldback			40		ms
<b>Inputs</b>							
$I_{IN}$	OV, UV, FB Pin Input Current	$V = 1.2\text{V}$	●		0	$\pm 1$	$\mu\text{A}$
$I_{SENSE-(IN)}$	SENSE <sup>-</sup> Pin Input Current	$V_{SENSE-} = 12\text{V}$	●		4	$\pm 10$	$\mu\text{A}$
$V_{TH}$	OV, UV, FB Pin Threshold Voltage	$V_{PIN}$ Rising	●	1.205	1.235	1.265	V
$\Delta V_{OV(HYST)}$	OV Pin Hysteresis		●	10	20	30	mV
$\Delta V_{UV(HYST)}$	UV Pin Hysteresis		●	50	80	110	mV
$V_{UV(RTH)}$	UV Pin Reset Threshold Voltage	$V_{UV}$ Falling	●	0.55	0.62	0.7	V
$\Delta V_{FB(HYST)}$	FB Pin Power Good Hysteresis		●	10	20	30	mV
$R_{ISET}$	$I_{SET}$ Pin Internal Resistor		●	19	20	21	k $\Omega$
<b>Outputs</b>							
$V_{INTVCC}$	INTV <sub>CC</sub> Output Voltage	$V_{DD} = 5\text{V}, 15\text{V}$ , $I_{LOAD} = 0\text{mA}, -10\text{mA}$	●	2.8	3.1	3.3	V
$V_{OL}$	PG, $\overline{\text{FLT}}$ Pin Output Low Voltage	$I = 2\text{mA}$	●		0.4	0.8	V
$I_{OH}$	PG, $\overline{\text{FLT}}$ Pin Input Leakage Current	$V = 30\text{V}$	●		0	$\pm 10$	$\mu\text{A}$
$V_{TIMER(H)}$	TIMER Pin High Threshold	$V_{TIMER}$ Rising	●	1.2	1.235	1.28	V
$V_{TIMER(L)}$	TIMER Pin Low Threshold	$V_{TIMER}$ Falling	●	0.1	0.21	0.3	V
$I_{TIMER(UP)}$	TIMER Pin Pull-Up Current	$V_{TIMER} = 0\text{V}$	●	-80	-100	-120	$\mu\text{A}$
$I_{TIMER(DN)}$	TIMER Pin Pull-Down Current	$V_{TIMER} = 1.2\text{V}$	●	1.4	2	2.6	$\mu\text{A}$
$I_{TIMER(RATIO)}$	TIMER Pin Current Ratio $I_{TIMER(DN)}/I_{TIMER(UP)}$		●	1.6	2	2.7	%
$A_{IMON}$	$I_{MON}$ Pin Current Gain		●	4.5	5	5.25	$\mu\text{A}/\text{A}$
$I_{OFF(IMON)}$	$I_{MON}$ Pin Offset Current	$I_{OUT} = 600\text{mA}$	●		0	$\pm 9$	$\mu\text{A}$
$I_{GATE(UP)}$	Gate Pull-Up Current	Gate Drive On, $V_{GATE} = V_{OUT} = 12\text{V}$	●	-18	-24	-29	$\mu\text{A}$
$I_{GATE(DN)}$	Gate Pull-Down Current	Gate Drive Off, $V_{GATE} = 18\text{V}$ , $V_{OUT} = 12\text{V}$	●	180	250	500	$\mu\text{A}$
$I_{GATE(FST)}$	Gate Fast Pull-Down Current	Fast Turn Off, $V_{GATE} = 18\text{V}$ , $V_{OUT} = 12\text{V}$			140		mA

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{DD} = 12\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>AC Characteristics</b>							
$t_{PHL(GATE)}$	Input High (OV), Input Low (UV) to GATE Low Propagation Delay	$V_{GATE} < 17.8\text{V}$ Falling	●		8	20	$\mu\text{s}$
$t_{PHL(ILIM)}$	Short Circuit to GATE Low	$V_{FB} = 0$ , Step $V_{DD} - \text{SENSE}^-$ to 50mV, $V_{GATE} < 15\text{V}$ Falling	●		1	5	$\mu\text{s}$
$t_{D(ON)}$	Turn-On Delay	Step $V_{UV}$ to 2V, $V_{GATE} > 13\text{V}$	●	24	48	72	ms
$t_{D(CB)}$	Circuit Breaker Filter Delay Time (Internal)	$V_{FB} = 0$ , Step $V_{DD} - \text{SENSE}^-$ to 50mV	●	1.2	2	2.7	ms
$t_{D(COOL\_DOWN)}$	Cool Down Delay (Internal)		●	600	900	1200	ms

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into pins are positive; all voltages are referenced to GND unless otherwise specified.

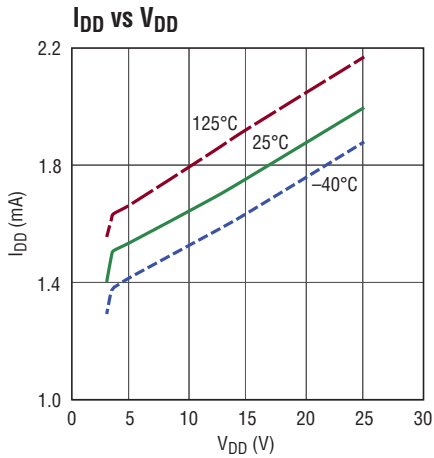
**Note 3:** An internal clamp limits the GATE pin to a maximum of 6.5V above OUT. Driving this pin to voltages beyond the clamp may damage the device.

**Note 4:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed  $150^\circ\text{C}$  when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

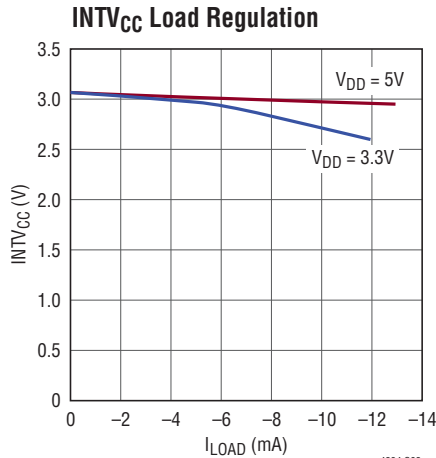
**Note 5:**  $T_J$  is calculated from the ambient temperature,  $T_A$ , and power dissipation,  $P_D$ , according to the formula:

$$T_J = T_A + (P_D \cdot 15^\circ\text{C/W})$$

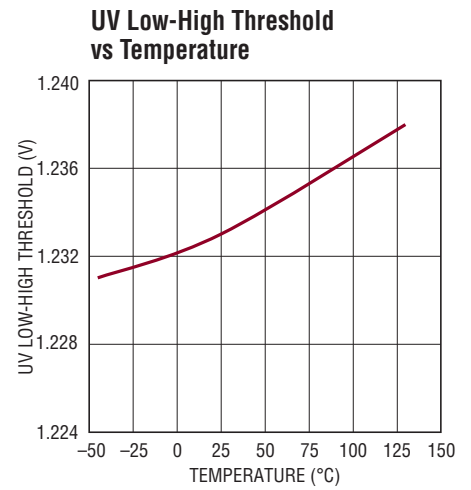
**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 12\text{V}$  unless otherwise noted.



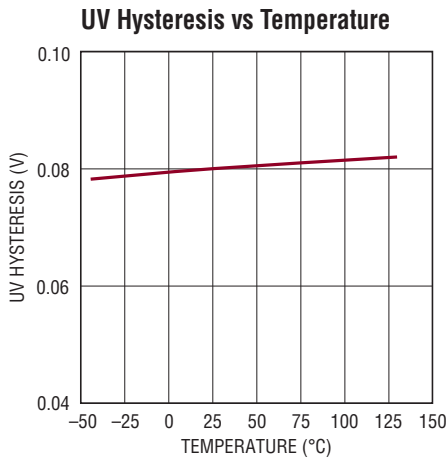
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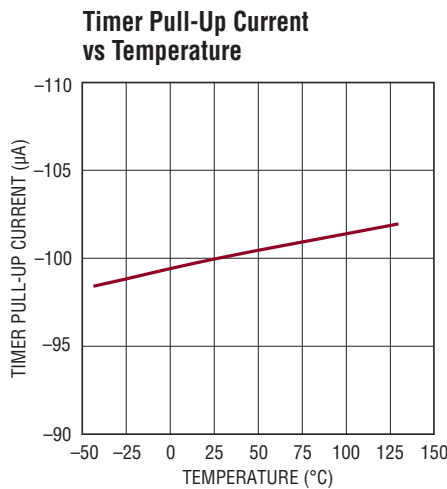
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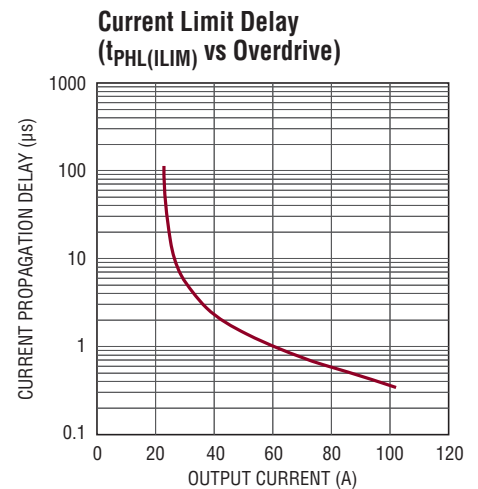
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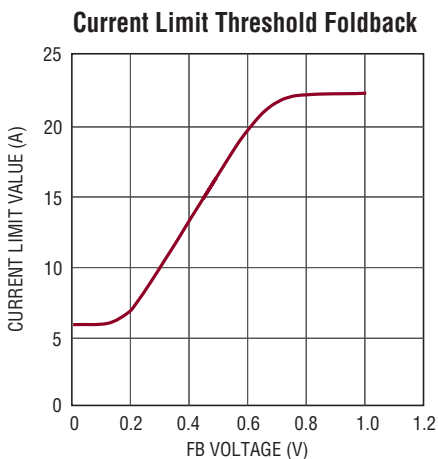
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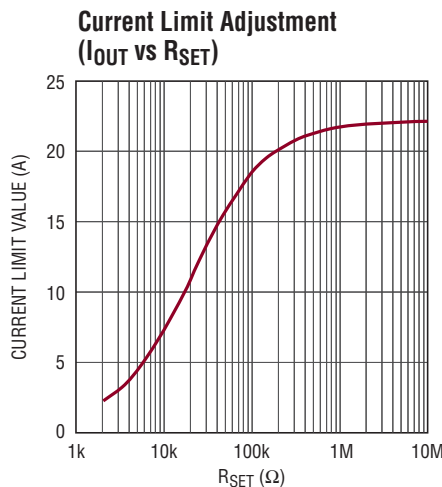
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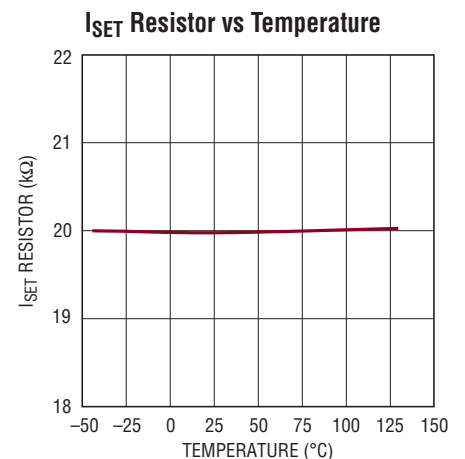
4234 G06



4234 G07

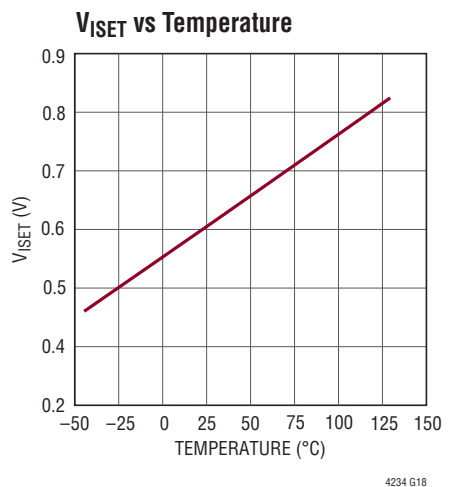
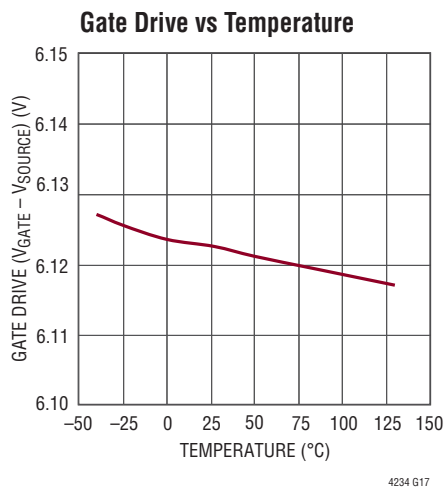
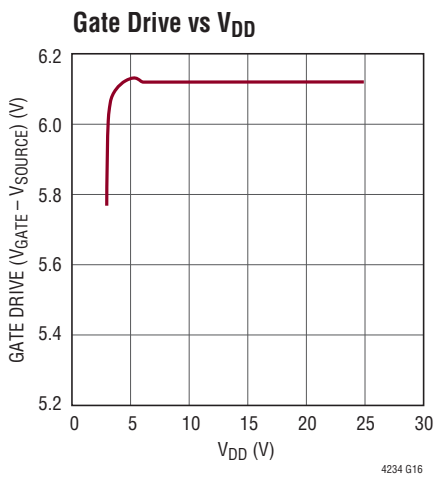
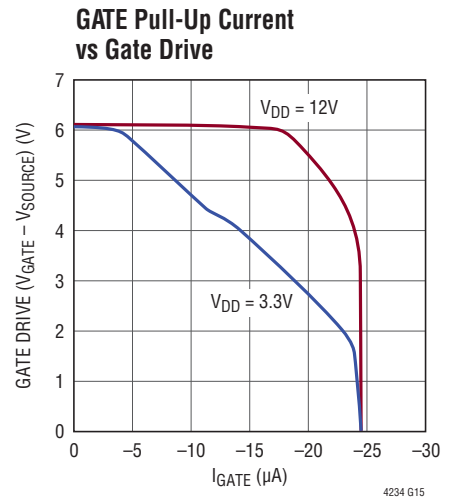
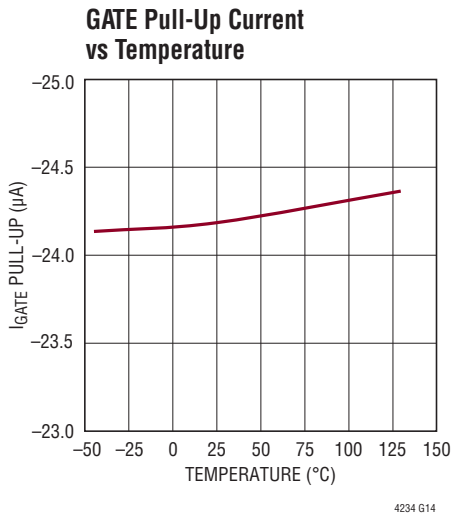
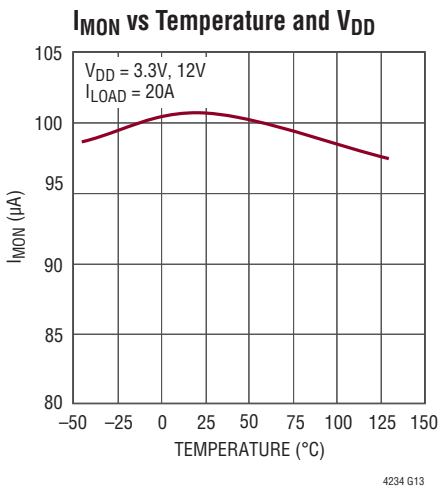
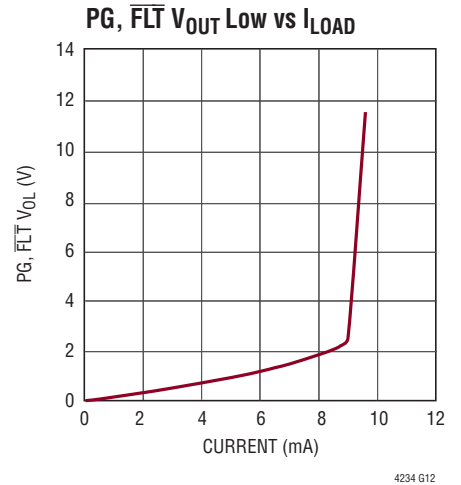
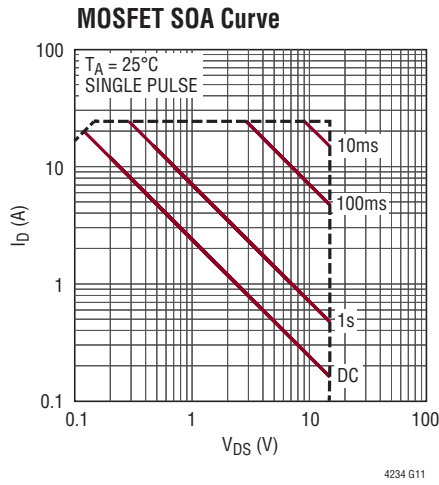
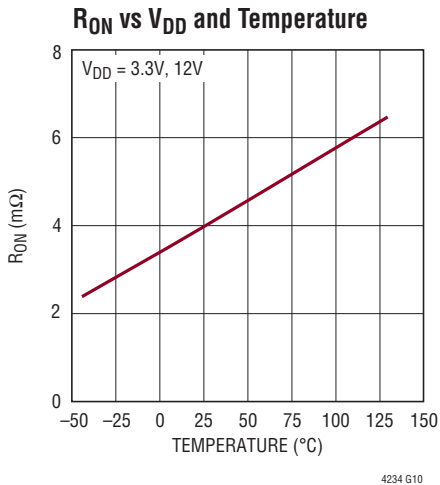


4234 G08



4234 G09

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , $V_{DD} = 12\text{V}$ unless otherwise noted.



## PIN FUNCTIONS

**FB:** Foldback and Power Good Input. Connect this pin to an external resistive divider from OUT. If the voltage falls below 0.6V, the current limit is reduced using a foldback profile (see the Typical Performance Characteristics section). If the voltage falls below 1.21V, the PG pin will pull low to indicate the power is bad

**FLT:** Overcurrent Fault Indicator. Open-drain output pulls low when an overcurrent fault has occurred and the circuit breaker trips. For overcurrent auto-retry tie to UV pin (see Applications Information section for details).

**GATE:** Gate Drive for Internal N-Channel MOSFET. An internal 24 $\mu$ A current source charges the gate of the N-channel MOSFET. At start-up the GATE pin ramps up at a 0.35V/ms rate determined by internal circuitry. During an undervoltage or overvoltage condition a 250 $\mu$ A pull-down current turns the MOSFET off. During a short circuit or undervoltage lockout condition, a 140mA pull-down current source between GATE and OUT is activated.

**GND:** Device Ground.

**I<sub>MON</sub>:** Current Monitor Output. The current in the internal MOSFET switch is divided by 200,000 and sourced from this pin. Placing a 20k resistor on this pin allows a 0V to 2V voltage swing when current ranges from 0A to 20A.

**INTV<sub>CC</sub>:** Internal 3.1V Supply Decoupling Output. This pin must have a 1.0 $\mu$ F or larger bypass capacitor.

**I<sub>SET</sub>:** Current Limit Adjustment Pin. For 22.5A current limit value, open this pin. This pin is driven by a 20k resistor in series with a voltage source. The pin voltage is used to generate the current limit threshold. The internal 20k resistor and an external resistor between I<sub>SET</sub> and ground create an attenuator that lowers the current limit value. Due to circuit tolerance this I<sub>SET</sub> resistor should not be less than 2k. In order to match the temperature variation of the sense resistor, the voltage on this pin is proportional to temperature of the MOSFET switch.

**OUT:** Output of Internal MOSFET Switch. Connect this pin directly to the load.

**OV:** Overvoltage Comparator Input. Connect this pin to an external resistive divider from V<sub>DD</sub>. If the voltage at this pin rises above 1.235V, an overvoltage is detected and the switch turns off. Tie to GND if unused.

**PG:** Power Good Indicator. Open-drain output pulls low when the FB pin drops below 1.21V indicating the power is bad. If the voltage at FB rises above 1.235V and the GATE-to-OUT voltage exceeds 4.2V, the open-drain pull-down releases the PG pin to go high.

**SENSE:** Current Sense Node and MOSFET Drain. One exposed pad on the UH package is connected to SENSE and should be soldered to an electrically isolated printed circuit board trace to properly transfer the heat out of the package. The two SENSE pins (Pins 8, 31) on opposite sides of the package are used for testing purposes and for driving the SENSE<sup>-</sup> pin (connect Pin 34 to Pin 31).

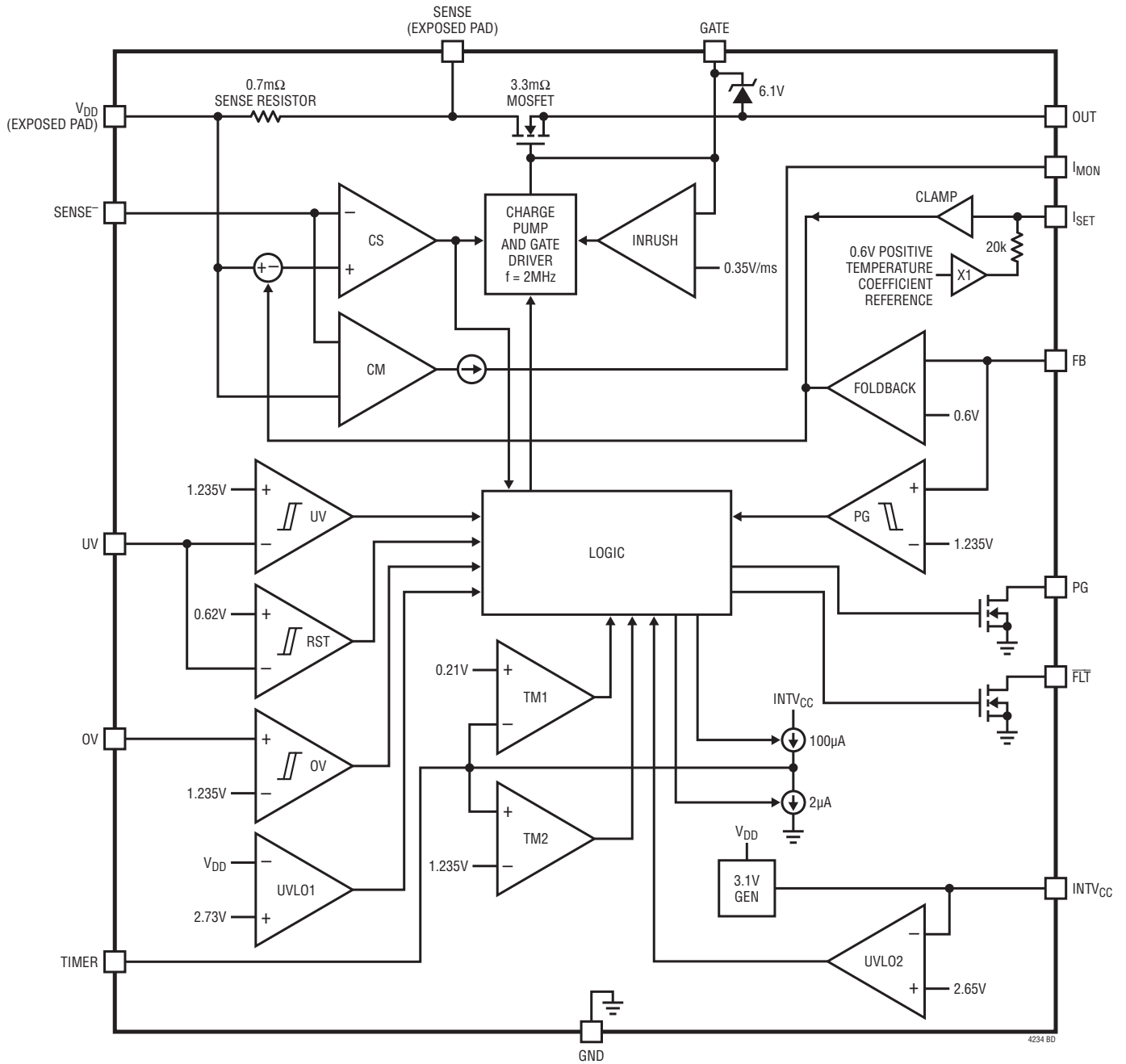
**SENSE<sup>-</sup>:** Current Limit and Current Monitor Amplifier Input. The current limit circuit controls the GATE pin to limit the voltage between the V<sub>DD</sub> and SENSE<sup>-</sup> pins to 15mV (22.5A) or less depending on the voltage at the FB pin. This pin must be connected to SENSE pin on the right side (connect Pin 34 to Pin 31).

**TIMER:** Current Limit Timer Input. Connect a capacitor between this pin and ground to set a 12ms/ $\mu$ F duration for current limit before the switch is turned off. If the UV pin is toggled low while the MOSFET switch is off, the switch will turn on again following cool down time of 4.14s/ $\mu$ F duration. Tie this pin to INTV<sub>CC</sub> for a fixed 2ms overcurrent delay and 900ms cool down time.

**UV:** Undervoltage Comparator Input. Tie high (e.g., to INTV<sub>CC</sub>) if unused. Connect this pin to an external resistive divider from V<sub>DD</sub>. If the UV pin voltage falls below 1.15V, an undervoltage is detected and the switch turns off. Pulling this pin below 0.62V resets the overcurrent fault and allows the switch to turn back on (see Application Information section for details). If overcurrent auto-retry is desired then tie this pin to the FLT pin.

**V<sub>DD</sub>:** Supply Voltage and Current Sense Input. This exposed pad on the UH package must be soldered to input power. The two V<sub>DD</sub> (NC) pins (Pins 6, 33) on opposite sides of the package are used for testing purposes only and should be left unconnected. This pad has an undervoltage lockout threshold of 2.73V.

## FUNCTIONAL DIAGRAM



4234 BD

## OPERATION

The Functional Diagram displays the main circuits of the device. The LTC4234 is designed to turn a board's supply voltage on and off in a controlled manner allowing the board to be safely inserted and removed from a live backplane. The LTC4234 includes a  $3.3\text{m}\Omega$  MOSFET and a  $0.7\text{m}\Omega$  current sense resistor. During normal operation, the charge pump and gate driver turn on the pass MOSFET's gate to provide power to the load. The inrush current control is accomplished by the INRUSH circuit. This circuit limits the GATE ramp rate to  $0.35\text{V/ms}$  and hence controls the voltage ramp rate of the output capacitor.

The current sense (CS) amplifier monitors the load current using the voltage sensed across the current sense resistor. The CS amplifier limits the current in the load by reducing the GATE-to-OUT voltage in an active control loop. It is simple to adjust the current limit threshold using the current setting ( $I_{\text{SET}}$ ) pin. This allows a different threshold during other times such as start-up. Note there must be a connection between SENSE to SENSE<sup>-</sup> (Pin 34 to Pin 31) in order to monitor current.

A short circuit on the output to ground causes significant power dissipation during active current limiting. To limit this power, the foldback amplifier reduces the current limit value from  $22.5\text{A}$  to  $5.7\text{A}$  in a linear manner as the FB pin drops below  $0.6\text{V}$  (see the Typical Performance Characteristics).

If an overcurrent condition persists, the TIMER pin ramps up with a  $100\mu\text{A}$  current source until the pin voltage exceeds  $1.235\text{V}$  (comparator TM2). This indicates to the logic that it is time to turn off the pass MOSFET to prevent overheating. At this point the TIMER pin ramps down

using the  $2\mu\text{A}$  current source until the voltage drops below  $0.21\text{V}$  (Comparator TM1) which completes one timer cycle. After eight TIMER pin cycles (ramping to  $1.235\text{V}$  and then below  $0.21\text{V}$ ) the logic starts the internal  $48\text{ms}$  timer. At this point, the pass transistor has cooled and it is safe to turn it on again. It is suitable in many applications to use an internal  $2\text{ms}$  overcurrent timer with a  $900\text{ms}$  cool down period. Tying the TIMER pin to INTV<sub>CC</sub> sets this default timing.

The output voltage is monitored using the FB pin and the PG comparator to determine if power is available for the load. The power good condition is signaled by the PG pin using an open-drain pull-down transistor.

The Functional Diagram shows the monitoring blocks of the LTC4234. The two comparators on the left side include the UV and OV comparators. These comparators are used to determine if the external conditions are valid prior to turning on the MOSFET. But first the undervoltage lockout circuits UVLO1 and UVLO2 must validate the input supply and the internally generated  $3.1\text{V}$  supply (INTV<sub>CC</sub>) and generate the power up initialization to the logic circuits. If the external conditions remain valid for  $48\text{ms}$  the MOSFET is allowed to turn on.

Other monitoring features include the MOSFET current and temperature monitoring. The current monitor (CM) outputs a current proportional to the sense resistor current. This current can drive an external resistor or other circuits for monitoring purposes. A voltage proportional to the MOSFET temperature is output to the  $I_{\text{SET}}$  pin. The MOSFET temperature allows external circuits to predict failure and shutdown the system.



## APPLICATIONS INFORMATION

allows the inrush current to stay under the folded back current limit threshold (5.7A) for capacitors less than 10mF. Included in the Typical Performance Characteristics section is a graph of the Safe Operating Area for the MOSFET. It is evident from this graph that the power dissipation at 12V, 350mA for 34ms is in the safe region.

Adding a capacitor and a 100k series resistor from GATE to ground will lower the inrush current below the default value set by the INRUSH circuit. The 3.3nF capacitor,  $C_{COMP}$ , is necessary to compensate the current limit regulation loop when the  $R_{GATE}$  and  $C_{GATE}$  network is on the GATE pin. The GATE is charged with a 24 $\mu$ A current source (when the INRUSH circuit is not driving the GATE). The voltage at the GATE pin rises with a slope equal to 24 $\mu$ A/ $C_{GATE}$  and the supply inrush current is set at:

$$I_{INRUSH} = \frac{C_L}{C_{GATE}} \cdot 24\mu A$$

When the GATE voltage reaches the MOSFET threshold voltage, the switch begins to turn on and the OUT voltage follows the GATE voltage as it increases. Once OUT reaches  $V_{DD}$ , the GATE will ramp up until clamped by the 6.1V Zener between GATE and OUT.

As the OUT voltage rises, so will the FB pin which is monitoring it. Once the FB pin crosses its 1.235V threshold

and the GATE to OUT voltage exceeds 4.2V, the PG pin will cease to pull low and indicate that the power is good.

### Parasitic MOSFET Oscillation

When the N-channel MOSFET ramps up the output during power-up it operates as a source follower. The source follower configuration may self-oscillate in the range of 25kHz to 300kHz when the load capacitance is less than 10 $\mu$ F, especially if the wiring inductance from the supply to  $V_{DD}$  pin is greater than 3 $\mu$ H. The possibility of oscillations will increase as the load current (during power-up) increases. There are two ways to prevent this type of oscillation. The simplest way is to avoid load capacitances below 10 $\mu$ F. For wiring inductances larger than 20 $\mu$ H, the minimum load capacitances may extend to 100 $\mu$ F. A second choice is to connect an external gate capacitor  $C_p > 1.5$ nF as shown in Figure 3.

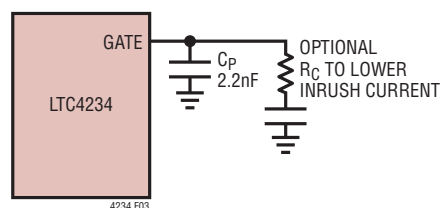


Figure 3. Compensation for Small  $C_{LOAD}$

## APPLICATIONS INFORMATION

### Turn-Off Sequence

The switch can be turned off by a variety of conditions. A normal turn-off is initiated by the UV pin going below its 1.235V threshold. Additionally, several fault conditions will turn off the switch. These include an input overvoltage (OV pin), overcurrent circuit breaker (SENSE<sup>-</sup> pin) or overtemperature. Normally the switch is turned off with a 250μA current pulling down the GATE pin to ground. With the switch turned off, the OUT voltage drops which pulls the FB pin below its threshold. The PG then pulls low to indicate output power is no longer good.

If V<sub>DD</sub> drops below 2.65V for greater than 5μs or INTV<sub>CC</sub> drops below 2.5V for greater than 1μs, a fast shut down of the switch is initiated. The GATE is pulled down with a 140mA current to the OUT pin.

### Overcurrent Fault

The LTC4234 features an adjustable current limit with foldback that protects against short circuits or excessive load current. To protect against excessive power dissipation in the switch during active current limit, the available current is reduced as a function of the output voltage sensed by the FB pin. A graph in the Typical Performance Characteristics curves shows the Current Limit Threshold Foldback.

An overcurrent fault occurs when the current limit circuitry has been engaged for longer than the timeout delay set by the TIMER. Current limiting begins when the MOSFET current reaches 5.7A to 22.5A (depending on the foldback).

The GATE pin is then brought down with a 140mA GATE-to-OUT current. The voltage on the GATE is regulated in order to limit the current to 22.5A. At this point, a circuit breaker time delay starts by charging the external timing capacitor from the TIMER pin with a 100μA pull-up current. If the TIMER pin reaches its 1.235V threshold, the internal switch turns off (with a 250μA current from GATE to ground). Included in the Typical Performance Characteristics curves is a graph of the Safe Operating Area for the MOSFET. From this graph one can determine the MOSFET's maximum time in current limit for a given output power.

Tying the TIMER pin to INTV<sub>CC</sub> will force the part to use the internally generated (circuit breaker) delay of 2ms. In either case the  $\overline{\text{FLT}}$  pin is pulled low to indicate an overcurrent fault has turned off the pass MOSFET. For a given circuit breaker time delay, the equation for setting the timing capacitor's value is as follows:

$$C_T = t_{CB} \cdot 0.083(\mu\text{F}/\text{ms})$$

After the switch is turned off, the TIMER pin begins discharging the timing capacitor with a 2μA pull-down current. When the TIMER pin reaches its 0.21V threshold, it completes one timer cycle. After eight TIMER pin cycles (ramping to 1.235V and then below 0.21V) plus the 48ms debounce time, the switch is allowed to turn on again if the overcurrent fault has been cleared. Bringing the UV pin below 0.6V and then high will clear the fault. If the TIMER pin is tied to INTV<sub>CC</sub> then the switch is allowed to turn on again (after an internal 900ms cool down time plus the 48ms debounce time) if the overcurrent fault is cleared.

## APPLICATIONS INFORMATION

Tying the  $\overline{\text{FLT}}$  pin to the UV pin allows the part to self-clear the fault and turn the MOSFET on as soon as TIMER pin has ramped below 0.21V for the eighth time followed by the 48ms debounce time. In this auto-retry mode the LTC4234 repeatedly tries to turn on after an overcurrent at a period determined by the capacitor on the TIMER pin. The auto retry mode also functions when the TIMER pin is tied to INTV<sub>CC</sub>.

The waveform in Figure 4 shows how the output latches off following a short-circuit. The current in the MOSFET is 5.7A as the TIMER pin ramps up.

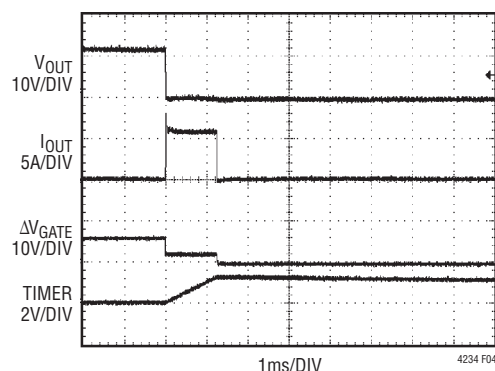


Figure 4. Short-Circuit Waveform

### Current Limit Adjustment

The default value of the active current limit is 22.5A. The current limit threshold can be adjusted lower by placing a resistor between the I<sub>SET</sub> pin and ground. As shown in the Functional Diagram the voltage at the I<sub>SET</sub> pin (via the clamp circuit) sets the CS amplifier's built-in offset voltage. This offset voltage directly determines the active current limit value. With the I<sub>SET</sub> pin open, the voltage at the I<sub>SET</sub> pin is determined by a positive temperature coefficient reference. This voltage is set to 0.618V which corresponds to a 22.5A current limit at room temperature.

An external resistor placed between the I<sub>SET</sub> pin and ground forms a resistive divider with the internal 20k sourcing resistor. The divider acts to lower the voltage at the I<sub>SET</sub> pin and therefore lower the current limit threshold. The overall current limit threshold precision is reduced to  $\pm 15\%$  when using a 20k resistor to halve the threshold.

Using a switch (connected to ground) in series with this external resistor allows the active current limit to change only when the switch is closed. This feature can be used when the start-up current exceeds the typical maximum load current.

## APPLICATIONS INFORMATION

### Monitor MOSFET Temperature

The voltage at the  $I_{SET}$  pin increases linearly with increasing temperature. The temperature profile of the  $I_{SET}$  pin is shown in the Typical Performance Characteristics section. Using a comparator or ADC to measure the  $I_{SET}$  voltage provides an accurate indication of the MOSFET temperature.

There is an overtemperature circuit in the LTC4234 that monitors an internal voltage similar to the  $I_{SET}$  pin voltage. When the die temperature exceeds  $155^{\circ}\text{C}$  the circuit turns off the MOSFET until the temperature drops to  $135^{\circ}\text{C}$ .

### Monitor MOSFET Current

The current in the MOSFET passes through a sense resistor. The voltage on the sense resistor is converted to a current that is sourced out of the  $I_{MON}$  pin. The gain of  $I_{SENSE}$  amplifier is  $5\mu\text{A}/\text{A}$  referenced from the MOSFET current. This output current can be converted to a voltage using an external resistor to drive a comparator or ADC. The voltage compliance for the  $I_{MON}$  pin is from  $0\text{V}$  to  $\text{INTV}_{CC} - 0.7\text{V}$ .

A microcontroller with a built-in comparator can build a simple integrating single-slope ADC by resetting a capacitor that is charged with this current. When the capacitor voltage trips the comparator and the capacitor is reset, a timer is started. The time between resets will indicate the MOSFET current.

### Monitor OV and UV Faults

Protecting the load from an overvoltage condition is the main function of the OV pin. In Figure 1 an external resistive divider (driving the OV pin) connects to a comparator to turn off the MOSFET when the  $V_{DD}$  voltage exceeds  $15.2\text{V}$ . If the  $V_{DD}$  pin subsequently falls back below  $14.9\text{V}$ , the switch will be allowed to turn on immediately. In the LTC4234 the OV pin threshold is  $1.235\text{V}$  when rising, and  $1.215\text{V}$  when falling out of overvoltage.

The UV pin functions as an undervoltage protection pin or as an “ON” pin. In the Figure 1 application the MOSFET turns off when  $V_{DD}$  falls below  $9.23\text{V}$ . If the  $V_{DD}$  pin subsequently rises above  $9.88\text{V}$  for  $48\text{ms}$ , the switch will be allowed to turn on again. The LTC4234 UV turn-on/off threshold are  $1.235\text{V}$  (rising) and  $1.155\text{V}$  (falling).

In the case of an undervoltage or overvoltage, the MOSFET turns off and there is indication on the PG status pin. When the overvoltage is removed, the MOSFET’s gate ramps up immediately at the rate determined by the INRUSH circuit.

### Power Good Indication

In addition to setting the foldback current limit threshold, the FB pin is used to determine a power good condition. The Figure 1 application uses an external resistive divider on the OUT pin to drive the FB pin. On the LTC4234 the PG comparator drives high when the FB pin rises above  $1.235\text{V}$  and low when falls below  $1.215\text{V}$ .

Once the PG comparator is high the GATE pin voltage is monitored with respect to the OUT pin. Once the GATE minus OUT voltage exceeds  $4.2\text{V}$  the PG pin goes high. This indicates to the system that it is safe to load the OUT pin while the MOSFET is completely turned “on”. The PG pin goes low when the GATE is commanded off (using the UV, OV or  $\text{SENSE}^-$  pins) or when the PG comparator drives low.

### Design Example

Consider the following design example (Figure 5):  $T_A = 60^{\circ}\text{C}$ ,  $V_{IN} = 12\text{V}$ ,  $I_{MAX} = 20\text{A}$ .  $I_{INRUSH} = 350\text{mA}$ ,  $C_L = 1000\mu\text{F}$ ,  $V_{UVON} = 9.88\text{V}$ ,  $V_{OVOFF} = 15.2\text{V}$ ,  $V_{PWRGD} = 10.5\text{V}$ . A current limit fault triggers an automatic restart of the power-up sequence.

## APPLICATIONS INFORMATION

The inrush current is defined by the current required to charge the output capacitor using the fixed 0.35V/ms GATE charge up rate. The inrush current is defined as:

$$I_{\text{INRUSH}} = C_L \cdot \left( \frac{0.35\text{V}}{\text{ms}} \right) = 1000\mu\text{F} \cdot \left( \frac{0.35\text{V}}{\text{ms}} \right) = 350\text{mA}$$

As mentioned previously the charge-up time is the output voltage (12V) divided by the output rate of 0.35V/ms resulting in 34ms. The peak power dissipation of 12V at 350mA (or 4.2W) is within the SOA of the pass MOSFET for 34ms (see MOSFET SOA curve in the Typical Performance Characteristics).

Next the power dissipated in the MOSFET during overcurrent must be limited. The active current limit uses a timer

to prevent excessive energy dissipation in the MOSFET. The worst-case power dissipation occurs when the voltage versus current profile of the foldback current limit is at the maximum. This occurs when the current is 25A and the voltage is one-half of the 12V or 6V. See the Current Limit Threshold Foldback in the Typical Performance Characteristics section to view this profile. In order to survive 150W, the MOSFET SOA dictates a maximum current limit timeout. The room temperature SOA graph presents a series of lines where the power (voltage times current) and time follow a constant  $P^2t$  relationship of 500  $\text{W}^2\text{-s}$ . If the MOSFET operating temperature is elevated prior to current limit the SOA constant must be derated as shown in Figure 6.

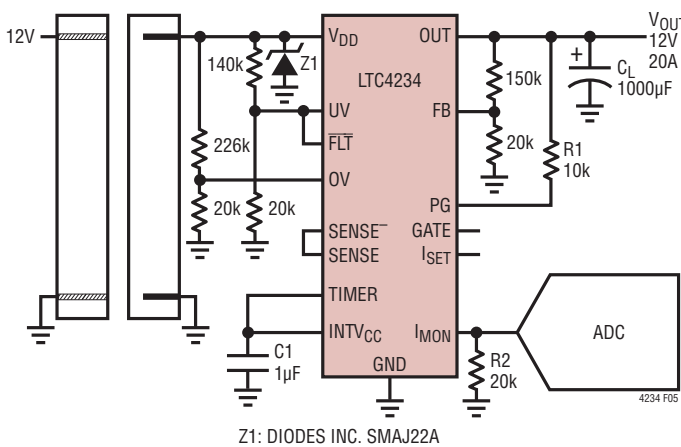


Figure 5. 20A, 12V Card Resident Application

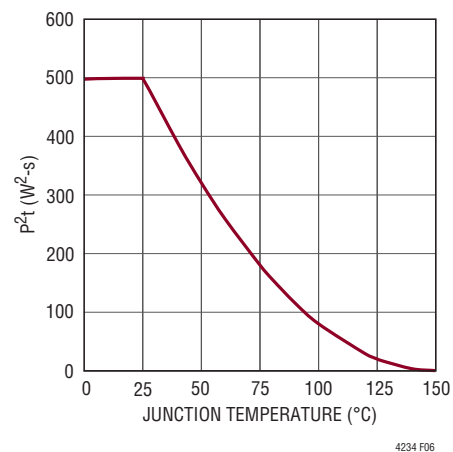


Figure 6. SOA Constant vs Junction Temperature

## APPLICATIONS INFORMATION

The operating temperature is calculated from the ambient temperature, package thermal impedance ( $R_{\theta JA}$ ) and the  $I^2R$  heating:

$$T_J = (R_{\theta JA} \cdot I^2 \cdot R_{ON}) + T_A = 15^\circ\text{C/W} \cdot (20\text{A})^2 \cdot 7.2\text{m}\Omega + 60^\circ\text{C} = 103^\circ\text{C}$$

and the SOA constant is derated to  $71\text{ W}^2\text{-s}$ . The maximum current limit timeout is calculated from the revised constant and the  $150\text{ W}$  dissipated in current limit:

$$t_{\text{MAX}} = \frac{P^2 t(T_J = 103^\circ\text{C})}{P^2} = \frac{71\text{W}^2\text{-S}}{(150\text{W})^2} = 3.2\text{ms}$$

Use the internal 2ms timer invoked by tying the TIMER pin to  $\text{INTV}_{\text{CC}}$ . After the 2ms timeout the  $\overline{\text{FLT}}$  pin needs to pull down on the UV pin restart the power-up sequence.

The values for overvoltage, undervoltage and power good thresholds using the resistive dividers on the UV, OV and FB pins match the requirements of turn-on at  $9.88\text{V}$  and turn-off at  $15.2\text{V}$ .

The final schematic in Figure 5 results in very few external components. The pull-up resistor, R1, connects to the PG pin while the  $20\text{k}$  (R2) converts the  $I_{\text{MON}}$  current to a voltage at a ratio:

$$V_{\text{IMON}} = 5[\mu\text{A/A}] \cdot 20\text{k} \cdot I_{\text{OUT}} = 0.1[\text{V/A}] \cdot I_{\text{OUT}}$$

In addition there is a  $1\mu\text{F}$  bypass (C1) on the  $\text{INTV}_{\text{CC}}$  pin and note the connection between SENSE to SENSE<sup>-</sup> (Pin 34 to Pin 31).

### Layout Considerations

In Hot Swap applications where load currents can be  $20\text{A}$ , narrow PCB tracks exhibit more resistance than wider tracks and operate at elevated temperatures. The minimum trace

width requirement for 1oz copper foil is  $0.02\text{''}$  per amp to make sure the trace stays at a reasonable temperature. Using  $0.03\text{''}$  per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about  $0.5\text{m}\Omega/\text{square}$ . Small resistances add up quickly in high current applications.

The input supply should be tied to  $V_{\text{DD}}$  exposed pad through a PCB trace that enters between Pin 1 and Pin 38. The  $V_{\text{DD}}$  pad connects to the sense resistor and MOSFET. The two  $V_{\text{DD}}$  (NC) Pins (6, 33) on opposite sides of the package are used for testing purposes only and should be left unconnected. Likewise the two SENSE Pins (8, 31) on opposite sides are used for testing and for driving the SENSE<sup>-</sup> pin (connect Pin 34 to Pin 31). Figure 7 shows a recommended layout for the LTC4234.

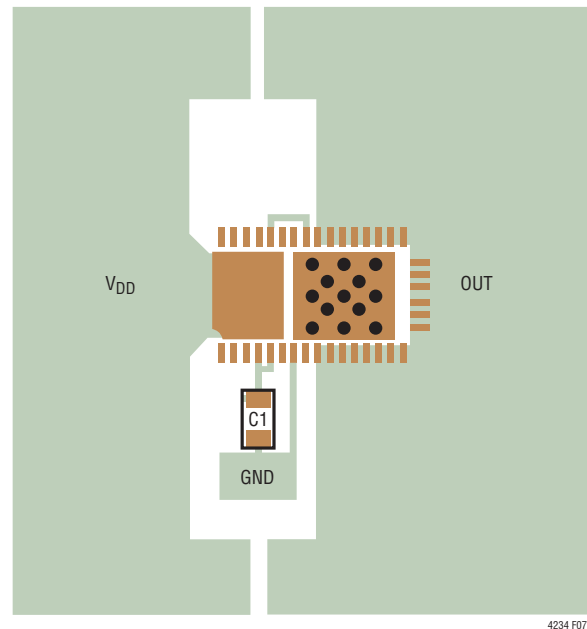


Figure 7. Recommended Layout

## APPLICATIONS INFORMATION

During normal loads the power dissipated in the MOSFET is as high as 2.9W. Although the MOSFET is self protected from overtemperature, it is recommended to solder the SENSE exposed pad to a copper trace that contains vias underneath the pad. Include area of 1oz copper on the OUT pins for additional heat sinking. Since the trace that connects OUT pins must accommodate high current, this area of copper is usually present. It is also important to put C1, the bypass capacitor for the INTV<sub>CC</sub> pin as close as possible between INTV<sub>CC</sub> and GND.

### Thermal Considerations

The LTC4234 junction temperature rise in still air when the load current is 10A, 15A and 20A is shown in curves of Figure 8 and Figure 9. This temperature rise falls as the board area is increases from 6.45cm<sup>2</sup> to 103cm<sup>2</sup>. Two different SENSE pad areas are shown as separate figures.

This thermal test board uses 2oz copper on the top layer divided equally between V<sub>DD</sub> and OUT traces similar to Figure 7. The second layer is 1oz copper connected to the vias to the SENSE pad on the top layer. Two versions of the second layer are considered. One uses a minimum sized SENSE pad that only covers the vias for the top layer while the remainder of the second layer is empty (see Figure 8). The other version fills the second layer with SENSE connected copper (see Figure 9). The third layer is 1oz copper tied to ground while the bottom layer is 2oz copper tied to ground except for a few signal traces.

The curves demonstrate that the heat from the MOSFET can be effectively transferred out of the package through the OUT pins and only requires a minimum sized SENSE pad under the package. However for small boards the larger SENSE area does reduce the junction temperature when sourcing higher currents.

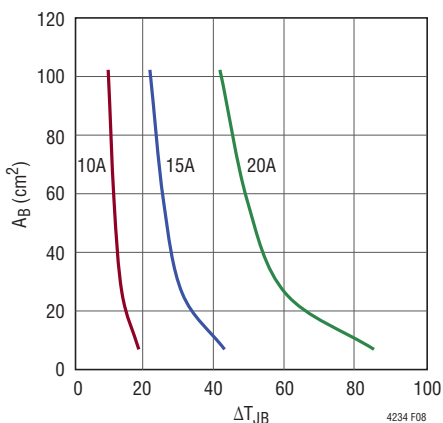


Figure 8. Temperature Rise for Small SENSE Pad

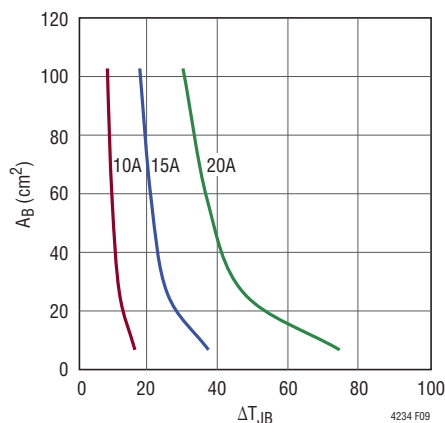


Figure 9. Temperature Rise for Large SENSE Pad

## APPLICATIONS INFORMATION

### Additional Applications

The LTC4234 has a wide operating range from 2.9V to 15V. The UV, OV and PG thresholds are set with few resistors. All other functions are independent of supply voltage.

In addition to Hot Swap applications, the LTC4234 also functions as a backplane resident switch for removable load cards (see Figure 10).

Figure 11 shows a 3.3V application with a UV threshold of 2.87V, an OV threshold of 3.77V and a PG threshold of 3.05V.

The last page shows a 40A parallel application where the two LTC4234 parts each provide 20A to the load. The PNPs prevent one LTC4234 from faulting off in current limit until both parts hit the 22.5A limit. The PNPs are disconnected when power good is false via the series MOSFETs M1 and M2

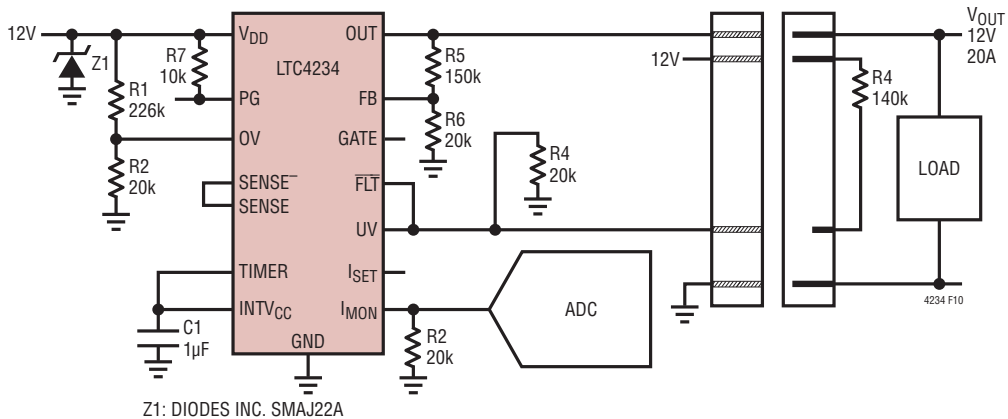


Figure 10. 12V, 20A Backplane Resident Application with Insertion Activated Turn-On

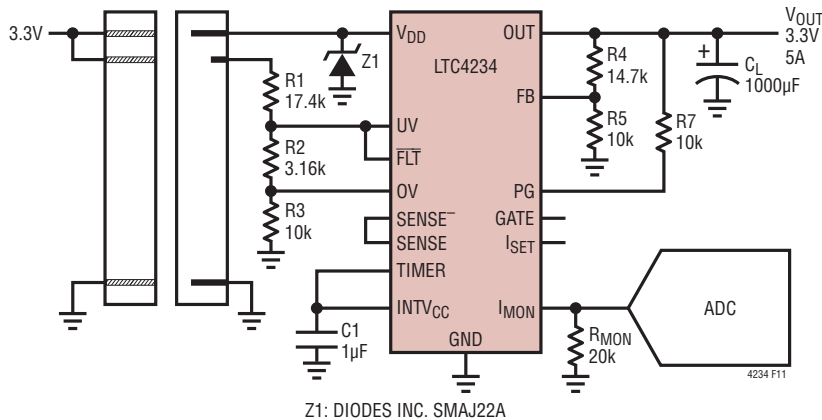
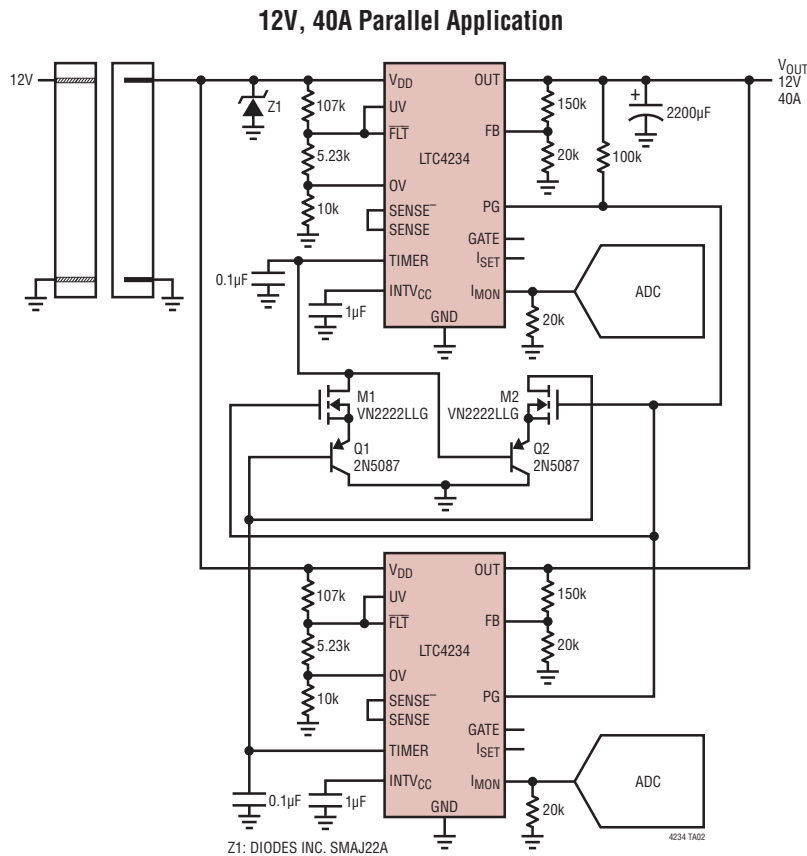


Figure 11. 3.3V, 20A Card Resident Application with Auto-Retry



## TYPICAL APPLICATION



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
<a href="#">LTC4210</a>	Single Channel Hot Swap Controller	Operates from 2.7V to 16.5V, Active Current Limiting, SOT23-6
<a href="#">LTC4211</a>	Single Channel Hot Swap Controller	Operates from 2.5V to 16.5V, Multifunction Current Control, MSOP-8 or MSOP-10
<a href="#">LTC4215</a>	Hot Swap Controller with I <sup>2</sup> C Compatible Monitoring	Operates from 2.9V to 15V, 8-Bit ADC Monitors Current and Voltage
<a href="#">LTC4217</a>	2A Integrated Hot Swap Controller	Operates from 2.9V to 26.5V, Adjustable 5% Accurate Current Limit
<a href="#">LTC4218</a>	Hot Swap Controller with 5% Accurate 15mV Current Limit	Operates from 2.9V to 26.5V, Adjustable Current Limit, SSOP-16, DFN-16
<a href="#">LTC4219</a>	5A Integrated Hot Swap Controller	12V and 5V Preset Versions, 10% Accurate Current Limit
<a href="#">LTC4221</a>	Dual Hot Swap Controller/Sequencer	Operates from 1V to 13.5V, Multifunction Current Control, SSOP-16
<a href="#">LTC4227</a>	Dual Ideal Diode and Single Hot Swap Controller	Operates from 2.9V to 18V, PowerPath™ and Inrush Current Control for Redundant Supplies
<a href="#">LTC4228</a>	Dual Ideal Diode and Hot Swap Controller	Operates from 2.9V to 18V, PowerPath and Inrush Current Control for MicroTCA, Redundant Supplies and Supply Holdup
<a href="#">LTC4232</a>	5A Integrated Hot Swap Controller	Operates from 2.9V to 15V, Adjustable 10% Accurate Current Limit