

FEATURES

Fast

- Slew Rate 50V/ μ s Min
- Settling-Time (0.01%) 1 μ s Max
- Gain-Bandwidth Product 10MHz Typ

Precise

- Common-Mode Rejection 88dB Min
- Open-Loop Gain 500V/mV Min
- Offset Voltage 750 μ V Max
- Bias Current 200pA Max

Excellent Radiation Hardness

Available in Die Form

ORDERING INFORMATION [†]

$T_A = 25^\circ\text{C}$ $V_{OS} \text{ MAX}$ (mV)	PACKAGE					OPERATING TEMPERATURE RANGE
	TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	SO 8-PIN	LCC 20-CONTACT	
1.0	OP42AJ*	OP42AZ*	—	—	OP42ARC/883	MIL
0.75	OP42EJ	OP42EZ	—	—	—	IND
1.5	OP42FJ	OP42FZ	—	—	—	IND
5.0	—	—	OP42GP	OP42GS	—	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

[†] Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages.

GENERAL DESCRIPTION

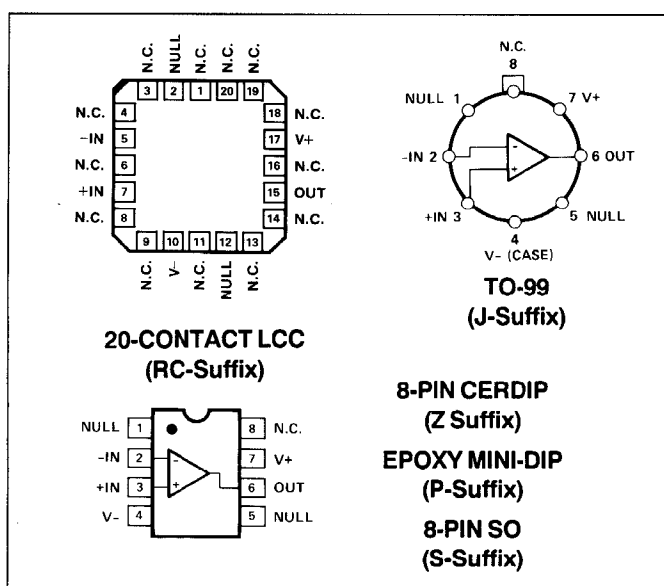
The OP-42 is a fast precision JFET-input operational amplifier. Similar in speed to the OP-17, the OP-42 offers a symmetric

58V/ μ s slew rate and is internally compensated for unity-gain operation. OP-42 speed is achieved with a supply current of less than 6mA. Unity-gain stability, a wide full-power bandwidth of 900kHz, and a fast settling-time of 800ns to 0.01% make the OP-42 an ideal output amplifier for fast digital-to-analog converters.

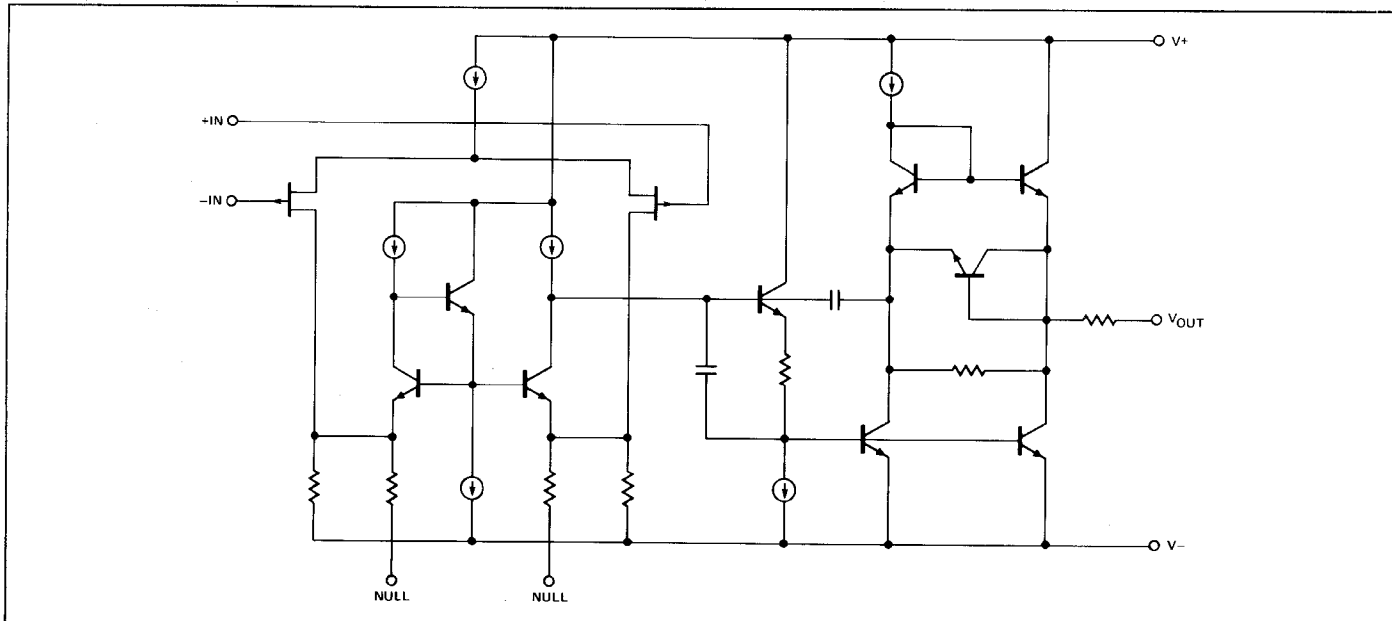
Equal attention was given to both speed and precision in the OP-42 design. Its tight 750 μ V maximum input offset voltage combined with well-controlled drift of less than 10 μ V/ $^\circ$ C eliminates the need for external nulling in many circuits. The OP-42's

Continued

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



OP-42

GENERAL DESCRIPTION *Continued*

common-mode rejection of 88dB minimum over a $\pm 11\text{V}$ input voltage range is exceptional for a high-speed amplifier. High CMR combined with a minimum 500V/mV gain into 10k Ω load ensure excellent linearity in both noninverting and inverting gain configurations. The low input bias and offset currents provided by the JFET input stage suit the OP-42 for use in high-speed sample and hold circuits, peak detectors, and log amplifiers. Excellent radiation hardness characteristics make the OP-42 ideal for military and aerospace applications.

The OP-42 conforms to the standard 741 pinout with nulling to V₋. The OP-42 upgrades the performance of circuits using the AD544, AD611, AD711, and LF400 by direct replacement. In circuits without nulling, the OP-42 offers an upgrade for designs using the OP-16, OP-17, LT1022, LT1056, and HA2510.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	$\pm 20\text{V}$
Input Voltage (Note 2)	$\pm 20\text{V}$
Differential Input Voltage (Note 2)	40V
Output Short-Circuit Duration	Indefinite

Storage Temperature Range -65°C to $+175^{\circ}\text{C}$

Operating Temperature Range

OP42A (J, Z) -55°C to $+125^{\circ}\text{C}$

OP42E, F (J, Z) -25°C to $+85^{\circ}\text{C}$

OP42G -40°C to $+85^{\circ}\text{C}$

Junction Temperature -65°C to $+175^{\circ}\text{C}$

Lead Temperature Range (Soldering, 60 sec.) $+300^{\circ}\text{C}$

PACKAGE TYPE	θ_{JA} (NOTE 3)	θ_{JC}	UNITS
TO-99 (J)	150	18	$^{\circ}\text{C/W}$
8-Pin Hermetic DIP (Z)	148	16	$^{\circ}\text{C/W}$
8-Pin Plastic DIP (P)	103	43	$^{\circ}\text{C/W}$
20-Contact LCC (RC, TC)	98	38	$^{\circ}\text{C/W}$
8-Pin SO (S)	158	43	$^{\circ}\text{C/W}$

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. For supply voltages less than $\pm 20\text{V}$, the absolute maximum input voltage is equal to the supply voltage.
3. θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, CERDIP, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15\text{V}$, $T_A = +25^{\circ}\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-42E			OP-42F			OP-42G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}		—	0.3	0.75	—	0.4	1.5	—	1.5	5.0	mV
Input Bias Current	I_B	$V_{CM} = 0\text{V}$ $T_J = 25^{\circ}\text{C}$	—	80	200	—	130	250	—	130	250	pA
Input Offset Current	I_{OS}	$V_{CM} = 0\text{V}$ $T_J = 25^{\circ}\text{C}$	—	4	40	—	6	50	—	6	50	pA
Input Voltage Range	IVR	(Note 1)	± 11	$+12.5$ -12.0	—	± 11	$+12.5$ -12.0	—	± 11	$+12.5$ -12.0	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11\text{V}$	88	98	—	80	92	—	80	92	—	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 10\text{V}$ to $\pm 20\text{V}$	—	9	40	—	12	50	—	12	50	$\mu\text{V/V}$
Large-Signal Voltage Gain	A_{VO}	$R_L = 10\text{k}\Omega$	500	900	—	500	900	—	500	900	—	V/mV
		$R_L = 2\text{k}\Omega$	200	260	—	200	260	—	200	260	—	
		$R_L = 1\text{k}\Omega$	100	170	—	100	170	—	100	170	—	
Output Voltage Swing	V_O	$R_L = 1\text{k}\Omega$	± 11.5	$+12.5$ -11.9	—	± 11.5	$+12.5$ -11.9	—	± 11.5	$+12.5$ -11.9	—	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	± 20	$+33$ -28	± 60	± 20	$+33$ -28	± 60	± 20	$+33$ -28	± 60	mA
Supply Current	I_{SY}	No Load $V_O = 0\text{V}$	—	5.1	6.0	—	5.1	6.5	—	5.1	6.5	mA
Slew Rate	SR		50	58	—	40	50	—	40	50	—	V/ μs
Full-Power Bandwidth	BW_p	(Note 2)	750	900	—	600	800	—	600	800	—	kHz
Gain-Bandwidth Product	GBW	$f_o = 10\text{kHz}$	—	10	—	—	10	—	—	10	—	MHz
Settling Time	t_s	10V Step 0.01% (Note 3)	—	0.8	1.0	—	0.9	1.2	—	0.9	1.2	μs
Overload Recovery Time	t_{OR}		—	700	—	—	700	—	—	700	—	ns
Phase Margin	ϕ_o	0db Gain	—	47	—	—	47	—	—	47	—	degrees
Gain Margin	A_{180}	180° Open-Loop Phase Shift	—	9	—	—	9	—	—	9	—	dB
Capacitive Load Drive Capability	C_L	Unity-Gain Stable (Note 4)	100	300	—	100	300	—	100	300	—	pF

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-42E			OP-42F			OP-42G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Differential Input Impedance	Z_{IN}		—	$10^{12} 6$	—	—	$10^{12} 6$	—	—	$10^{12} 6$	—	ΩpF
Open-Loop Output Resistance	R_O		—	50	—	—	50	—	—	50	—	Ω
Voltage Noise	$e_{n\ p-p}$	0.1Hz to 10Hz	—	2	—	—	2	—	—	2	—	μV_{p-p}
Voltage Noise Density	e_n	$f_O = 10Hz$	—	38	—	—	38	—	—	38	—	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	—	16	—	—	16	—	—	16	—	
		$f_O = 1kHz$	—	13	—	—	13	—	—	13	—	
		$f_O = 10kHz$	—	12	—	—	12	—	—	12	—	
Current Noise Density	i_n	$f_O = 1kHz$	—	0.007	—	—	0.007	—	—	0.007	—	$pA/\sqrt{Hz}$
External V_{OS} Trim Range		$R_{pot} = 20k\Omega$	—	4	—	—	4	—	—	4	—	mV
Long-Term V_{OS} Drift			—	5	—	—	5	—	—	5	—	$\mu V/month$
Supply Voltage Range	V_S		± 8	± 15	± 20	± 8	± 15	± 20	± 8	± 15	± 20	V

NOTES:

1. Guaranteed by CMR test.
2. Guaranteed by slew-rate test and formula $BW_p = SR/(2\pi 10V_{PEAK})$.
3. Settling-time is sample tested for A and E grades. Test circuit is shown in Figure 4. Settling-time for F grade is guaranteed but not tested.
4. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	OP-42A		UNITS
				TYP	MAX	
Offset Voltage	V_{OS}		—	0.3	1.0	mV
Input Bias Current	I_B	$V_{CM} = 0V$ $T_J = 25^\circ C$	—	80	200	pA
Input Offset Current	I_{OS}	$V_{CM} = 0V$ $T_J = 25^\circ C$	—	4	40	pA
Input Voltage Range	IVR	(Note 1)	± 11	+12.5 -12.0	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	86	96	—	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	—	9	40	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$ $V_O = \pm 10V$	500	900	—	V/mV
		$R_L = 2k\Omega$ $T_J = 25^\circ C$	200	260	—	
		$R_L = 1k\Omega$	100	170	—	
Output Voltage Swing	V_O	$R_L = 1k\Omega$	± 11.5	+12.5 -11.9	—	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	± 20	+33 -28	± 60	mA
Supply Current	I_{SY}	No Load $V_O = 0V$	—	5.1	6.0	mA
Slew Rate	SR		45	52	—	V/ μs
Full-Power Bandwidth	BW_p	(Note 2)	700	850	—	kHz
Gain-Bandwidth Product	GBW	$f_O = 10kHz$	—	10	—	MHz
Settling -Time	t_s	10V Step 0.01% (Note 3)	—	0.8	1.0	μs
Overload Recovery Time	t_{OR}		—	700	—	ns
Phase Margin	ϕ_o	0db Gain	—	47	—	degrees

OP-42

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	MIN	OP-42A TYP	MAX	UNITS
Gain Margin	A_{180}	180° Open-Loop Phase Shift	—	9	—	dB
Capacitive Load Drive Capability	C_L	Unity-Gain Stable (Note 4)	100	300	—	pF
Differential Input Impedance	Z_{IN}		—	$10^{12} 6$	—	ΩpF
Open-Loop Output Resistance	R_O		—	50	—	Ω
Voltage Noise	$e_{n\ p-p}$	0.1Hz to 10Hz	—	2	—	μV_{p-p}
Voltage Noise Density	e_n	$f_o = 10Hz$	—	38	—	$nV/\sqrt{Hz}$
		$f_o = 100Hz$	—	16	—	
		$f_o = 1kHz$	—	13	—	
		$f_o = 10kHz$	—	12	—	
Current Noise Density	i_n	$f_o = 1kHz$	—	0.007	—	$pA/\sqrt{Hz}$
External V_{OS} Trim Range		$R_{pot} = 20k\Omega$	—	4	—	mV
Long-Term V_{OS} Drift			—	5	—	$\mu V/month$
Supply Voltage Range	V_S		± 8	± 15	± 20	V

NOTES:

1. Guaranteed by CMR test.
2. Guaranteed by slew-rate test and formula $BW_p = SR/(2\pi 10V_{PEAK})$.

3. Settling-time is sample tested for A and E grades. Test circuit is shown in Figure 4. Settling-time for F grade is guaranteed but not tested.
4. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq 85^\circ C$ for E/F grades, and $-40^\circ C \leq T_A \leq +85^\circ C$ for G grade, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-42E			OP-42F			OP-42G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}		—	0.4	1.2	—	0.6	2.5	—	2.0	6.0	mV
Offset Voltage Temperature Coefficient	TCV_{OS}		—	4	10	—	8	—	—	8	—	$\mu V/^\circ C$
Input Bias Current	I_B	(Note 1)	—	0.5	1.2	—	0.6	2.0	—	0.6	2.0	nA
Input Offset Current	I_{OS}	(Note 1)	—	0.05	0.2	—	0.06	0.4	—	0.06	0.4	nA
Input Voltage Range	IVR	(Note 2)	± 11	$+12.5$ -12.0	—	± 11	$+12.5$ -12.0	—	± 11	$+12.5$ -12.0	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	86	96	—	80	94	—	80	94	—	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	—	2	40	—	6	50	—	6	50	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$ (Note 1)	200	500	—	200	500	—	200	500	—	V/mV
		$R_L = 2k\Omega$ $V_O = \pm 10V$	100	160	—	100	160	—	100	160	—	
Output Voltage Swing	V_O	$R_L = 2k\Omega$	± 11.0	$+12.3$ -11.8	—	± 11.0	$+12.3$ -11.8	—	± 11.0	$+12.3$ -11.8	—	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	± 8	—	± 60	± 8	—	± 60	± 8	—	± 60	mA
Supply Current	I_{SY}	No Load $V_O = 0V$	—	5.1	6.0	—	5.1	6.5	—	5.1	6.5	mA
Slew Rate	SR	$R_L = 2k\Omega$	45	57	—	40	50	—	40	50	—	V/ μs
Capacitive Load Drive Capability	C_L	Unity-Gain Stable (Note 3)	100	250	—	100	250	—	100	250	—	pF

NOTES:

1. $T_j = 85^\circ C$ for E/F/G Grades; $T_j = 125^\circ C$ for A grade.

2. Guaranteed by CMR test.
3. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$ for A grade, unless otherwise noted.

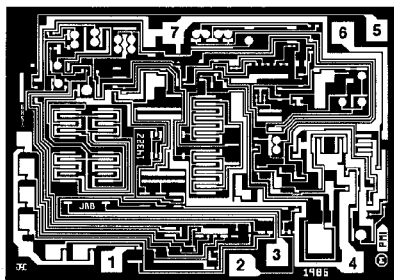
PARAMETER	SYMBOL	CONDITIONS	OP-42A			UNITS
			MIN	TYP	MAX	
Offset Voltage	V_{OS}		–	0.5	2.0	mV
Offset Voltage Temperature Coefficient	TCV_{OS}		–	4	10	$\mu V/^\circ C$
Input Bias Current	I_B	(Note 1)	–	6	20	nA
Input Offset Current	I_{OS}	(Note 1)	–	0.2	1.0	nA
Input Voltage Range	IVR	(Note 2)	± 11	+12.5 –12.0	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	80	94	–	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	–	10	50	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$ (Note 1)	160	350	–	V/mV
		$R_L = 2k\Omega$ $V_O = \pm 10V$	80	110	–	
Output Voltage Swing	V_O	$R_L = 2k\Omega$	± 11.0	+12.3 –11.8	–	V
Short-Circuit Current Limit	I_{sc}	Output Shorted to Ground	± 8	–	± 60	mA
Supply Current	I_{SY}	No Load $V_O = 0V$	–	5.1	6.0	mA
Slew Rate	SR	$R_L = 2k\Omega$	40	52	–	V/ μs
Capacitive Load Drive Capability	C_L	Unity-Gain Stable (Note 3)	100	250	–	pF

NOTES:

1. $T_j = 85^\circ C$ for E/F Grades; $T_j = 125^\circ C$ for A grade.
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

OP-42

DICE CHARACTERISTICS



DIE SIZE 0.098 × 0.070 inch, 6860 sq. mils
(2.49 × 1.78 mm, 4.43 sq. mm)

1. OFFSET VOLTAGE NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. NEGATIVE SUPPLY
5. OFFSET VOLTAGE NULL
6. AMPLIFIER OUTPUT
7. POSITIVE SUPPLY

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_J = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-42N LIMIT	UNITS
Offset Voltage	V_{OS}		1.5	mV MAX
Input Bias Current	I_B	$V_{CM} = 0V$	250	pA MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	50	pA MAX
Input Voltage Range	IVR	(Note 1)	± 11	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	80	dB MIN
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	50	$\mu V/V$ MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$	500	V/mV MIN
		$R_L = 2k\Omega$	200	
		$R_L = 1k\Omega$	100	
Output Voltage Swing	V_O	$R_L = 1k\Omega$	± 11.5	V MIN
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	$\pm 20/\pm 60$	mA MIN/MAX
Supply Current	I_{SY}	No Load $V_O = 0V$	6.5	mA MAX
Slew Rate	SR		40	V/ μs MIN
Capacitive Load Drive Capability	C_L	Unity-Gain Stable (Note 2)	100	pF MIN

NOTES:

1. Guaranteed by CMR test.
2. Guaranteed but not tested.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

BURN-IN CIRCUIT

