

FEATURES

Single/Dual-Supply Operation

1.6 V to 36 V

± 0.8 V to ± 18 V

True Single-Supply Operation; Input and Output

Voltage Ranges Include Ground

Low Supply Current: 80 μ A Max

High Output Drive: 5 mA Min

Low Offset Voltage: 0.5 mV Max

High Open-Loop Gain: 700 V/mV Min

Outstanding PSRR: 5.6 mV/V Min

Industry Standard Quad Pinouts

Available in Die Form

GENERAL DESCRIPTION

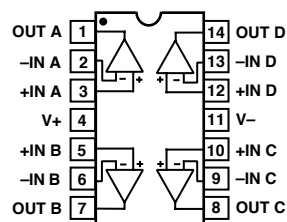
The OP490 is a high-performance micropower quad op amp that operates from a single supply of 1.6 V to 36 V or from dual supplies of ± 0.8 V to ± 18 V. Input voltage range includes the negative rail allowing the OP490 to accommodate input signals down to ground in single-supply operation. The OP490's output swing also includes ground when operating from a single supply, enabling "zero-in, zero-out" operation.

The quad OP490 draws less than 20 μ A of quiescent supply current per amplifier, but each amplifier is able to deliver over 5 mA of output current to a load. Input offset voltage is under 0.5 mV with offset drift below 5 μ V/ $^{\circ}$ C over the military temperature range. Gain exceeds over 700,000 and CMR is better than 100 dB. A PSRR of under 5.6 μ V/V minimizes offset voltage changes experienced in battery-powered systems.

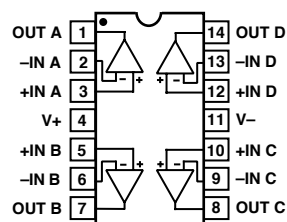
The quad OP490 combines high performance with the space and cost savings of quad amplifiers. The minimal voltage and current requirements of the OP490 make it ideal for battery- and solar-powered applications, such as portable instruments and remote sensors.

PIN CONNECTION

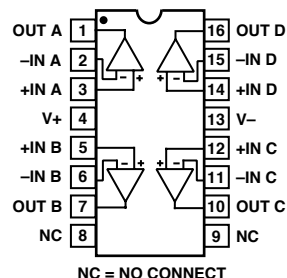
14-Lead Hermetic DIP (Y Suffix)



14-Lead Plastic DIP (P Suffix)



16-Lead SOIC (S Suffix)



OP490—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 1.5\text{ V}$ to $\pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Conditions	OP490E			OP490F			OP490G			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{OS}			0.2	0.5		0.4	0.75		0.6	1.0	mV
Input Offset Current	I_{OS}	$V_{CM} = 0\text{ V}$		0.4	3.0		0.4	5		0.4	5	nA
Input Bias Current	I_B	$V_{CM} = 0\text{ V}$		4.2	15.0		4.2	20		4.2	25	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15\text{ V}$, $V_O = \pm 10\text{ V}$, $R_L = 100\text{ k}\Omega$	700	1,200		500	1,000		400	800		V/mV
		$R_L = 10\text{ k}\Omega$	350	600		250	500		200	400		V/mV
		$R_L = 2\text{ k}\Omega$	125	250		100	200		100	200		V/mV
		$V_+ = 5\text{ V}$, $V_- = 0\text{ V}$, $1\text{ V} < V_O < 4\text{ V}$										
		$R_L = 100\text{ k}\Omega$	200	400		125	300		100	250		V/mV
		$R_L = 10\text{ k}\Omega$	100	180		75	140		70	140		V/mV
Input Voltage Range	IVR	$V_+ = 5\text{ V}$, $V_- = 0\text{ V}$ $V_S = \pm 15\text{ V}^1$	0/4 -15/+13.5			0/4 -15/+13.5			0/4 -15/+13.5			V V
Output Voltage Swing	V_O	$V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$	± 13.5	± 14.2		± 13.5	± 14.2		± 13.5	± 14.2		V
	V_{OH}	$R_L = 2\text{ k}\Omega$ $V_+ = 5\text{ V}$, $V_- = 0\text{ V}$,	± 10.5	± 11.5		± 10.5	± 11.5		± 10.5	± 11.5		V
	V_{OL}	$R_L = 2\text{ k}\Omega$ $V_+ = 5\text{ V}$, $V_- = 0\text{ V}$,	4.0	4.2		4.0	4.2		4.0	4.2		V
		$R_L = 10\text{ k}\Omega$		100	500		100	500		100	500	μV
Common-Mode Rejection Ratio	CMRR	$V_+ = 5\text{ V}$, $V_- = 0\text{ V}$, $0\text{ V} < V_{CM} < 4\text{ V}$	90	110		80	100		800	100		dB
		$V_S = \pm 15\text{ V}$, $-15\text{ V} < V_{CM} < +13.5\text{ V}$	100	130		90	120		90	120		dB
Power Supply Rejection Ratio	PSRR			1.0	5.6		3.2	10		3.2	10	$\mu\text{V/V}$
Slew Rate	SR	$V_S = \pm 15\text{ V}$	5	12		5	12		5	12		V/ms
Supply Current (All Amplifiers)	I_{SY}	$V_S = \pm 1.5\text{ V}$, No Load		40	60		40	60		40	60	μA
		$V_S = \pm 15\text{ V}$, No Load		60	80		60	80		60	80	μA
Capacitive Load Stability		$A_V = 1$		650			650			650		pF
Input Noise Voltage	e_n p-p	$f_O = 0.1\text{ Hz}$ to 10 Hz , $V_S = \pm 15\text{ V}$		3			3			3		$\mu\text{V p-p}$
Input Resistance Differential Mode	R_{IN}	$V_S = \pm 15\text{ V}$		30			30			30		M Ω
Input Resistance Common-Mode	R_{INCM}	$V_S = \pm 15\text{ V}$		20			20			20		G Ω
Gain Bandwidth Product	GBWP	$A_V = 1$		20			20			20		kHz
Channel Separation	CS	$f_O = 10\text{ Hz}$, $V_O = 20\text{ V p-p}$ $V_S = \pm 15\text{ V}^2$	120	150		120	150		120	150		dB

NOTES

¹Guaranteed by CMRR test.

²Guaranteed but not 100% tested.

Specifications subject to change without notice

ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 1.5 \text{ V}$ to $\pm 15 \text{ V}$, $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ for OP490E/F, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ for OP490G, unless otherwise noted)

Parameter	Symbol	Conditions	OP490E			OP490F			OP490G			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{OS}			0.32	0.8		0.6	1.35		0.8	1.5	mV
Average Input Offset Voltage Drift	TCV_{OS}	$V_S = \pm 15 \text{ V}$		2	5		4			4		$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{OS}	$V_{CM} = 0 \text{ V}$		0.8	3		1.0	5		1.3	7	nA
Input Bias Current	I_B	$V_{CM} = 0 \text{ V}$		4.4	15		4.4	20		4.4	25	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15 \text{ V}$, $V_O = \pm 10 \text{ V}$, $R_L = 100 \text{ k}\Omega$	500	800		350	700		300	600		V/mV
		$R_L = 10 \text{ k}\Omega$	250	400		175	250		150	250		V/mV
		$R_L = 2 \text{ k}\Omega$	100	200		75	150		75	125		V/mV
		$V_+ = 5 \text{ V}$, $V_- = 0 \text{ V}$, $1 \text{ V} < V_O < 4 \text{ V}$										
		$R_L = 100 \text{ k}\Omega$	150	280		100	220		80	160		V/mV
		$R_L = 10 \text{ k}\Omega$	75	140		50	110		40	90		V/mV
Input Voltage Range	IVR	$V_+ = 5 \text{ V}$, $V_- = 0 \text{ V}$ $V_S = \pm 15 \text{ V}^*$	0.3/5 -15/+13.5			0.3/5 -15/+13.5			0.3/5 -15/+13.5			V V
Output Voltage Swing	V_O	$V_S = \pm 15 \text{ V}$, $R_L = 10 \text{ k}\Omega$	± 13	± 14		± 13	± 14		± 13	± 14		V
	V_{OH}	$R_L = 2 \text{ k}\Omega$	± 10	± 11		± 10	± 11		± 10	± 11		V
	V_{OL}	$V_+ = 5 \text{ V}$, $V_- = 0 \text{ V}$, $R_L = 2 \text{ k}\Omega$	3.9	4.1		3.9	4.1		3.9	4.1		V
		$V_+ = 5 \text{ V}$, $V_- = 0 \text{ V}$, $R_L = 10 \text{ k}\Omega$		100	500		100	500		100	500	μV
Common-Mode Rejection Ratio	CMRR	$V_+ = 5 \text{ V}$, $V_- = 0 \text{ V}$, $0 \text{ V} < V_{CM} < 3.5 \text{ V}$	90	110		80	100		800	100		dB
		$V_S = \pm 15 \text{ V}$, $-15 \text{ V} < V_{CM} < +13.5 \text{ V}$	100	120		90	110		90	110		dB
Power Supply Rejection Ratio	PSRR			1.0	5.6		3.2	10		5.6	17.8	$\mu\text{V}/\text{V}$
Supply Current (All Amplifiers)	I_{SY}	$V_S = \pm 1.5 \text{ V}$, No Load		65	100		65	100		60	100	μA
		$V_S = \pm 15 \text{ V}$, No Load		80	120		80	120		75	120	μA

NOTE

*Guaranteed by CMRR test.

Specifications subject to change without notice

OP490

WAFER TEST LIMITS (@ $V_S = \pm 1.5\text{ V}$ to $\pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Conditions	Limits	Unit
Input Offset Voltage	V_{OS}		0.75	mV max
Input Offset Current	I_{OS}	$V_{CM} = 0\text{ V}$	5	nA max
Input Bias Current	I_B	$V_{CM} = 0\text{ V}$	20	nA max
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15\text{ V}$, $V_O = \pm 10\text{ V}$, $R_L = 100\text{ k}\Omega$	500	V/mV min
		$R_L = 10\text{ k}\Omega$	250	V/mV min
		$V_+ = 5\text{ V}$, $V_- = 0\text{ V}$	125	V/mV min
		$1\text{ V} < V_O < 4\text{ V}$, $R_L = 100\text{ k}\Omega$		
Input Voltage Range	IVR	$V_+ = 5\text{ V}$, $V_- = 0\text{ V}$ $V_S = \pm 15\text{ V}^*$	0/4 -15/+13.5	V min V min
Output Voltage Swing	V_O	$V_S = \pm 15\text{ V}$ $R_L = 10\text{ k}\Omega$	± 13.5	V min
		$R_L = 2\text{ k}\Omega$	± 10.5	V min
	V_{OH}	$V_+ = 5\text{ V}$, $V_- = 0\text{ V}$, $R_L = 2\text{ k}\Omega$	4.0	V min
	V_{OL}	$V_+ = 5\text{ V}$, $V_- = 0\text{ V}$, $R_L = 10\text{ k}\Omega$	500	μV max
Common-Mode Rejection Ratio	CMRR	$V_+ = 5\text{ V}$, $V_- = 0\text{ V}$, $0\text{ V} < V_{CM} < 4\text{ V}$	80	dB min
		$V_S = \pm 15\text{ V}$, $-15\text{ V} < V_{CM} < +13.5\text{ V}$	90	dB min
Power Supply Rejection Ratio	PSRR		10	$\mu\text{V/V}$ max
Supply Current (All Amplifiers)	I_{SY}	$V_S = \pm 15\text{ V}$, No Load	80	μA max

NOTE
*Guaranteed by CMRR test.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

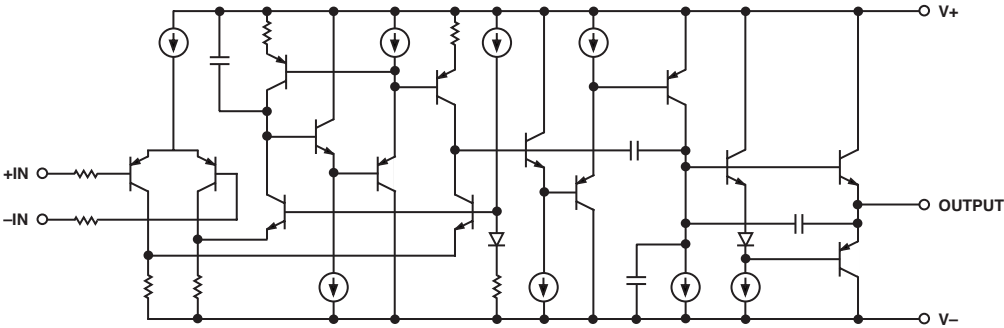


Figure 1. Simplified Schematic

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage	± 18 V
Digital Input Voltage	[(V-) - 20 V] to [(V+) + 20 V]
Common-Mode Input Voltage	[(V-) - 20 V] to [(V+) + 20 V]
Output Short Circuit Duration	Continuous
Storage Temperature Range	
Y and P Packages	-65°C to +150°C
Operating Temperature Range	
OP490E, OP490F	-25°C to +85°C
OP490G	-40°C to +85°C
Junction Temperature (T _J)	-65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Type	θ_{JA} *	θ_{JC}	Unit
14-Pin Hermetic DIP (Y)	99	12	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOL (S)	92	27	°C/W

* θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for Cerdip and PDIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOL package

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP490EY*	-25°C to +85°C	14-Lead Cerdip	Y-14
OP490FY*	-25°C to +85°C	14-Lead Cerdip	Y-14
OP490GP	-40°C to +85°C	14-Lead Plastic DIP	P-14
OP490GS	-40°C to +85°C	16-Lead SOIC	S-14

*Not recommended for new designs. Obsolete April 2002.

For Military processed devices, please refer to the Standard Microcircuit Drawing (SMD) available at www.dscc.dla.mil/programs/milspec/default.asp

SMD Part Number	ADI Equivalent
5962-89670013A*	OP490ATCMTDA
5962-8967001CA*	OP490AYMTDA

*Not recommended for new designs. Obsolete April 2002.

CAUTION

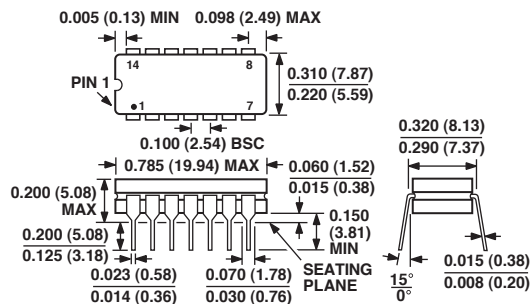
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP490 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



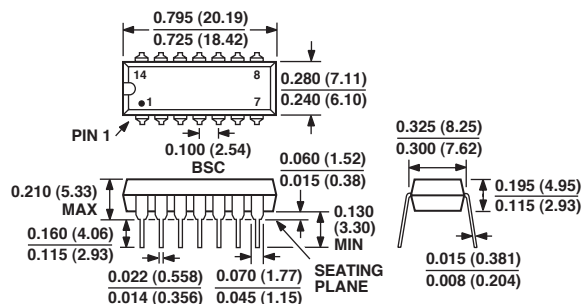
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead Hermetic DIP (Y Suffix)



14-Lead Plastic DIP (P Suffix)



16-Lead SOIC (S Suffix)

