Dual/Quad Rail-to-Rail Operational Amplifiers

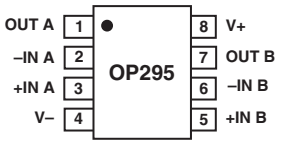
OP295/OP495

FEATURES
Rail-to-Rail Output Swing
Single-Supply Operation: 3 V to 36 V
Low Offset Voltage: 300 mV
Gain Bandwidth Product: 75 kHz
High Open-Loop Gain: 1,000 V/mV
Unity-Gain Stable
Low Supply Current/Per Amplifier: 150 μA max

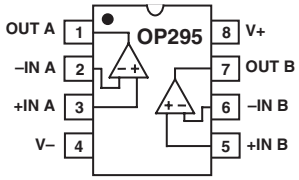
APPLICATIONS
Battery-Operated Instrumentation
Servo Amplifiers
Actuator Drives
Sensor Conditioners
Power Supply Control

PIN CONNECTIONS

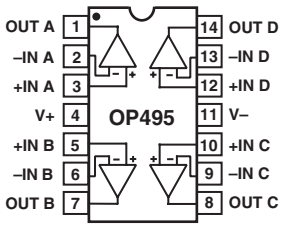
8-Lead Narrow-Body SOIC (S Suffix)



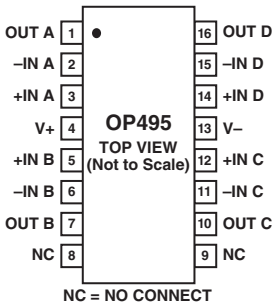
8-Lead Narrow-Body SOIC (S Suffix)



14-Lead PDIP (P Suffix)



14-Lead PDIP (P Suffix)



GENERAL DESCRIPTION

Rail-to-rail output swing combined with dc accuracy are the key features of the OP495 quad and OP295 dual CBCMOS operational amplifiers. By using a bipolar front end, lower noise and higher accuracy than that of CMOS designs has been achieved. Both input and output ranges include the negative supply, providing the user zero-in/zero-out capability. For users of 3.3 V systems such as lithium batteries, the OP295/OP495 is specified for 3 V operation.

Maximum offset voltage is specified at 300 μV for 5 V operation, and the open-loop gain is a minimum of 1000 V/mV. This yields performance that can be used to implement high accuracy systems, even in single-supply designs.

The ability to swing rail-to-rail and supply 15 mA to the load makes the OP295/OP495 an ideal driver for power transistors and "H" bridges. This allows designs to achieve higher efficiencies and to transfer more power to the load than previously possible without the use of discrete components. For applications such as transformers that require driving inductive loads, increases in efficiency are also possible. Stability while driving capacitive loads is another benefit of this design over CMOS rail-to-rail amplifiers. This is useful for driving coax cable or large FET transistors. The OP295/OP495 is stable with loads in excess of 300 pF.

The OP295 and OP495 are specified over the extended industrial (–40°C to +125°C) temperature range. OP295s are available in 8-lead plastic DIP plus SOIC-8 surface-mount packages. OP495s are available in 14-lead plastic and SOIC-16 surface-mount packages.

REV. D

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OP295/OP495–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = 5.0 V, V_{CM} = 2.5 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			30	300	µV
		–40°C ≤ T_A ≤ +125°C			800	µV
Input Bias Current	I_B			8	20	nA
		–40°C ≤ T_A ≤ +125°C			30	nA
Input Offset Current	I_{OS}			±1	±3	nA
		–40°C ≤ T_A ≤ +125°C			±5	nA
Input Voltage Range	V_{CM}		0		4.0	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 4.0 V, –40°C ≤ T_A ≤ +125°C	90	110		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, 0.005 ≤ V_{OUT} ≤ 4.0 V	1,000	10,000		V/mV
		R_L = 10 kΩ, –40°C ≤ T_A ≤ +125°C	500			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1	5	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	R_L = 100 kΩ to GND	4.98	5.0		V
		R_L = 10 kΩ to GND	4.90	4.94		V
		I_{OUT} = 1 mA, –40°C ≤ T_A ≤ +125°C		4.7		V
Output Voltage Swing Low	V_{OL}	R_L = 100 kΩ to GND		0.7	2	mV
		R_L = 10 kΩ to GND		0.7	2	mV
		I_{OUT} = 1 mA, –40°C ≤ T_A ≤ +125°C		90		mV
Output Current	I_{OUT}		±11	±18		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	±1.5 V ≤ V_S ≤ ±15 V	90	110		dB
		±1.5 V ≤ V_S ≤ ±15 V, –40°C ≤ T_A ≤ +125°C	85			dB
Supply Current Per Amplifier	I_{SY}	V_{OUT} = 2.5 V, R_L = ∞, –40°C ≤ T_A ≤ +125°C			150	µA
DYNAMIC PERFORMANCE						
Skew Rate	SR	R_L = 10 kΩ		0.03		V/µs
Gain Bandwidth Product	GBP			75		kHz
Phase Margin	θ_O			86		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		1.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		51		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		<0.1		pA/√Hz

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = 3.0 V, V_{CM} = 1.5 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			100	500	µV
Input Bias Current	I_B			8	20	nA
Input Offset Current	I_{OS}			±1	±3	nA
Input Voltage Range	V_{CM}		0		2.0	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 2.0 V, –40°C ≤ T_A ≤ +125°C	90	110		dB
Large Voltage Gain	A_{VO}	R_L = 10 kΩ		750		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	R_L = 10 kΩ to GND	2.9			V
Output Voltage Swing Low	V_{OL}	R_L = 10 kΩ to GND		0.7	2	mV
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	±1.5 V ≤ V_S ≤ ±15 V	90	110		dB
		±1.5 V ≤ V_S ≤ ±15 V, –40°C ≤ T_A ≤ +125°C	85			dB
Supply Current Per Amplifier	I_{SY}	V_{OUT} = 1.5 V, R_L = ∞, –40°C ≤ T_A ≤ +125°C			150	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.03		V/µs
Gain Bandwidth Product	GBP			75		kHz
Phase Margin	θ_O			85		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		1.6		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		53		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		<0.1		pA/√Hz

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			300	500	µV
		–40°C ≤ T_A ≤ +125°C			800	µV
Input Bias Current	I_B	V_{CM} = 0 V		7	20	nA
		V_{CM} = 0 V, –40°C ≤ T_A ≤ +125°C			30	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V		±1	±3	nA
		V_{CM} = 0 V, –40°C ≤ T_A ≤ +125°C			±5	nA
Input Voltage Range	V_{CM}		–15		13.5	V
Common-Mode Rejection Ratio	CMRR	–15.0 V ≤ V_{CM} ≤ +13.5 V, –40°C ≤ T_A ≤ +125°C	90	110		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ	1,000	4,000		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	R_L = 100 kΩ to GND	14.95			V
		R_L = 10 kΩ to GND	14.80			V
Output Voltage Swing Low	V_{OL}	R_L = 100 kΩ to GND			–14.95	V
		R_L = 10 kΩ to GND			–14.85	V
Output Current	I_{OUT}		±15	±25		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±1.5 V to ±15 V	90	110		dB
		V_S = ±1.5 V to ±15 V, –40°C ≤ T_A ≤ +125°C	85			dB
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞, V_S = ±18 V,				
		–40°C ≤ T_A ≤ +125°C			175	µA
Supply Voltage Range	V_S		3 (±1.5)		36 (±18)	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.03		V/µs
Gain Bandwidth Product	GBP			85		kHz
Phase Margin	θ_O			83		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		1.25		µV p-p
Voltage Noise Density	e_n	f =1 kHz		45		nV/$\sqrt{\text{Hz}}$
Current Noise Density	i_n	f = 1 kHz		<0.1		pA/$\sqrt{\text{Hz}}$

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1, 2]

Supply Voltage . . . . . ±18 V
Input Voltage[2] . . . . . ±18 V
Differential Input Voltage[3]. . . . . 36 V
Output Short-Circuit Duration . . . . . Indefinite
Storage Temperature Range
P, S Package . . . . . –65°C to +150°C
Operating Temperature Range
OP295G, OP495G . . . . . –40°C to +125°C
Junction Temperature Range
P, S Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C

NOTES
[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2] Absolute maximum ratings apply to packaged parts, unless otherwise noted.
[3] For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

Package Type	θ_{JA}*	θ_{JC}	Unit
8-Lead Plastic DIP (P)	103	43	°C/W
8-Lead SOIC (S)	158	43	°C/W
14-Lead Plastic DIP (P)	83	39	°C/W
16-Lead SOIC (S)	98	30	°C/W

*θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for CERDIP, PDIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

ORDERING GUIDE

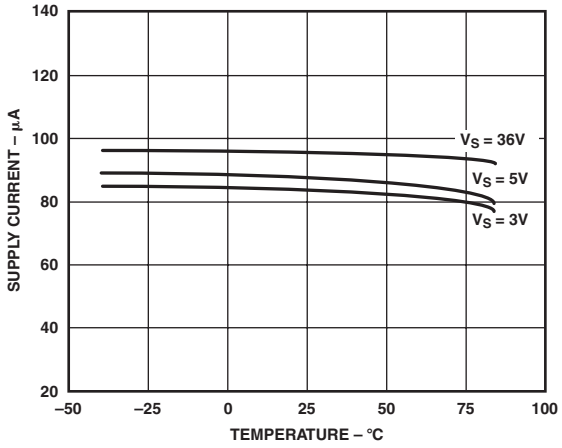
Model	Temperature Range	Package Description	Package Option
OP295GP	–40°C to +125°C	8-Lead Plastic DIP	P-8 (N-8)
OP295GS	–40°C to +125°C	8-Lead SOIC	S-8 (R-8)
OP295GS-REEL	–40°C to +125°C	8-Lead SOIC	S-8 (R-8)
OP295GS-REEL7	–40°C to +125°C	8-Lead SOIC	S-8 (R-8)
OP495GP	–40°C to +125°C	14-Lead Plastic DIP	P-14 (N-14)
OP495GS	–40°C to +125°C	16-Lead SOIC	S-16 (RW-16)
OP495GS-REEL	–40°C to +125°C	16-Lead SOIC	S-16 (RW-16)
OP495GSZ*	–40°C to +125°C	16-Lead SOIC	S-16 (RW-16)
OP495GSZ-REEL7*	–40°C to +125°C	16-Lead SOIC	S-16 (RW-16)

*Z = Pb-free part.

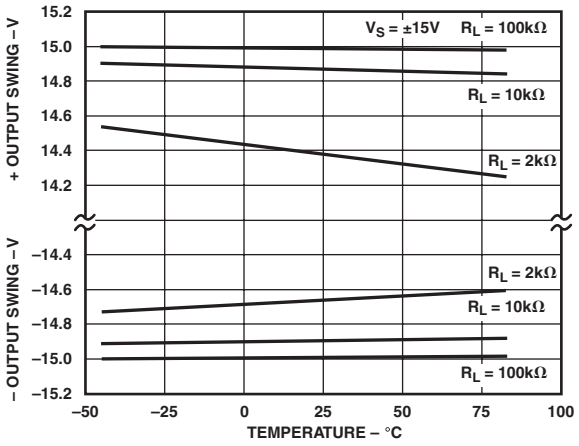
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP295/OP495 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Typical Performance Characteristics



TPC 1. Supply Current Per Amplifier vs. Temperature



TPC 2. Output Voltage Swing vs. Temperature