

FEATURES

Filterless Class-D amplifier with built-in output stage
2 W into 4 Ω and 1.4 W into 8 Ω at 5.0 V supply with <10% THD
85% efficiency at 5.0 V, 1.4 W into 8 Ω speaker
Better than 98 dB SNR (signal-to-noise ratio)
Available in 16-lead, 3 mm $\times$ 3 mm LFCSP
Single-supply operation from 2.5 V to 5.0 V
20 nA ultralow shutdown current
Short-circuit and thermal protection
Pop-and-click suppression
Built-in resistors reduce board component count
Default fixed 18 dB gain and user-adjustable

APPLICATIONS

Notebooks and PCs
Mobile phones
MP3 players
Portable gaming
Portable electronics
Educational toys

GENERAL DESCRIPTION

The SSM2304 is a fully integrated, high efficiency, Class-D stereo audio amplifier. It is designed to maximize performance for portable applications. The application circuit requires a minimum of external components and operates from a single 2.5 V to 5.0 V supply. It is capable of delivering 2 W of continuous output power with less than 10% THD + N driving a 4 Ω load from a 5.0 V supply.

The SSM2304 features a high efficiency, low noise modulation scheme. It operates with 85% efficiency at 1.4 W into 8 Ω from a 5.0 V supply and has a signal-to-noise ratio (SNR) that is better than 98 dB. PDM modulation is used to provide lower EMI-radiated emissions compared with other Class-D architectures.

The SSM2304 has a micropower shutdown mode with a typical shutdown current of 20 nA. Shutdown is enabled by applying a logic low to the $\overline{\text{SD}}$ pin.

The architecture of the device allows it to achieve a very low level of pop and click. This minimizes voltage glitches at the output during turn-on and turn-off, thus reducing audible noise on activation and deactivation.

The fully differential input of the SSM2304 provides excellent rejection of common-mode noise on the input. Input coupling capacitors can be omitted if the dc input common-mode voltage is approximately $V_{\text{DD}}/2$.

The SSM2304 also has excellent rejection of power supply noise, including noise caused by GSM transmission bursts and RF rectification.

The SSM2304 has a preset gain of 18 dB, which can be reduced by using external resistors.

The SSM2304 is specified over the commercial temperature range (-40°C to $+85^{\circ}\text{C}$). It has built-in thermal shutdown and output short-circuit protection. It is available in a 16-lead, 3 mm $\times$ 3 mm lead-frame chip scale package (LFCSP).

FUNCTIONAL BLOCK DIAGRAM

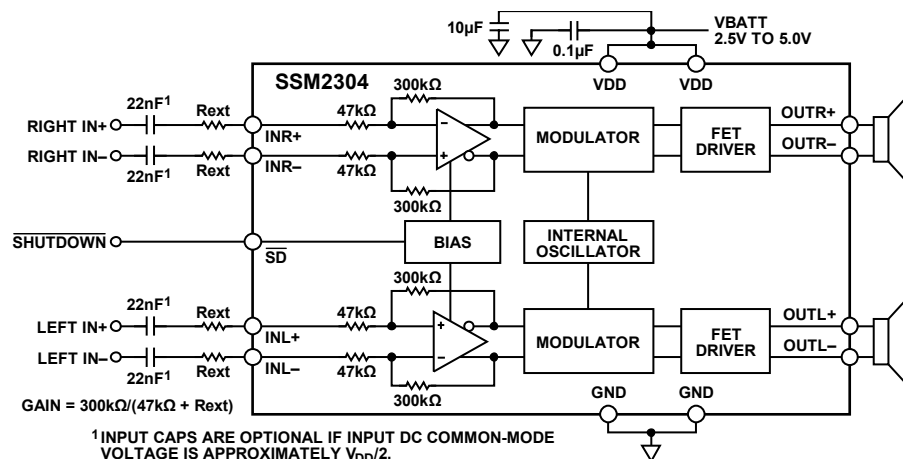


Figure 1.

Rev. 0

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SPECIFICATIONS

$V_{DD} = 5.0\text{ V}$; $T_A = 25^\circ\text{C}$; $R_L = 4\ \Omega, 8\ \Omega$; gain = 18 dB; unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Output Power	P_O	$R_L = 4\ \Omega$, THD = 1%, $f = 1\text{ kHz}$, 20 kHz BW, $V_{DD} = 5.0\text{ V}$		1.8		W
		$R_L = 8\ \Omega$, THD = 1%, $f = 1\text{ kHz}$, 20 kHz BW, $V_{DD} = 5.0\text{ V}$		1.4		W
		$R_L = 4\ \Omega$, THD = 1%, $f = 1\text{ kHz}$, 20 kHz BW, $V_{DD} = 3.6\text{ V}$		0.9		W
		$R_L = 8\ \Omega$, THD = 1%, $f = 1\text{ kHz}$, 20 kHz BW, $V_{DD} = 3.6\text{ V}$		0.615		W
		$R_L = 4\ \Omega$, THD = 1%, $f = 1\text{ kHz}$, 20 kHz BW, $V_{DD} = 2.5\text{ V}$		0.35		W
		$R_L = 8\ \Omega$, THD = 1%, $f = 1\text{ kHz}$, 20 kHz BW, $V_{DD} = 2.5\text{ V}$		0.275		W
		$R_L = 4\ \Omega$, THD = 10%, $f = 1\text{ kHz}$, 20 kHz BW, $V_{DD} = 5.0\text{ V}$		2.4		W
		$R_L = 8\ \Omega$, THD = 10%, $f = 1\text{ kHz}$, 20 kHz BW, $V_{DD} = 5.0\text{ V}$		1.53		W
		$R_L = 4\ \Omega$, THD = 10%, $f = 1\text{ kHz}$, 20 kHz BW, $V_{DD} = 3.6\text{ V}$		1.1		W
		$R_L = 8\ \Omega$, THD = 10%, $f = 1\text{ kHz}$, 20 kHz BW, $V_{DD} = 3.6\text{ V}$		0.77		W
		$R_L = 4\ \Omega$, THD = 10%, $f = 1\text{ kHz}$, 20 kHz BW, $V_{DD} = 2.5\text{ V}$		0.45		W
		$R_L = 8\ \Omega$, THD = 10%, $f = 1\text{ kHz}$, 20 kHz BW, $V_{DD} = 2.5\text{ V}$		0.35		W
		$P_{OUT} = 2\text{ W}$, $4\ \Omega$, $V_{DD} = 5.0\text{ V}$		75		%
		$P_{OUT} = 1.4\text{ W}$, $8\ \Omega$, $V_{DD} = 5.0\text{ V}$		85		%
Efficiency	η	$P_O = 2\text{ W}$ into $4\ \Omega$ each channel, $f = 1\text{ kHz}$, $V_{DD} = 5.0\text{ V}$		0.2		%
Total Harmonic Distortion + Noise	THD + N	$P_O = 1\text{ W}$ into $8\ \Omega$ each channel, $f = 1\text{ kHz}$, $V_{DD} = 3.6\text{ V}$		0.25		%
Input Common-Mode Voltage Range	V_{CM}		1.0		$V_{DD} - 1$	V
Common-Mode Rejection Ratio	$CMRR_{GSM}$	$V_{CM} = 2.5\text{ V} \pm 100\text{ mV}$ at 217 Hz		60		dB
Channel Separation	X_{TALK}	$P_O = 100\text{ mW}$, $f = 1\text{ kHz}$		78		dB
Average Switching Frequency	f_{SW}			1.8		MHz
Differential Output Offset Voltage	V_{OOS}			2.0		mV
POWER SUPPLY						
Supply Voltage Range	V_{DD}	Guaranteed from PSRR test	2.5		5.0	V
Power Supply Rejection Ratio	PSRR	$V_{DD} = 2.5\text{ V}$ to 5.0 V ,	70	85		dB
	$PSRR_{GSM}$	$V_{RIPPLE} = 100\text{ mV rms}$ at 217 Hz, inputs ac GND, $C_{IN} = 0.01\ \mu\text{F}$, input referred		68		dB
Supply Current	I_{SY}	$V_{IN} = 0\text{ V}$, no load, $V_{DD} = 5.0\text{ V}$		7.0		mA
		$V_{IN} = 0\text{ V}$, no load, $V_{DD} = 3.6\text{ V}$		6.5		mA
		$V_{IN} = 0\text{ V}$, no load, $V_{DD} = 2.5\text{ V}$		5.2		mA
Shutdown Current	I_{SD}	$\overline{SD} = \text{GND}$		20		nA
GAIN						
Closed-Loop Gain	A_v	$R_{EXT} = 0$		18		dB
Differential Input Impedance	Z_{IN}	$\overline{SD} = V_{DD}$		47		k Ω
SHUTDOWN CONTROL						
Input Voltage High	V_{IH}	$I_{SY} \geq 1\text{ mA}$		1.2		V
Input Voltage Low	V_{IL}	$I_{SY} \leq 300\text{ nA}$		0.5		V
Turn-On Time	t_{WU}	$\overline{SD}$ rising edge from GND to V_{DD}		30		ms
Turn-Off Time	t_{SD}	$\overline{SD}$ falling edge from V_{DD} to GND		5		μs
Output Impedance	Z_{OUT}	$\overline{SD} = \text{GND}$		>100		k Ω
NOISE PERFORMANCE						
Output Voltage Noise	e_n	$V_{DD} = 3.6\text{ V}$, $f = 20\text{ Hz}$ to 20 kHz , inputs are ac grounded, $A_v = 6\text{ dB}$, $R_L = 4\ \Omega$, A weighting		22		μV
Signal-to-Noise Ratio	SNR	$P_{OUT} = 2.0\text{ W}$, $R_L = 4\ \Omega$		102		dB

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	V_{DD}
Common-Mode Input Voltage	V_{DD}
ESD Susceptibility	4 kV
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–40°C to +85°C
Junction Temperature Range	–65°C to +165°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
16-lead, 3 mm × 3 mm LFCSP	44	31.5	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

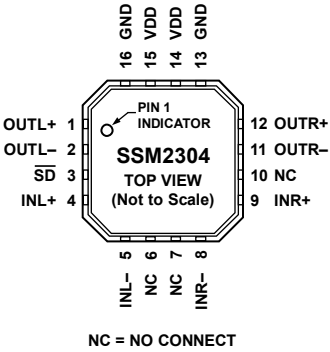
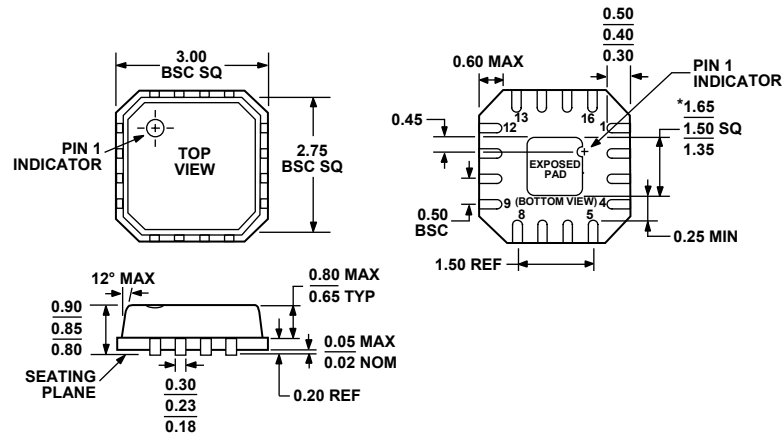


Figure 2. SSM2304 LFCSP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUTL+	Inverting Output for Left Channel.
2	OUTL-	Noninverting Output for Left Channel.
3	$\overline{SD}$	Shutdown Input. Active low digital input.
4	INL+	Noninverting Input for Left Channel.
5	INL-	Inverting Input for Left Channel.
6	NC	No Connect.
7	NC	No Connect.
8	INR-	Inverting Input for Right Channel.
9	INR+	Noninverting Input for Right Channel.
10	NC	No Connect
11	OUTR-	Noninverting Output for Right Channel.
12	OUTR+	Inverting Output for Right Channel.
13	GND	Ground for Output Amplifiers.
14	VDD	Power Supply for Output Amplifiers.
15	VDD	Power Supply for Output Amplifiers.
16	GND	Ground for Output Amplifiers.

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-220-VEED-2
EXCEPT FOR EXPOSED PAD DIMENSION.

Figure 47. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm × 3 mm Body, Very Thin Quad
(CP-16-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
SSM2304CPZ-REEL ¹	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-3	A1F
SSM2304CPZ-REEL7 ¹	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-3	A1F
SSM2304Z-EVAL ¹		Evaluation Board		

¹ Z = Pb-free part.