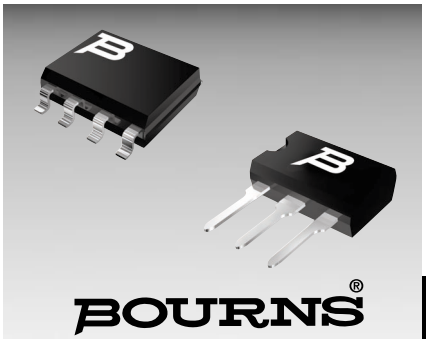


TISP3240F3, TISP3260F3, TISP3290F3,TISP3320F3,TISP3380F3

HIGH-VOLTAGE DUAL BIDIRECTIONAL THYRISTOR OVERVOLTAGE PROTECTORS

TISP3xxxF3 (HV) Overvoltage Protector Series

Ion-Implanted Breakdown Region
Precise and Stable Voltage
Low Voltage Overshoot under Surge

DEVICE	V_{DRM} V	$V_{(BO)}$ V
'3240F3	180	240
'3260F3	200	260
'3290F3	220	290
'3320F3	240	320
'3380F3	270	380

Planar Passivated Junctions
Low Off-State Current <10 μA

Rated for International Surge Wave Shapes

Waveshape	Standard	I_{TSP} A
2/10 μs	GR-1089-CORE	175
8/20 μs	IEC 61000-4-5	120
10/160 μs	FCC Part 68	60
10/700 μs	ITU-T K.20/21 FCC Part 68	50
10/560 μs	FCC Part 68	45
10/1000 μs	GR-1089-CORE	35

..... UL Recognized Component

Description

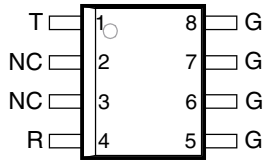
These high-voltage dual bidirectional thyristor protectors are designed to protect ground backed ringing central office, access and customer premise equipment against overvoltages caused by lightning and a.c. power disturbances. Offered in five voltage variants to meet battery and protection requirements, they are guaranteed to suppress and withstand the listed international lightning surges in both polarities. Overvoltages are initially clipped by breakdown clamping until the voltage rises to the breakover level, which causes the device to switch. The high crowbar holding current prevents d.c. latchup as the current subsides.

How To Order

Device	Package	Carrier	Order As
TISP3xxxF3	D, Small-outline	Tape And Reeled	TISP3xxxF3DR
	P, Plastic Dip	Tube	TISP3xxxF3P
	SL, Single-in-line	Tube	TISP3xxxF3SL

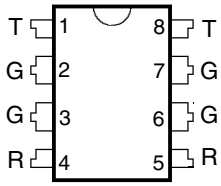
Insert xxx value corresponding to protection voltages of 240 through to 380

D Package (Top View)



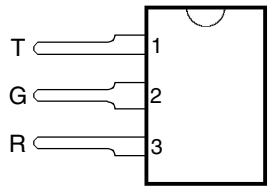
NC - No internal connection

P Package (Top View)



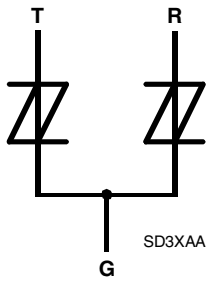
Specified T terminal ratings require connection of pins 1 and 8.
Specified R terminal ratings require connection of pins 4 and 5.

SL Package (Top View)



MD1XAB

Device Symbol



Terminals T, R and G correspond to the alternative line designators of A, B and C

Description (continued)

These monolithic protection devices are fabricated in ion implanted planar structures to ensure precise and matched breakover control and are virtually transparent to the system in normal operation.

Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating		Symbol	Value	Unit
Repetitive peak off-state voltage, 0 °C < T_A < 70 °C	'3240F3	V_{DRM}	±180	V
	'3260F3		±200	
	'3290F3		±220	
	'3320F3		±240	
	'3380F3		±270	
Non-repetitive peak on-state pulse current (see Notes 1 and 2)		I_{PPSM}		A
1/2 (Gas tube differential transient, 1/2 voltage wave shape)			350	
2/10 (Telcordia GR-1089-CORE, 2/10 voltage wave shape)			175	
1/20 (ITU-T K.22, 1.2/50 voltage wave shape, 25 Ω resistor)			90	
8/20 (IEC 61000-4-5, combination wave generator, 1.2/50 voltage wave shape)			120	
10/160 (FCC Part 68, 10/160 voltage wave shape)			60	
4/250 (ITU-T K.20/21, 10/700 voltage wave shape, simultaneous)			55	
0.2/310 (CNET I 31-24, 0.5/700 voltage wave shape)			38	
5/310 (ITU-T K.20/21, 10/700 voltage wave shape, single)			50	
5/320 (FCC Part 68, 9/720 voltage wave shape, single)			50	
10/560 (FCC Part 68, 10/560 voltage wave shape)			45	
10/1000 (Telcordia GR-1089-CORE, 10/1000 voltage wave shape)			35	
Non-repetitive peak on-state current, 0 °C < T_A < 70 °C (see Notes 1 and 3)		I_{TSM}		A
50 Hz, 1 s	D Package		4.3	
	P Package		5.7	
	SL Package		7.1	
Initial rate of rise of on-state current, Linear current ramp, Maximum ramp value < 38 A		di_T/dt	250	A/µs
Junction temperature		T_J	-65 to +150	°C
Storage temperature range		T_{stg}	-65 to +150	°C

NOTES: 1. Further details on surge wave shapes are contained in the Applications Information section.
2. Initially, the TISP® device must be in thermal equilibrium with 0 °C < T_J <70 °C. The surge may be repeated after the TISP® device returns to its initial conditions.
3. Above 70 °C, derate linearly to zero at 150 °C lead temperature.

Electrical Characteristics for R and T Terminal Pair, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	V_D = ±2V_{DRM}, 0 °C < T_A < 70 °C				±10	µA
I_D	Off-state current	V_D = ±50 V				±10	µA
C_{off}	Off-state capacitance	f = 100 kHz, V_d = 100 mV , V_D = 0,	D Package		0.05	0.15	pF
		Third terminal voltage = -50 V to +50 V	P Package		0.065	0.2	
		(see Notes 4 and 5)	SL Package		0.03	0.1	

NOTES: 4. These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The third terminal is connected to the guard terminal of the bridge.
5. Further details on capacitance are given in the Applications Information section.

MARCH 1994 - REVISED OCTOBER 2000

Electrical Characteristics for T and G or R and G Terminals, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	$V_D = \pm V_{DRM}$, 0 °C < T_A < 70 °C				±10	µA
$V_{(BO)}$	Breakover voltage	dv/dt = ±250 V/ms, R_{SOURCE} = 300 Ω	'3240F3			±240	V
			'3260F3			±260	
			'3290F3			±290	
			'3320F3			±320	
			'3380F3			±380	
$V_{(BO)}$	Impulse breakover voltage	dv/dt ≤ ±1000 V/µs, Linear voltage ramp, Maximum ramp value = ±500 V, R_{SOURCE} = 50 Ω	'3240F3		±267		V
			'3260F3		±287		
			'3290F3		±317		
			'3320F3		±347		
			'3380F3		±407		
$I_{(BO)}$	Breakover current	dv/dt = ±250 V/ms, R_{SOURCE} = 300 Ω		±0.1		±0.6	A
V_T	On-state voltage	I_T = ±5 A, t_W = 100 µs				±3	V
I_H	Holding current	I_T = ±5 A, di/dt = -/+30 mA/ms		±0.15			A
dv/dt	Critical rate of rise of off-state voltage	Linear voltage ramp, Maximum ramp value < 0.85V_{DRM}		±5			kV/µs
I_D	Off-state current	V_D = ±50 V				±10	µA
C_{off}	Off-state capacitance	f = 1 MHz, V_d = 0.1 V r.m.s., V_D = 0			57	95	pF
		f = 1 MHz, V_d = 0.1 V r.m.s., V_D = -5 V			26	45	
		f = 1 MHz, V_d = 0.1 V r.m.s., V_D = -50 V (see Notes 5 and 6)			11	20	

NOTES: 6 These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The third terminal is connected to the guard terminal of the bridge.
7. Further details on capacitance are given in the Applications Information section.

Thermal Characteristics

Parameter		Test Conditions		Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to free air thermal resistance	P_{tot} = 0.8 W, T_A = 25 °C, 5 cm^2, FR4 PCB	D Package			160	°C/W
			P Package			100	
			SL Package			135	

APPLICATIONS INFORMATION

Longitudinal Balance

Figure 18 shows a three terminal TISP® device with its equivalent "delta" capacitance. Each capacitance, C_{TG}, C_{RG} and C_{TR}, is the true terminal pair capacitance measured with a three terminal or guarded capacitance bridge. If wire R is biased at a larger potential than wire T, then $C_{TG} > C_{RG}$. Capacitance C_{TG} is equivalent to a capacitance of C_{RG} in parallel with the capacitive difference of $(C_{TG} - C_{RG})$. The line capacitive unbalance is due to $(C_{TG} - C_{RG})$ and the capacitance shunting the line is $C_{TR} + C_{RG}/2$.

All capacitance measurements in this data sheet are three terminal guarded to allow the designer to accurately assess capacitive unbalance effects. Simple two terminal capacitance meters (unguarded third terminal) give false readings as the shunt capacitance via the third terminal is included.

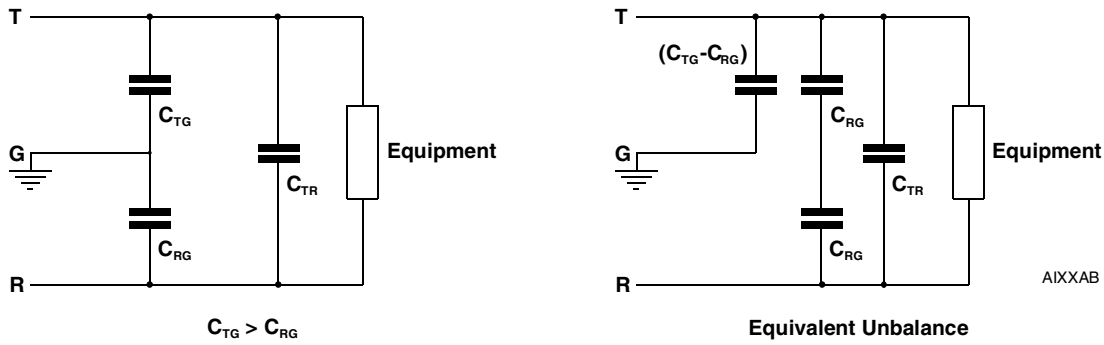


Figure 18.

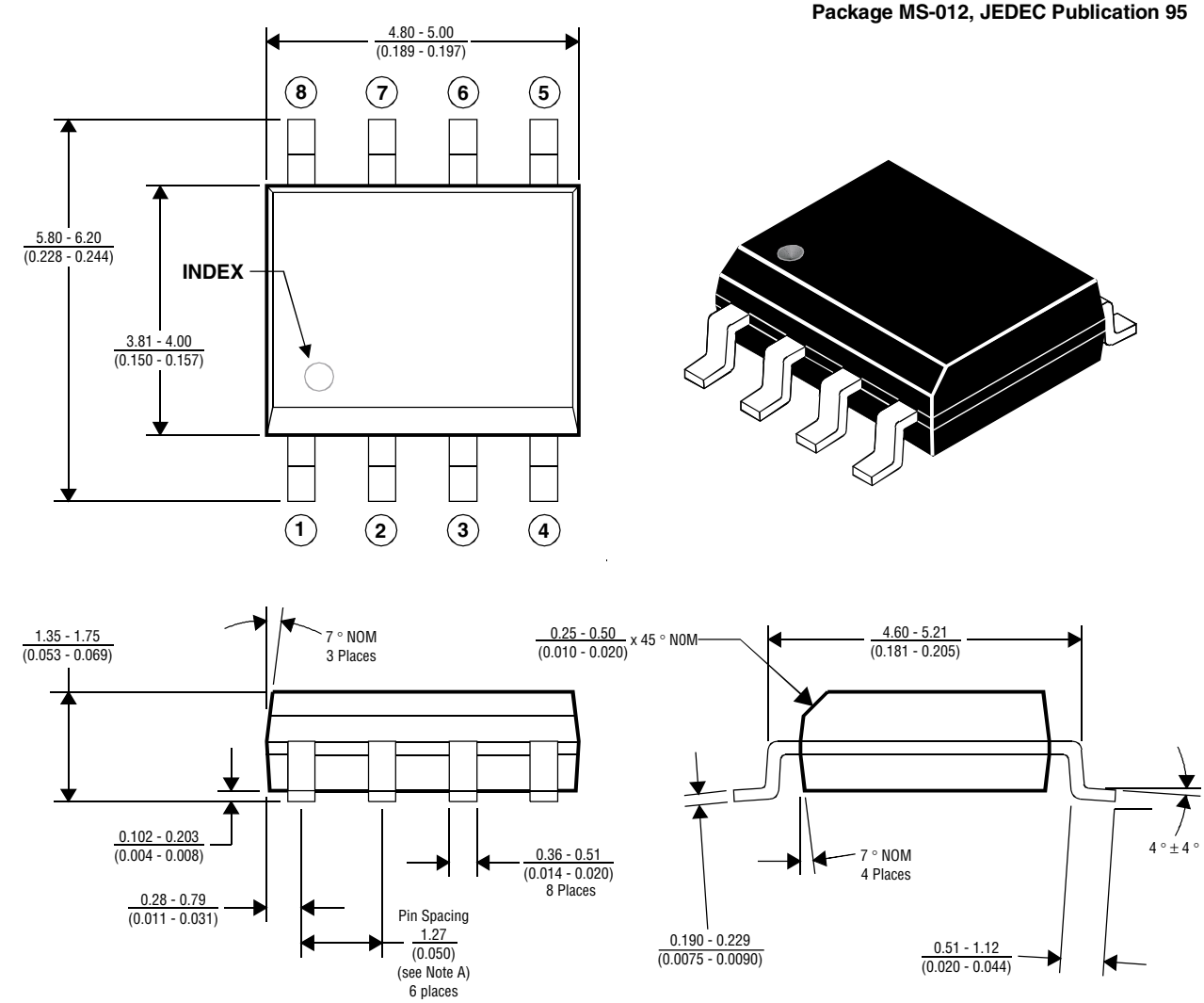
MECHANICAL DATA

D008 Plastic Small-outline Package

This small-outline package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D008

8-pin Small Outline Microelectronic Standard Package MS-012, JEDEC Publication 95



MDXXAAC

NOTES: A. Leads are within 0.25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0.15 (0.006).
D. Lead tips to be planar within ±0.051 (0.002).

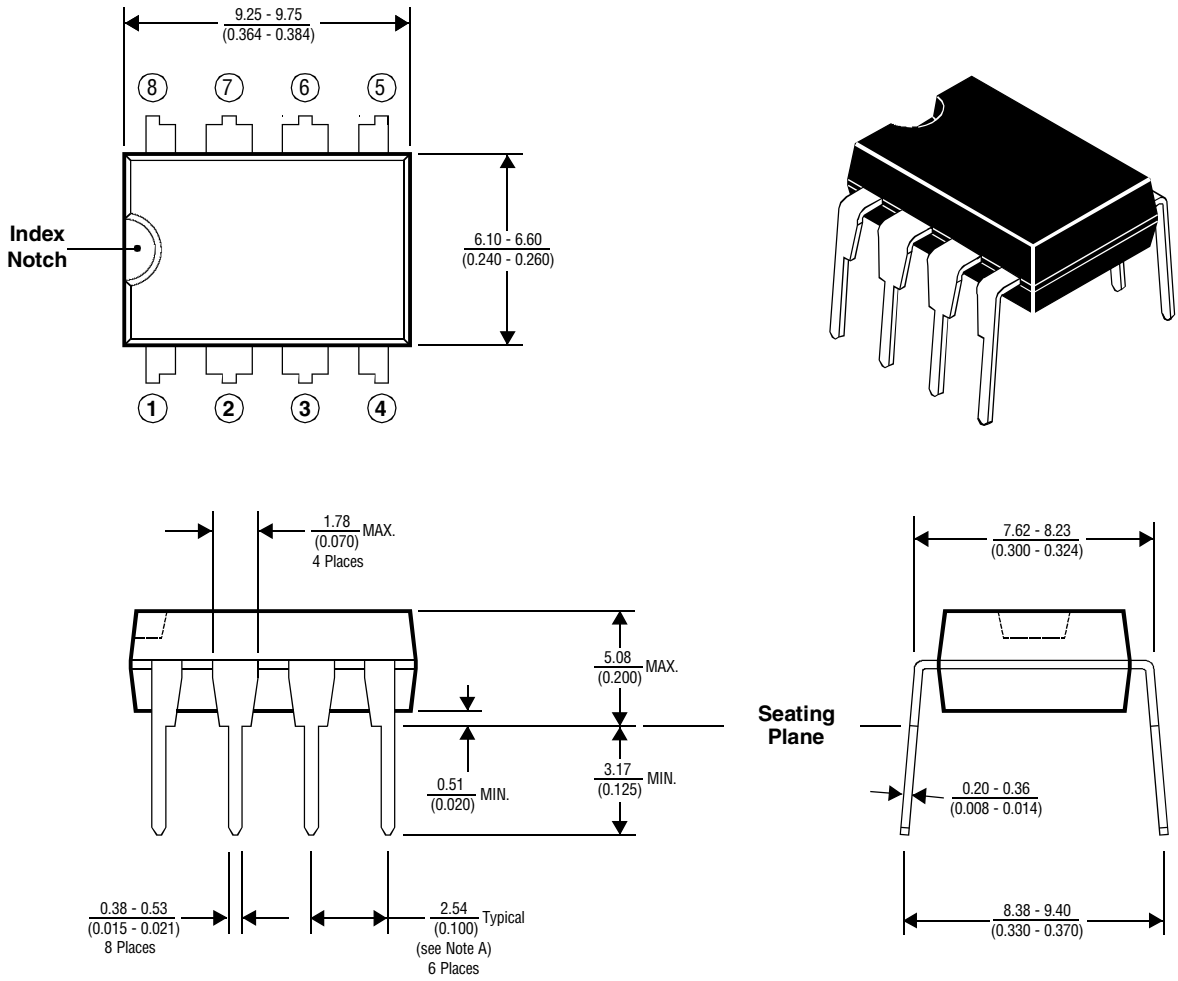
MECHANICAL DATA

D008 Plastic Dual-in-Line Package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. The package is intended for insertion in mounting-hole rows on 7.62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

P008

DIMENSIONS ARE: METRIC / (INCHES)



MDXXCF

NOTES: A. Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.
B. Dimensions fall within JEDEC MS001 - R-PDIP-T, 0.300" Dual-In-Line Plastic Family.