ACPL-785E , HCPL-7850, HCPL-7851, 5962-97557

Hermetically Sealed Analog Isolation Amplifier

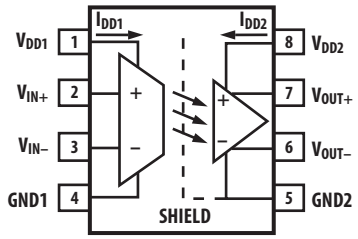
AVAGO TECHNOLOGIES

Data Sheet

Description

The HCPL-7850, HCPL-7851 and ACPL-785E are isolation amplifiers that provide accurate, electrically isolated and amplified representations of voltage and current. When used with a shunt resistor to monitor the motor phase current in a high speed motor drive, the device will offer superior reliability compared with the traditional solutions such as current transformers and Hall-effect sensors. These devices consist of a sigma-delta analog-to-digital converter optically coupled to a digital-to-analog converter in a hermetically sealed package. The products are capable of operation and storage over the full military temperature range and may be purchased as a standard product (HCPL-7850), with full MIL-PRF-38534 Class H testing (HCPL-7851), with MIL-PRF-38534 Class E testing (Class K with exceptions) or from the DLA Standard Micro-circuit Drawing (SMD) 5962-97557. Details of the Class E program may be found on page 16 of this datasheet.

Schematic Diagram



A 0.1 µF bypass capacitor must be connected between pins 1 and 4 and between pins 5 and 8.

Features

- Performance guaranteed over full military temperature range: -55° C to +125° C
- Manufactured and tested on a MIL-PRF-38534 certified line
- Hermetically sealed packages
- Dual marked with device part number and DLA drawing number
- QML-38534, Class H and Class E
- HCPL-7840 function compatibility
- High common mode rejection (CMR): 8 kV/µs at VCM = 1000 V
- 5% gain tolerance
- 0.1% nonlinearity
- Low offset voltage and offset temperature coefficient
- 100 kHz bandwidth

Applications

- Industrial, military and space systems
- High reliability systems
- Harsh industrial environments
- Transportation, medical, and life critical systems
- General purpose analog signal isolation

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Superior performance in design critical specifications such as common-mode rejection, offset voltage, nonlinearity, and operating temperature make the HCPL-7850, HCPL-7851 and ACPL-785E excellent choices for designing reliable products such as motor controllers and inverters.

With common-mode rejection of 8 kV/μs these devices are suitable for noisy electrical environments such as those generated by the high switching rates of power IGBTs.

Low offset voltage together with a low offset voltage temperature coefficient permits accurate use of auto-calibration techniques.

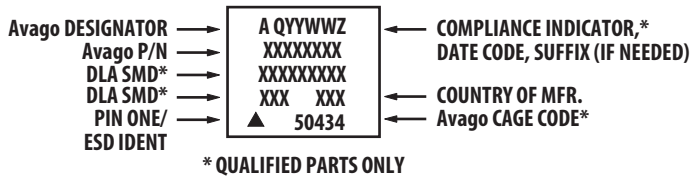
Gain tolerance of 5% with 0.1% nonlinearity further provide the performance necessary for accurate feedback and control.

Selection Guide – Package Styles and Lead Configuration Options

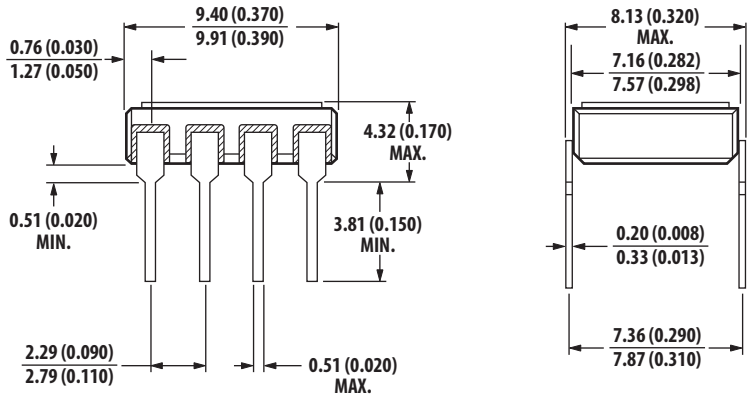
Avago Technologies's Part Number and Options		
Commercial	HCPL-7850	
MIL-PRF-38534, Class H	HCPL-7851	
MIL-PRF-38534, Class E		ACPL-785E
Standard Lead Finish	Gold Plate	Gold Plate
Solder Dipped *	Option #200	Option -200
Butt Cut/Gold Plate	Option #100	Option -100
Gull Wing/Soldered *	Option #300	Option -300
SMD Part Number		
Prescript for all below	5962-	5962-
Gold Plate	9755701HPC	9755701EPC
Solder Dipped *	9755701HPA	9755701EPA
Butt Cut/Gold Plate	9755701HYC	9755701EYC
Butt Cut/Soldered *	9755701HYA	9755701EYA
Gull Wing/Soldered *	9755701HXA	9755701EXA

*Solder contains lead.

Device Marking



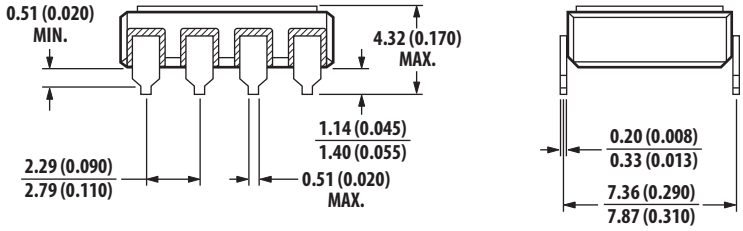
Outline Drawing



NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

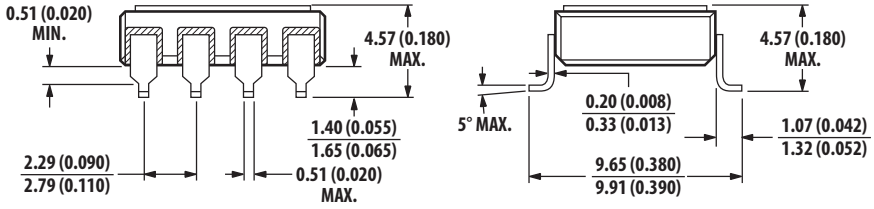
Hermetic Optocoupler Options

Option	Description
100	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product in 8 pin DIP (see drawings below for details).



NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

200	Lead finish is solder dipped rather than gold plated. This option is available on commercial and hi-rel product in 8 pin DIP. DLA Drawing part numbers contain provisions for lead finish.
300	Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product in 8 pin DIP (see drawings below for details). This option has solder dipped leads.



NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Solder contains lead.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-65	+150	°C	
Operating Temperature	T_A	-55	+125	°C	
Supply Voltages	V_{DD1}, V_{DD2}	0.0	+5.5	V	
Steady-State Input Voltage	V_{IN+}, V_{IN-}	-2.0	V_{DD1} + 0.5	V	1
2 Second Transient Input Voltage		-6.0	V_{DD1} + 0.5	V	1
Output Voltages	V_{OUT+}, V_{OUT-}	-0.5	V_{DD2} + 0.5	V	
Lead Solder Temperature			260 for 10 sec	°C	

ESD Classification (MIL-STD-883, Method 3015)

HCPL-7850, HCPL-7851 and ACPL-785E	(▲); Class 1

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltages	V_{DD1}, V_{DD2}	4.5	5.5	Volts
Input Voltage (See Note 1)	V_{IN+}, V_{IN-}	-200	+200	mV

DC Electrical Specifications

Over recommended operating conditions (T_A = -55° C to +125° C, V_{IN+} = 0 V, V_{IN-} = 0 V, V_{DD1} = 5 V and V_{DD2} = 5 V, unless otherwise specified).

Parameter	Symbol	Group A[12] Subgroups	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input Offset Voltage	V_{OS}	1, 2 ,3	-1.0	0.6	5.0	mV	4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	1, 2, 3	2
Gain	G	2, 3	7.36	8.00	8.64	V/V	-200 mV ≤ V_{IN+} ≤ 200 mV, 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	5, 6, 7	
		1	7.60	8.00	8.4				
200 mV Nonlinearity	NL_{200}	2, 3		0.05	0.8	%	-200 mV ≤ V_{IN+} ≤ 200 mV, 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	5, 8, 9, 10, 12	3
		1		0.05	0.2				
100 mV Nonlinearity	NL_{100}	2, 3		0.01	0.2		-100 mV ≤ V_{IN+} ≤ 100 mV, 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	5, 8, 9, 11, 12	
		1		0.01	0.1				
Output Common-Mode Voltage	V_{OCM}	1, 2, 3	2.20	2.56	2.80	V	-400 mV ≤ V_{IN+} ≤ 400 mV, 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V		
Input Supply Current	I_{DD1}	1, 2, 3		10.7	15.5	mA		14,17	
Output Supply Current	I_{DD2}	1, 2, 3		9.4	14.5	mA		15,17	
Input-Output Insulation Leakage Current	I_{I-O}	1			1.0	μA	RH ≤ 65%, t = 5 sec. V_{I-O} = 1500 Vdc, T_A = 25° C		11
Maximum Input Voltage Before Output Clipping	$\|V_{IN+}\|$ MAX			320		mV		4, 12	
Average Input Bias Current	I_{IN}			-0.57		μA		13	4
Average Input Resistance	R_{IN}			480		kΩ			
Input DC Common-Mode Rejection Ratio	$CMRR_{IN}$			69		dB			5
Output Resistance	R_O			1		Ω			
Output Low Voltage	V_{OL}			1.28		V	V_{IN+} = 400 mV	4	6
Output High Voltage	V_{OH}			3.84		V	V_{IN+} = -400 mV		
Output Short-Circuit Current	$\|I_{OSC}\|$			11		mA	V_{OUT} = 0 V or V_{DD2}		7
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 Vdc		11
Capacitance (Input–Output)	C_{I-O}			2.7		pF	f = 1 MHz V_{I-O} = 0 Vdc		

* All typicals are at the nominal operating conditions of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25° C, V_{DD1} = 5 V and V_{DD2} = 5 V.

AC Electrical Specifications

Over recommended operating conditions (T_A = -55° C to +125° C, V_{IN+} = 0 V, V_{IN-} = 0 V, V_{DD1} = 5 V and V_{DD2} = 5 V, unless otherwise specified).

Parameter	Symbol	Group A[12] Subgroups	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Common Mode Rejection	CMR	9	5	8	5.0	kV/µs	V_{CM} = 1 kV 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V, T_A = 25° C	16	8, 13
Propagation Delay to 50%	t_{PD50}	9, 10, 11		3.7	7.5	µs	V_{IN+} = 0 to 100 mV step 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	18, 19	
Propagation Delay to 90%	t_{PD90}	9, 10, 11		5.7	11.0				
Rise/Fall Time (10-90%)	$t_{R/F}$	9, 10, 11		3.4	7.5				
Small-Signal Bandwidth (-3 dB)	$f_{-3\ dB}$	9, 10, 11	45	100		kHz	4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V V_{IN+} = 200 mVpk-pk	18, 20, 21	14
Small-Signal Bandwidth (-45°)	$f_{-45°}$			31					
RMS Input-Referred Noise	V_N			0.6		mV_{rms}	In recommended application circuit	22, 24	9
Power Supply Rejection	PSR			570		mV_{P-P}			10

* All typicals are at the nominal operating conditions of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25° C, V_{DD1} = 5 V and V_{DD2} = 5 V.

Notes:

1. If V_{IN-} is brought above V_{DD1} -2 V with respect to GND1 an internal test mode may be activated. This test mode is not intended for customer use.
2. Exact offset value is dependent on layout of external bypass capacitors. The offset value in the data sheet corresponds to Avago's recommended layout (see Figures 26 and 27).
3. Nonlinearity is defined as half of the peak-to-peak output deviation from the best-fit gain line, expressed as a percentage of the full-scale differential output voltage.
4. Because of the switched capacitor nature of the sigma-delta A/D converter, time averaged values are shown.
5. $CMRR_{IN}$ is defined as the ratio of the gain for differential inputs applied between pins 2 and 3 to the gain for both common mode inputs applied to both pins 2 and 3 with respect to pin 4.
6. When the differential input signal exceeds approximately 320 mV, the outputs will limit at the typical values shown.
7. Short-circuit current is the amount of output current generated when either output is shorted to V_{DD2} or ground. Avago does not recommend operations under these conditions.
8. CMR (also known as IMR or Isolation Mode Rejection) specifies the minimum rate of rise of a common mode signal applied across the isolation boundary at which small output perturbations begin to occur. These output perturbations can occur with both the rising and falling edges of the common mode waveform and may be of either polarity. A CMR failure is defined as a perturbation exceeding 200 mV at the output of the recommended application circuit (Figure 24). See Applications section for more information on CMR.
9. Output noise comes from two primary sources: chopper noise and sigma-delta quantization noise. Chopper noise results from chopper stabilization of the output op-amps. It occurs at a specific frequency (typically 500 kHz) and is not attenuated by the on-chip output filter. The on-chip filter does eliminate most, but not all, of the sigma-delta quantization noise. An external filter circuit may be easily added to the external post-amplifier to reduce the total RMS output noise. See Applications section for more information.
10. Data sheet value is the amplitude of the transient at the differential output of the device when a 1 V_{P-P}, 1 MHz square wave with 100 ns rise and fall times (measured at pins 1 and 8) is applied to both V_{DD1} and V_{DD2}.
11. Device considered a two-terminal device: Pins 1, 2, 3, and 4 are shorted together and pins 5, 6, 7, and 8 are shorted together.
12. Commercial parts receive 100% testing at 25° C (Subgroups 1 and 9). Hi-Rel and SMD parts receive 100% testing at 25° C, +125° C and -55° C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
13. Parameters are tested as part of device initial characterization and after design and process changes only. Parameters are guaranteed to limits specified for all lots not specifically tested.
14. The f_{-3dB} test is guaranteed by the T_{RISE} test.

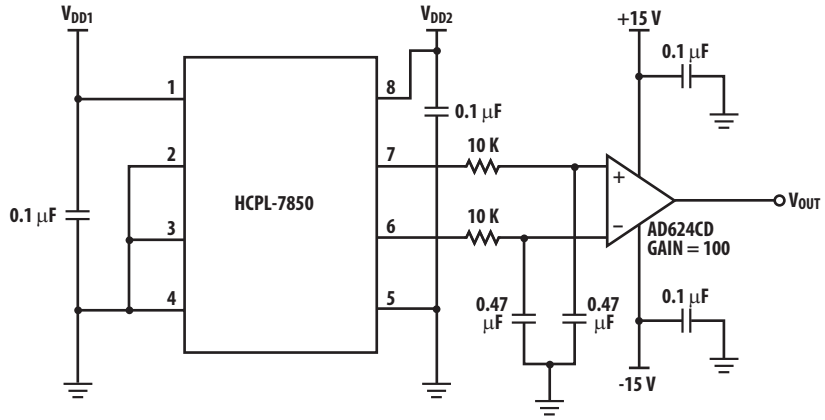


Figure 1. Input Offset Voltage Test Circuit.

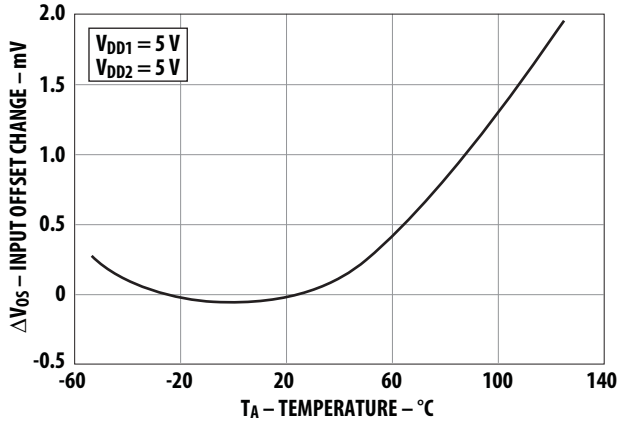


Figure 2. Input Offset Change vs. Temperature.

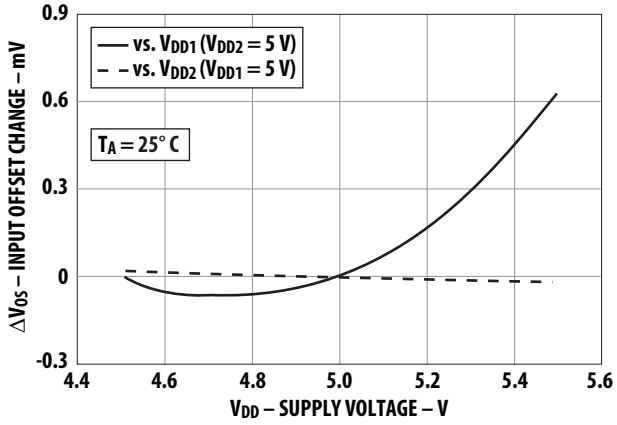


Figure 3. Input Offset Change vs. V_{DD1} and V_{DD2}.

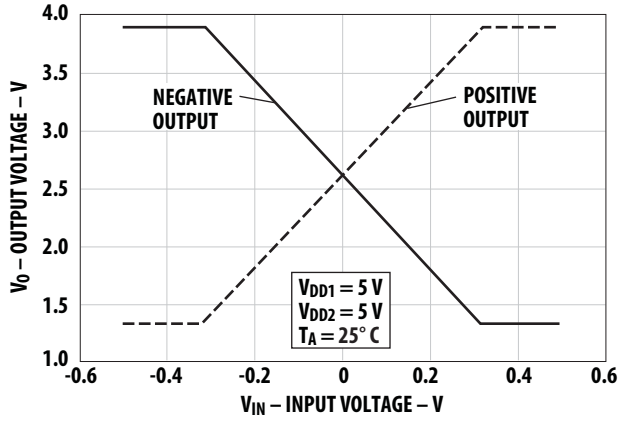


Figure 4. Output Voltages vs. Input Voltage.

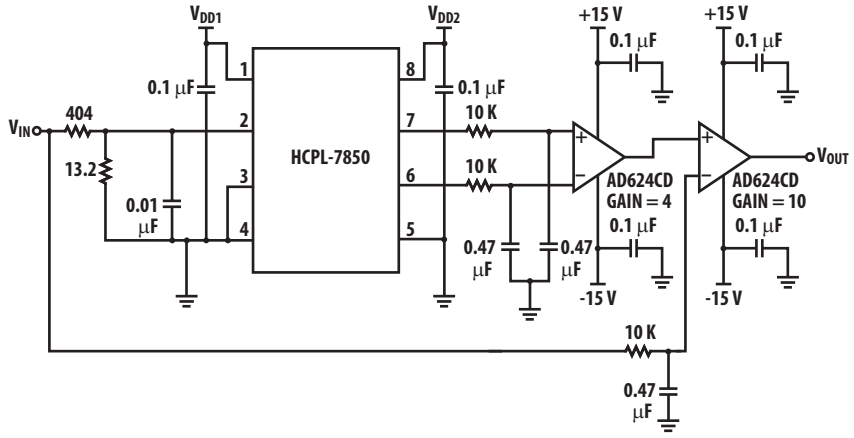


Figure 5. Gain and Nonlinearity Test Circuit.

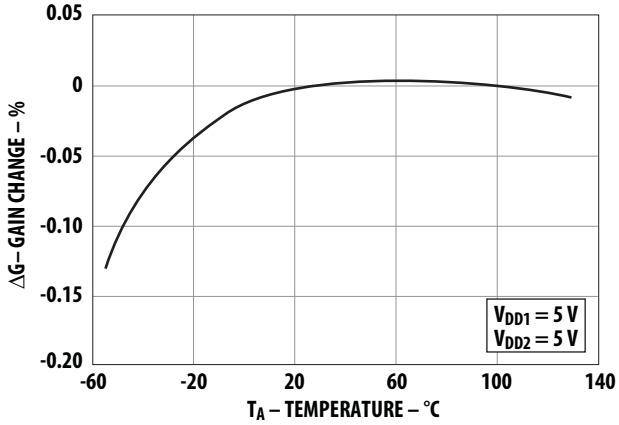


Figure 6. Gain Change vs. Temperature.

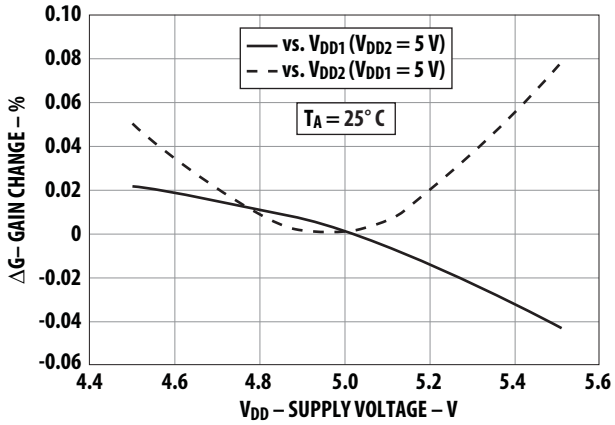


Figure 7. Gain Change vs. V_{DD1} and V_{DD2}.

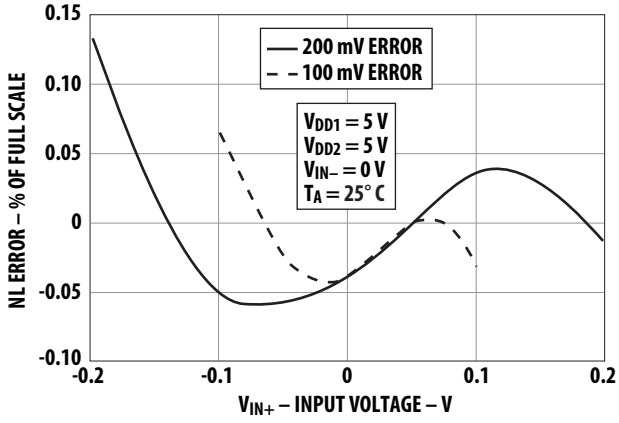


Figure 8. Nonlinearity Error Plot vs. Input Voltage.

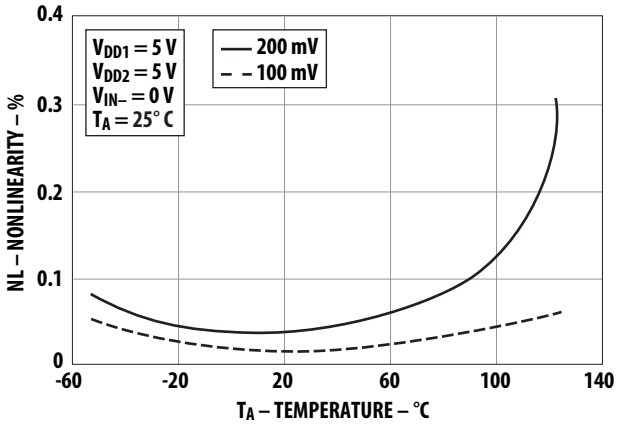


Figure 9. Nonlinearity vs. Temperature.

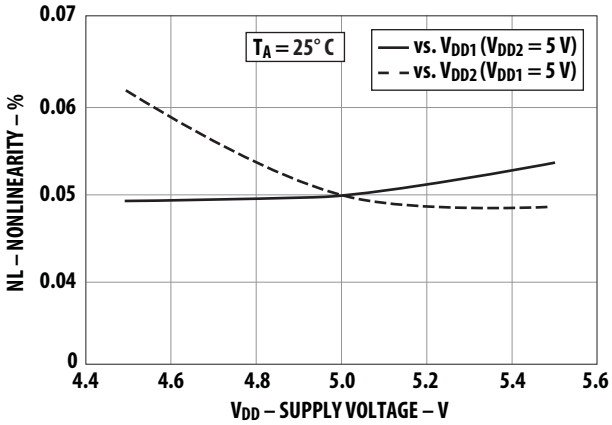


Figure 10. 200 mV Nonlinearity vs. V_{DD1} and V_{DD2}.

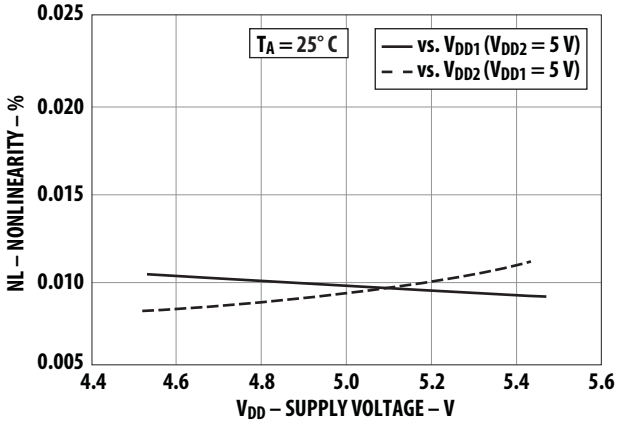


Figure 11. 100 mV Nonlinearity vs. V_{DD1} and V_{DD2}.

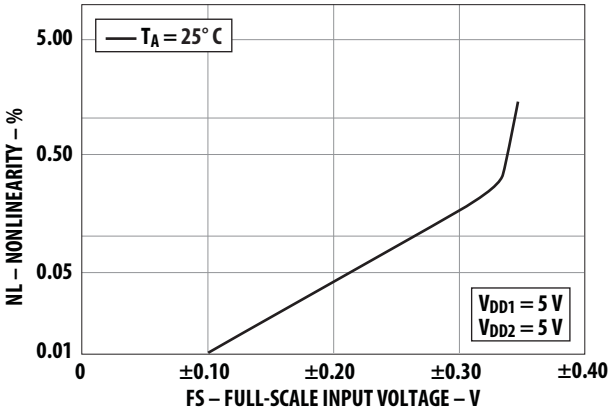


Figure 12. Nonlinearity vs. Full-Scale Input Voltage.

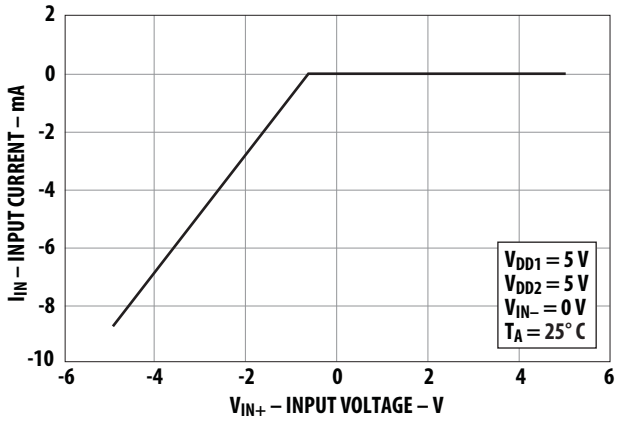


Figure 13. Input Current vs. Input Voltage.

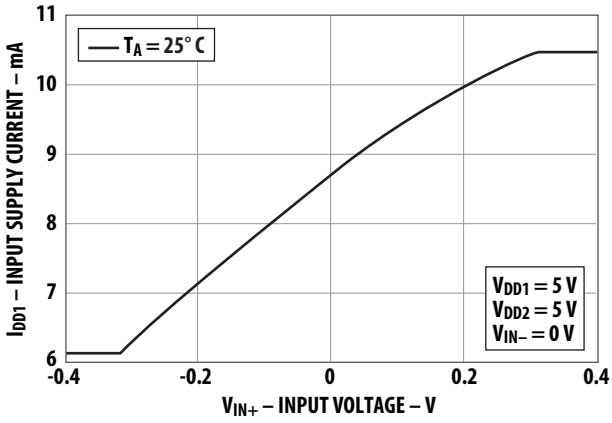


Figure 14. Input Supply Current vs. Input Voltage.

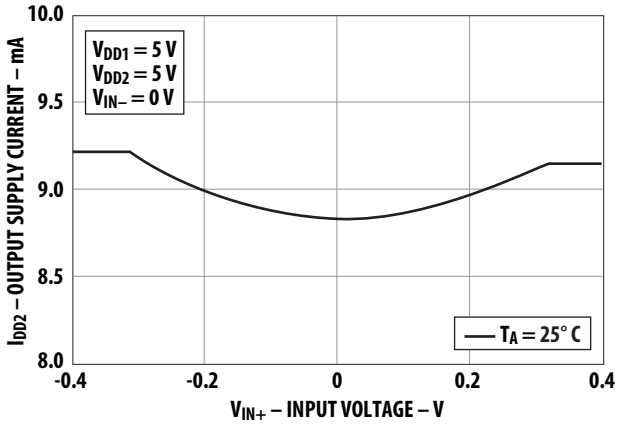


Figure 15. Output Supply Current vs. Input Voltage.

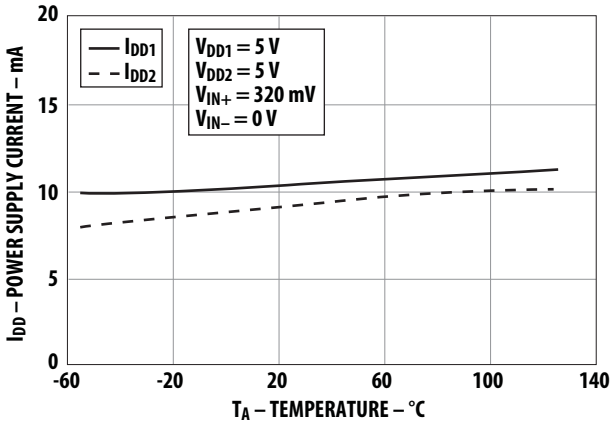


Figure 17. Input and Output Supply Current vs. Temperature.

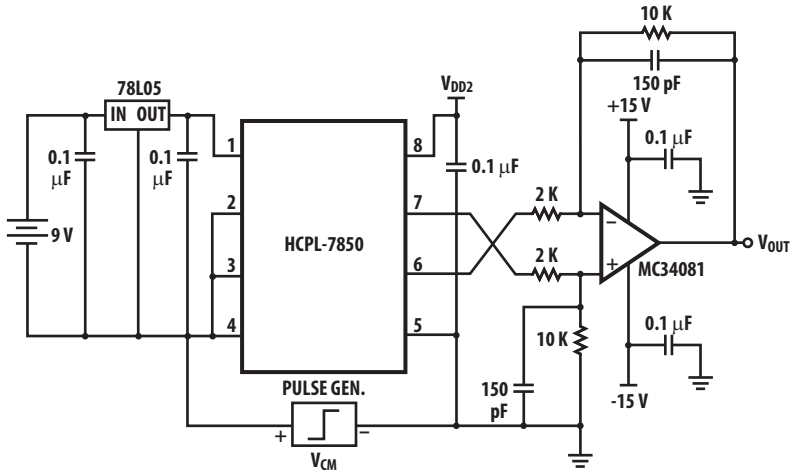
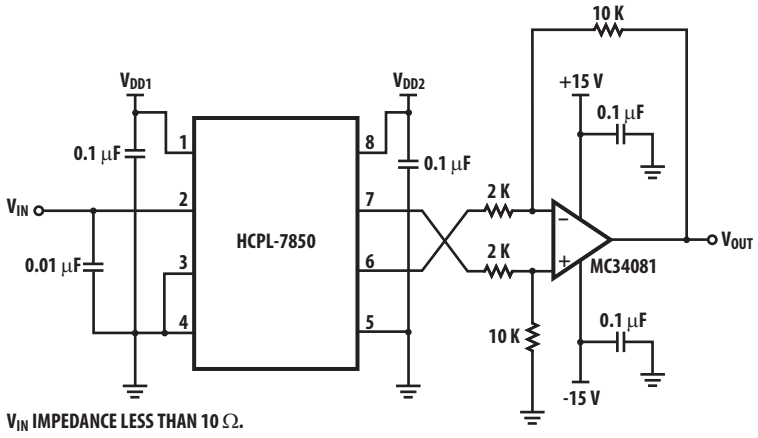


Figure 16. Common Mode Rejection Test Circuit.



V_{IN} IMPEDANCE LESS THAN 10 Ω.

Figure 18. Propagation Delay, Rise/Fall Time and Bandwidth Test Circuit.

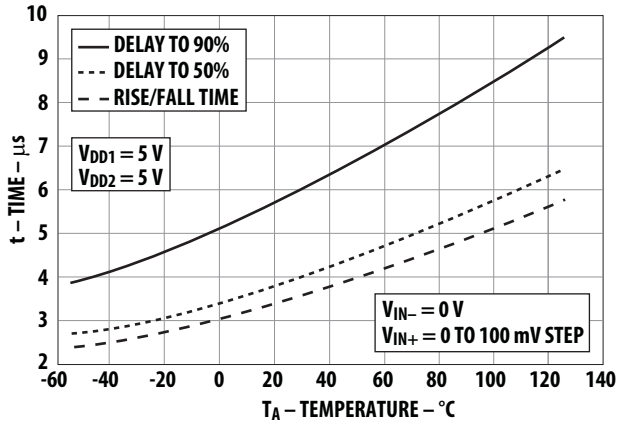


Figure 19. Propagation Delays and Rise/Fall Time vs. Temperature.

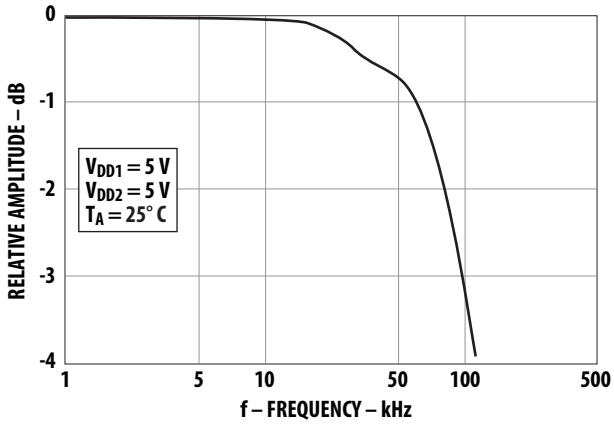


Figure 20. Amplitude Response vs. Frequency.

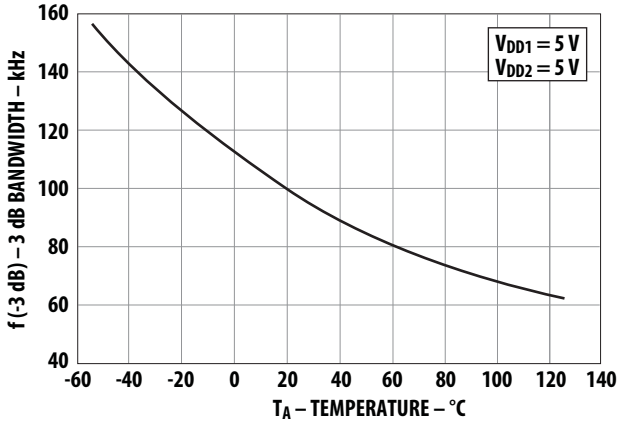


Figure 21. 3 dB Bandwidth vs. Temperature.

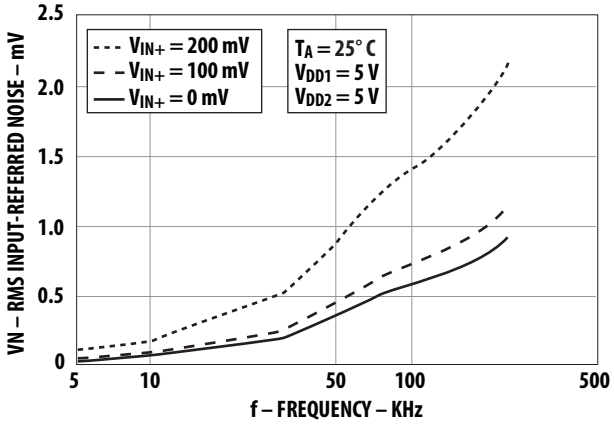


Figure 22. RMS Input-Referred Noise vs. Recommended Application Circuit Bandwidth.

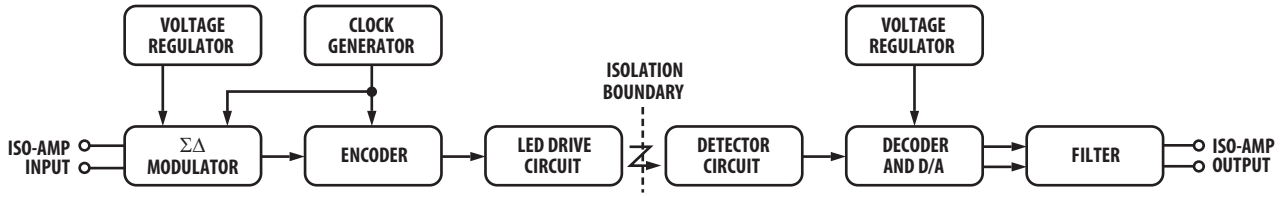


Figure 23. HCPL-7850 Block Diagram.

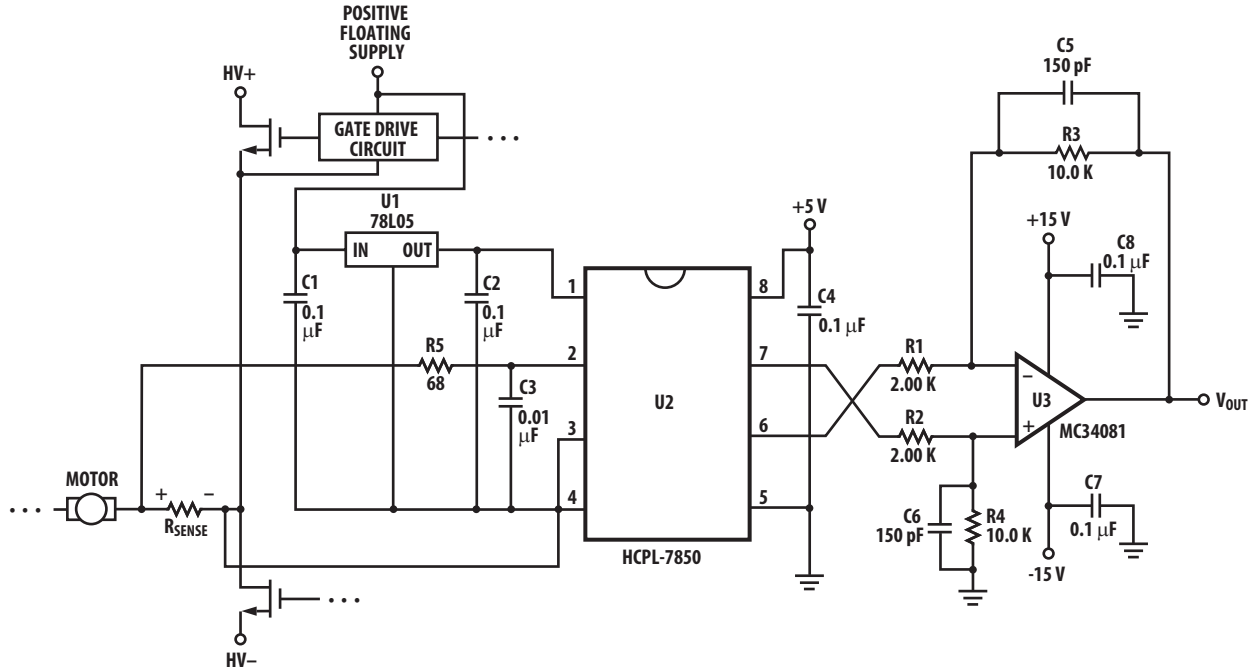


Figure 24. Recommended Application Circuit.

Applications Information

Functional Description

Figure 23 shows the primary functional blocks of the HCPL-7850. In operation, the sigma-delta modulator converts the analog input signal into a high-speed serial bit stream. The time average of this bit stream is directly proportional to the input signal. This stream of digital data is encoded and optically transmitted to the detector circuit. The detected signal is decoded and converted back into an analog signal, which is filtered to obtain the final output signal.

Application Circuit

The recommended application circuit is shown in Figure 24. A floating power supply (which in many applications could be the same supply that is used to drive the high-side power transistor) is regulated to 5 V using a simple three-terminal voltage regulator (U1). The voltage from the current sensing resistor, or shunt (Rsense), is applied to the input of the HCPL-7850 through an RC anti-aliasing filter (R5, C3). And finally, the differential output of the isolation amplifier is converted to a ground-referenced single-ended output voltage with a simple differential amplifier circuit (U3 and associated components). Although the application circuit is relatively simple, a few recommendations should be followed to ensure optimal performance.

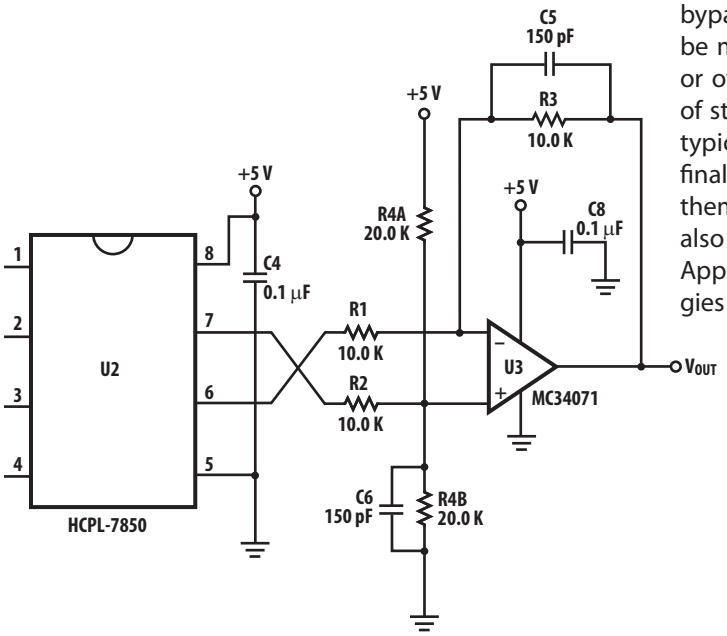


Figure 25. Single-Supply Post-Amplifier Circuit.

Supplies and Bypassing

As mentioned above, an inexpensive three-terminal regulator can be used to reduce the gate-drive power supply voltage to 5 V. To help attenuate high frequency power supply noise or ripple, a resistor or inductor can be used in series with the input of the regulator to form a low-pass filter with the regulator's input bypass capacitor.

As shown in Figure 24, a 0.1 µF bypass capacitor (C2, C4) should be located as close as possible to the input and output power supply pins of the HCPL-7850. The bypass capacitors are required because of the high-speed digital nature of the signals inside the isolation amplifier. A 0.01 µF bypass capacitor (C3) is also recommended at the input pin(s) due to the switched-capacitor nature of the input circuit. The input bypass capacitor should be at least 1000 pF to maintain gain accuracy of the isolation amplifier.

Inductive coupling between the input power-supply capacitor and the input circuit, including the input bypass capacitor and the input leads of the HCPL-7850, can introduce additional DC offset in the circuit. Several steps can be taken to minimize the mutual coupling between the two parts of the circuit, thereby improving the offset performance of the design. Separate the two bypass capacitors C2 and C3 as much as possible (even putting them on opposite sides of the PC board), while keeping the total lead lengths, including traces, of each bypass capacitor less than 20 mm. PC board traces should be made as short as possible and placed close together or over ground plane to minimize loop area and pickup of stray magnetic fields. Avoid using sockets, as they will typically increase both loop area and inductance. And finally, using capacitors with small body size and orienting them perpendicular to each other on the PC board can also help. For more information concerning this effect, see Application Note 1078, Designing with Avago Technologies Isolation Amplifiers.

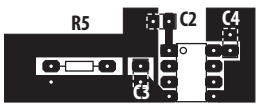


Figure 26. Top Layer of Printed Circuit Board Layout.

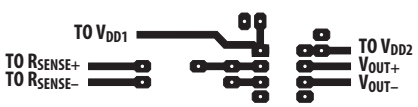


Figure 27. Bottom Layer of a Printed Circuit Board Layout.

Shunt Resistor Selections

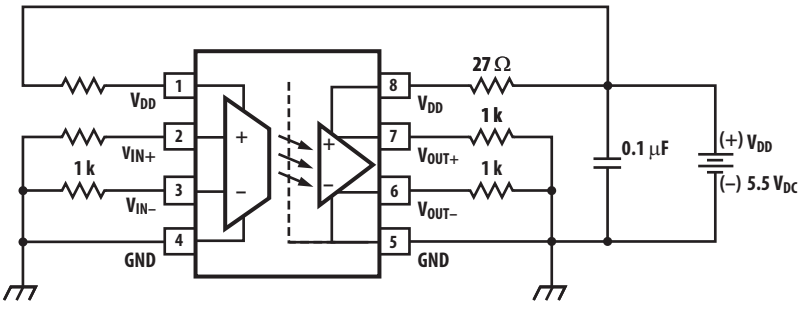
The current-sensing shunt resistor should have low resistance (to minimize power dissipation), low inductance (to minimize di/dt induced voltage spikes which could adversely affect operation), and reasonable tolerance (to maintain overall circuit accuracy). The value of the shunt should be chosen as a compromise between minimizing power dissipation by making the shunt resistance smaller and improving circuit accuracy by making it larger and utilizing the full input range of the HCPL-7850. Avago Technologies recommends four different shunts which can be used to sense average currents in motor drives up to 35 A and 35 hp. Table 1 shows the maximum current and horsepower range for each of the LVR-series shunts from Dale. Even higher currents can be sensed with lower value shunts available from vendors such as Dale, IRC, and Isotek (Isabellenhuette). When sensing currents large enough to cause significant heating of the shunt, the temperature coefficient of the shunt can introduce nonlinearity due to the signal dependent temperature rise of the shunt. Using a heat sink for the shunt or using a shunt with a lower tempco can help minimize this effect. The Application Note 1078, Designing with Avago Technologies Isolation Amplifiers, contains additional information on designing with current shunts.

The recommended method for connecting the isolation amplifier to the shunt resistor is shown in Figure 24. Pin 2 (VIN+) is connected to the positive terminal of the shunt resistor, while pin 3 (VIN–) is shorted to pin 4 (GND1), with the power-supply return path functioning as the sense line to the negative terminal of the current shunt. This allows a single pair of wires or PC board traces to connect the isolation amplifier circuit to the shunt resistor. In some applications, however, supply currents flowing through the power-supply return path may cause offset or noise problems. In this case, better performance may be obtained by connecting pin 3 to the negative terminal of the shunt resistor separate from the power supply return path. When connected this way, both input pins should be bypassed. Whether two or three wires are used, it is recommended that twisted-pair wire or very close PC board traces be used to connect the current shunt to the isolation amplifier circuit to minimize electromagnetic interference to the sense signal.

The 68 Ω resistor in series with the input lead forms a low-pass anti-aliasing filter with the input bypass capacitor with a 200 kHz bandwidth. The resistor performs another important function as well; it dampens any ringing which might be present in the circuit formed by the shunt, the input bypass capacitor, and the wires or traces connecting the two. Undampened ringing of the input circuit near the input sampling frequency can alias into the baseband producing what might appear to be noise at the output of the device. To be effective, the damping resistor should be at least 39 Ω.

PC Board Layout

In addition to affecting offset, the layout of the PC board can also affect the common mode rejection (CMR) performance of the isolation amplifier, due primarily to stray capacitive coupling between the input and the output circuits. To obtain optimal CMR performance, the layout of the printed circuit board (PCB) should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground plane on the PCB does not pass directly below the HCPL-7850. Using surface mount components can help achieve many of the PCB objectives discussed in the preceding paragraphs. An example through-hole PCB layout illustrating some of the more important layout recommendations is shown in Figures 26 and 27. See Applications Note 1078, Designing with Avago Technologies Isolation Amplifiers, for more information on PCB layout consideration.



CONDITIONS: I_{CC} = 17.5 mA
T_A = +125° C

Figure 28. Operating Circuit for Burn-In and Steady State Life Tests.

Post-Amplifier Circuit

The recommended application circuit (Figure 24) includes a post-amplifier circuit that serves three functions: to reference the output signal to the desired level (usually ground), to amplify the signal to appropriate levels, and to help filter output noise. The particular op-amp used in the post-amp is not critical; however, it should have low enough offset and high enough bandwidth and slew rate so that it does not adversely affect circuit performance. The offset of the op-amp should be low relative to the output offset of the HCPL-7850, or less than about 5 mV.

To maintain overall circuit bandwidth, the post-amplifier circuit should have a bandwidth at least twice the minimum bandwidth of the isolation amplifier, or about 200 kHz. To obtain a bandwidth of 200 kHz with a gain of 5, the op-amp should have a gain-bandwidth greater than 1 mHz. The post-amplifier circuit includes a pair of capacitors (C5 and C6) that form a single-pole low-pass filter. These capacitors allow the bandwidth of the post-amp to be adjusted independently of the gain and are useful for reducing the output noise from the isolation amplifier (doubling the capacitor values halves the circuit bandwidth). The component values shown in Figure 24 form a differential amplifier with a gain of 5 and a cutoff frequency of approximately 100 kHz, and were chosen as a compromise between low noise and fast response times. The overall recommended application circuit has a bandwidth of 66 kHz, a rise time of 5.2 μs and a delay to 90% of 8.5 μs.

The gain-setting resistors in the post-amp should have a tolerance of 1% or better to ensure adequate CMRR and gain tolerance for the overall circuit. Resistor networks with even better ratio tolerances can be used which offer better performance, as well as reducing the total component count and board space.

The post-amplifier circuit can be easily modified to allow for single-supply operation. Figure 25 shows a schematic for a post amplifier for use in 5 V single supply applications. One additional resistor is needed and the gain is decreased to 1 to allow circuit operation over the full input voltage range. See Application Note 1078, Designing with Avago Technologies Isolation Amplifiers, for more information on the post-amplifier circuit.

Other Information

As mentioned above, reducing the bandwidth of the post amplifier circuit reduces the amount of output noise. Figure 22 shows how the output noise changes as a function of the post-amplifier bandwidth. The post-amplifier circuit exhibits a first-order low-pass filter characteristic. For the same filter bandwidth, a higher-order filter can achieve even better attenuation of modulation noise due to the second-order noise shaping of the sigma-delta modulator. For more information on the noise characteristics of the HCPL-7850, see Application Note 1078, Designing with Avago Technologies Isolation Amplifiers.

The HCPL-7850 can also be used to isolate signals with amplitudes larger than its recommended input range through the use of a resistive voltage divider at its input. The only restrictions are that the impedance of the divider be relatively small (less than 1 KΩ so that the input resistance (480 KΩ) and input bias current (0.6 μA) do not affect the accuracy of the measurement. An input bypass capacitor is still required, although the 68 Ω series damping resistor is not. (The resistance of the voltage divider provides the same function.) The low pass filter formed by the divider resistance and the input bypass capacitor may limit the achievable bandwidth.

Table 1. Current Shunt Summary

Shunt Resistor Part Number	Shunt Resistance	Maximum Power Dissipation	Maximum Average Current	Maximum Horsepower Range
LVR-3.05-1%	50 mΩ	3 W	3 A	0.8 to 3.0 hp
LVR-3.02-1%	20 mΩ	3 W	8 A	2.2 to 8.0 hp
LVR-3.01-1%	10 mΩ	3 W	15 A	4.1 to 15 hp
LVR-5.005-1%	5 mΩ	5 W	35 A	9.6 to 35 hp

MIL-PRF-38534 Class H, Class E and DLA SMD Test Program

Class H:

Avago Technologies' Hi-Rel Optocouplers are in compliance with MIL-PRF-38534 Class H. Class H devices are also in compliance with DLA drawing 5962-97557.

Testing consists of 100% screening and quality conformance inspection to MIL-PRF-38534.

Class E:

Class E devices are in compliance with DLA drawing 5962-9755701Exx. Avago Technologies has defined the Class E device on this drawing to be based on the Class K requirements of MIL-PRF-38534 with exceptions. The exceptions are as follows:

1. Nondestructive Bond Pull, Test method 2023 of MIL-STD-883 in screening is not required.
2. Particle Impact Noise Detection (PIND), Test method 2020 of MIL-STD-883 in device screening and group C testing is not required.
3. Die Shear Strength, Test method 2019 of MIL-STD-883 in group B testing is not required.
4. Internal Water Vapor Content, Test method 1018 of MIL-STD-883 in group C is not required.
5. Scanning Electron Microscope (SEM) inspection, Test method 2018 of MIL-STD-883 in element evaluation is not required.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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