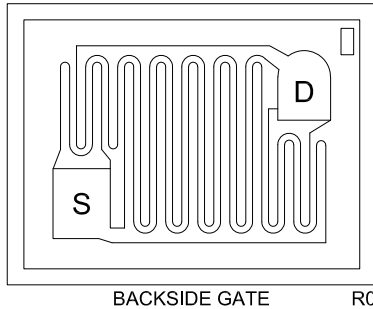


The CP216-2N4856 is a silicon N-Channel small signal JFET designed for analog switching and chopper applications.



MECHANICAL SPECIFICATIONS:

Die Size	21 x 16 MILS
Die Thickness	7.9 MILS
Drain Bonding Pad Size	3.3 x 4.5 MILS
Source Bonding Pad Size	3.3 x 4.5 MILS
Top Side Metalization	Al – 10,000Å
Back Side Metalization	Au – 3,250Å
Scribe Alley Width	2.0 MILS
Wafer Diameter	4 INCHES
Gross Die Per Wafer	29,732

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

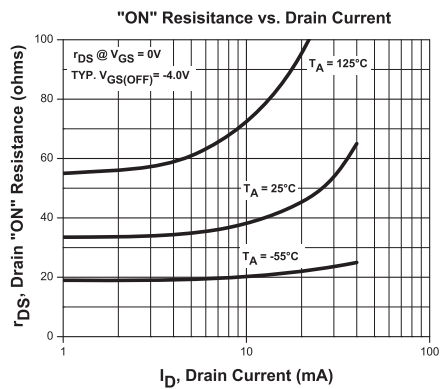
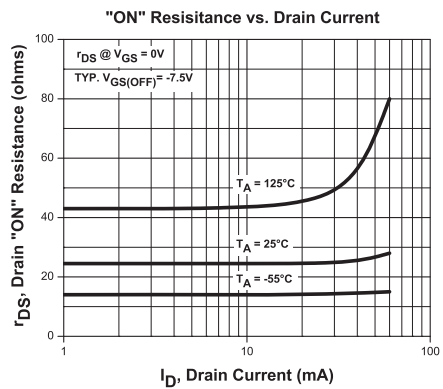
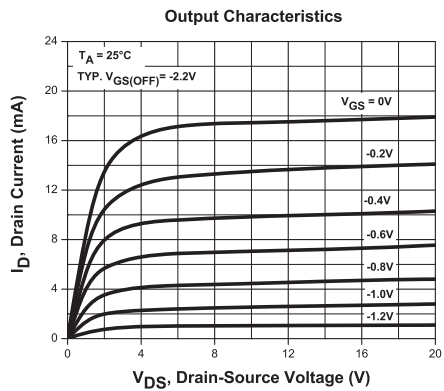
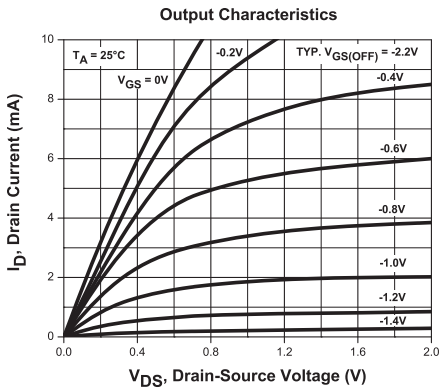
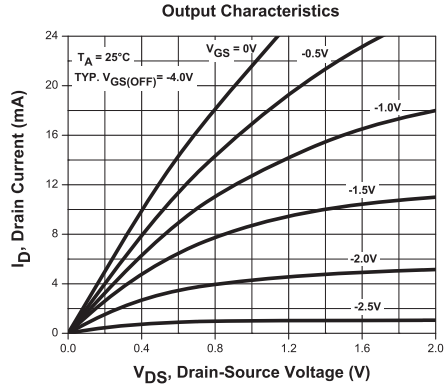
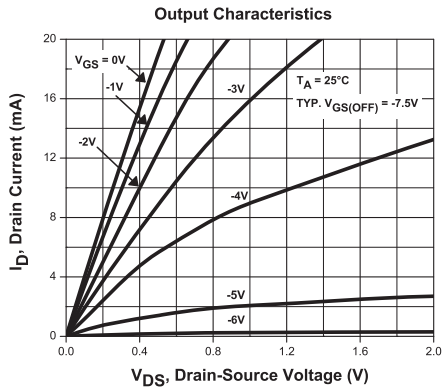
	SYMBOL		UNITS
Drain-Source Voltage	V_{DS}	40	V
Drain-Gate Voltage	V_{DG}	40	V
Reverse Gate-Source Voltage	V_{GSR}	40	V
Forward Gate Current	I_{GF}	50	mA
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +175	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
I_{GSS}	$V_{GS}=20\text{V}, V_{DS}=0$		0.25	nA
I_{DSS}	$V_{DS}=15\text{V}, V_{GS}=0$	50		mA
$I_{D(OFF)}$	$V_{DS}=15\text{V}, V_{GS}=10\text{V}$		0.25	nA
BV_{GSS}	$I_G=1.0\mu\text{A}, V_{DS}=0$	40		V
$V_{GS(OFF)}$	$V_{DS}=15\text{V}, I_D=0.5\text{nA}$	4.0	10	V
$V_{DS(ON)}$	$I_D=20\text{mA}, V_{GS}=0$		0.75	V
$r_{DS(ON)}$	$V_{GS}=0, I_D=0, f=1.0\text{kHz}$		25	Ω
C_{rss}	$V_{GS}=10\text{V}, V_{DS}=0, f=1.0\text{MHz}$		8.0	pF
C_{iss}	$V_{GS}=10\text{V}, V_{DS}=0, f=1.0\text{MHz}$		18	pF
t_d	$V_{DD}=10\text{V}, V_{GS(OFF)}=10\text{V}, I_D=20\text{mA}$		6.0	ns
t_r	$V_{DD}=10\text{V}, V_{GS(OFF)}=10\text{V}, I_D=20\text{mA}$		3.0	ns
t_{off}	$V_{DD}=10\text{V}, V_{GS(OFF)}=10\text{V}, I_D=20\text{mA}$		25	ns

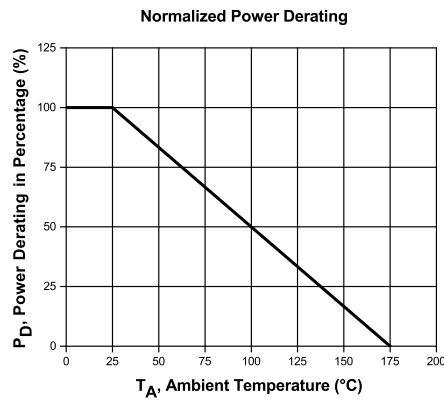
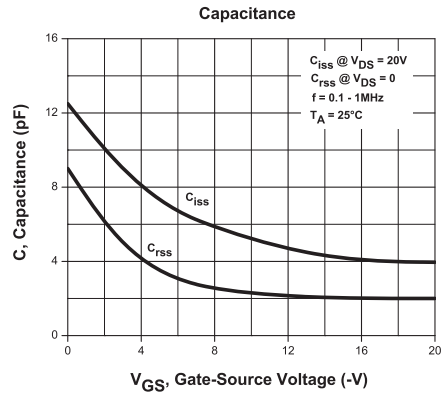
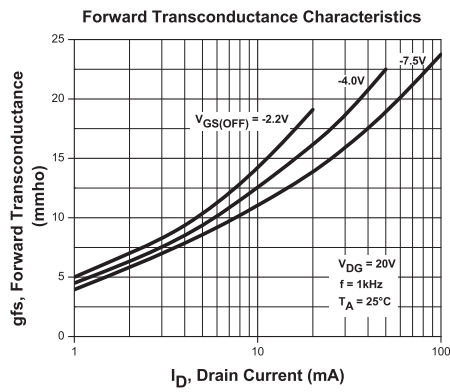
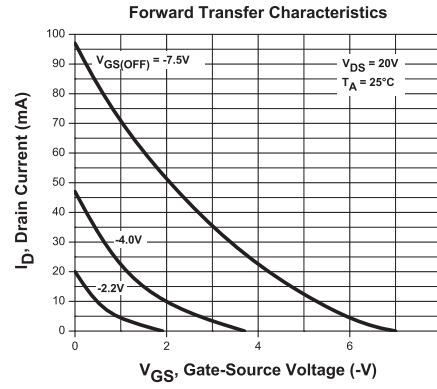
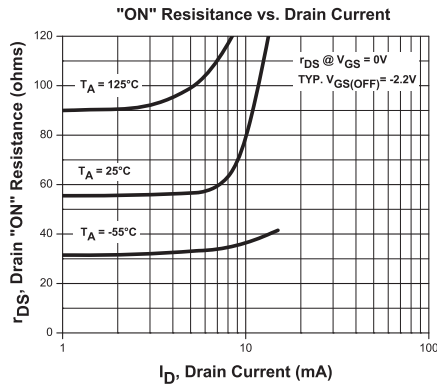
CP216-2N4856

Typical Electrical Characteristics



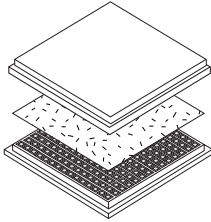
CP216-2N4856

Typical Electrical Characteristics



R0 (2-October 2019)

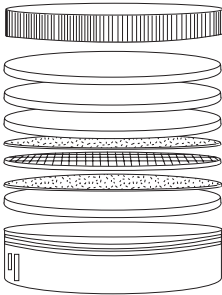
BARE DIE PACKING OPTIONS



BARE DIE IN TRAY (WAFFLE) PACK

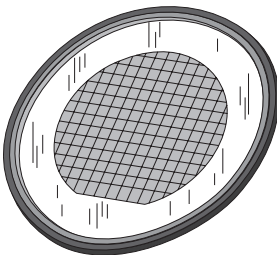
CT: Singulated die in tray (waffle) pack.
(example: CP211-PART NUMBER-CT)

CM: Singulated die in tray (waffle) pack 100% visually inspected as per MIL-STD-750, (method 2072 transistors, method 2073 diodes).
(example: CP211-PART NUMBER-CM)



UNSAWN WAFER

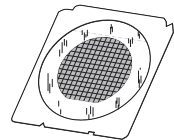
WN: Full wafer, unsawn, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WN)



SAWN WAFER ON PLASTIC RING

WR: Full wafer, sawn and mounted on plastic ring,
100% tested with reject die inked.
(example: CP211-PART NUMBER-WR)

Please note: Sawn Wafer on Metal Frame (WS) is possible as a special order. Please contact your Central Sales Representative at 631-435-1110.



Visit the Central website for a complete listing of specifications:
www.centrasemi.com/bdspecs

OUTSTANDING SUPPORT AND SUPERIOR SERVICES



PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix "TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix "PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

CONTACT US

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