DMMT3906W

MATCHED PNP SMALL SIGNAL SURFACE MOUNT TRANSISTOR

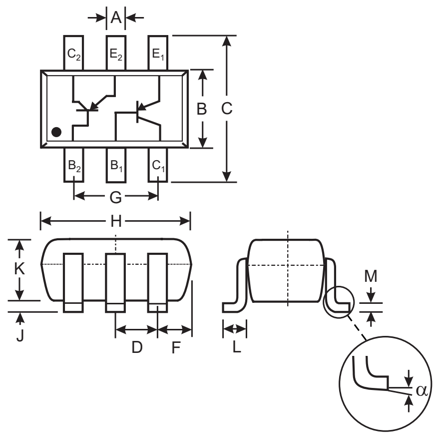
NEW PRODUCT

Features

- Epitaxial Planar Die Construction
- Intrinsically Matched PNP Pair (Note 1)
- Small Surface Mount Package
- 2% Matched Tolerance, h_{FE}, $V_{CE(SAT)}$, $V_{BE(SAT)}$
- 1% Matched Tolerance Available (Note 2)
- **Lead Free/RoHS Compliant (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: SOT-363
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020C
- Terminals: Solderable per MIL-STD-202, Method 208
- Lead Free Plating (Matte Tin Finish annealed over Alloy 42 leadframe).
- Terminal Connections: See Diagram
- Marking (See Below): K4B
- Ordering & Date Code Information: See Below
- Weight: 0.015 grams (approximate)



SOT-363		
Dim	**Min**	**Max**
A	0.10	0.30
B	1.15	1.35
C	2.00	2.20
D	0.65 Nominal	
F	0.30	0.40
H	1.80	2.20
J	—	0.10
K	0.90	1.00
L	0.25	0.40
M	0.10	0.25
α	8°	
All Dimensions in mm		

Maximum Ratings

@ T_A = 25°C unless otherwise specified

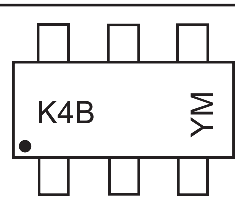
Characteristic	Symbol	DMMT3906W	Unit
Collector-Base Voltage	V_{CBO}	-40	V
Collector-Emitter Voltage	V_{CEO}	-40	V
Emitter-Base Voltage	V_{EBO}	-5.0	V
Collector Current - Continuous	I_C	-200	mA
Power Dissipation (Note 4)	P_d	200	mW
Thermal Resistance, Junction to Ambient (Note 4)	$R_{\theta JA}$	625	°C/W
Operating and Storage and Temperature Range	T_j, T_{STG}	-55 to +150	°C

Ordering Information (Note 5)

Device	Packaging	Shipping
DMMT3906W-7-F	SOT-363	3000/Tape & Reel

Notes:
1. Built with adjacent die from a single wafer.
2. Contact the Diodes, Inc. Sales department.
3. No purposefully added lead.
4. Device mounted on FR5 PCB: 1.0 x 0.75 x 0.62 in.; pad layout as shown on suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.
5. For Packaging Details, go to our website at http://www.diodes.com/datasheets/ap02007.pdf.

Marking Information



K4B = Product Type Marking Code
YM = Date Code Marking
Y = Year ex: N = 2002
M = Month ex: 9 = September

Date Code Key

Year	2002	2003	2004	2005	2006	2007	2008
Code	N	P	R	S	T	U	V

Month	Jan	Feb	March	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

NEW PRODUCT

Electrical Characteristics @ T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)					
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	-40	—	V	I_C = -10μA, I_E = 0
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	-40	—	V	I_C = -1.0mA, I_B = 0
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	-5.0	—	V	I_E = -10μA, I_C = 0
Collector Cutoff Current	I_{CEX}	—	-50	nA	V_{CE} = -30V, $V_{EB(OFF)}$ = -3.0V
Base Cutoff Current	I_{BL}	—	-50	nA	V_{CE} = -30V, $V_{EB(OFF)}$ = -3.0V
ON CHARACTERISTICS (Note 6)					
DC Current Gain (Note 7)	h_{FE}	60 80 100 60 30	— — 300 — —	—	I_C = -100μA, V_{CE} = -1.0V I_C = -1.0mA, V_{CE} = -1.0V I_C = -10mA, V_{CE} = -1.0V I_C = -50mA, V_{CE} = -1.0V I_C = -100mA, V_{CE} = -1.0V
Collector-Emitter Saturation Voltage (Note 7)	$V_{CE(SAT)}$	—	-0.25 -0.40	V	I_C = -10mA, I_B = -1.0mA I_C = -50mA, I_B = -5.0mA
Base-Emitter Saturation Voltage (Note 7)	$V_{BE(SAT)}$	-0.65 —	-0.85 -0.95	V	I_C = -10mA, I_B = -1.0mA I_C = -50mA, I_B = -5.0mA
Base-Emitter Voltage Matching	ΔV_{BE}	—	-1	mV	V_{CE} = -5V, I_C = -2mA
SMALL SIGNAL CHARACTERISTICS					
Output Capacitance	C_{obo}	—	4.5	pF	V_{CB} = -5.0V, f = 1.0MHz, I_E = 0
Input Capacitance	C_{ibo}	—	10	pF	V_{EB} = -0.5V, f = 1.0MHz, I_C = 0
Input Impedance	h_{ie}	2.0	12	kΩ	V_{CE} = 10V, I_C = 1.0mA, f = 1.0kHz
Voltage Feedback Ratio	h_{re}	0.1	10	$x\ 10^{-4}$	
Small Signal Current Gain	h_{fe}	100	400	—	
Output Admittance	h_{oe}	3.0	60	μS	
Current Gain-Bandwidth Product	f_T	250	—	MHz	V_{CE} = -20V, I_C = -10mA, f = 100MHz
Noise Figure	NF	—	4.0	dB	V_{CE} = -5.0V, I_C = -100μA, R_S = 1.0kΩ, f = 1.0kHz
SWITCHING CHARACTERISTICS					
Delay Time	t_d	—	35	ns	V_{CC} = -3.0V, I_C = -10mA, $V_{BE(off)}$ = 0.5V, I_{B1} = -1.0mA
Rise Time	t_r	—	35	ns	
Storage Time	t_s	—	225	ns	V_{CC} = -3.0V, I_C = -10mA, I_{B1} = I_{B2} = -1.0mA
Fall Time	t_f	—	75	ns	

Notes: 6. Short duration test pulse used to minimize self-heating effect.
7. The DC current gain, h_{FE}, (matched at I_C = -10mA and V_{CE} = -1.0V) Collector-Emitter Saturation Voltage, $V_{CE\ (sat)}$, and Base-Emitter Saturation Voltage, $V_{BE(sat)}$ are matched with typical matched tolerances of 1% and maximum of 2%.

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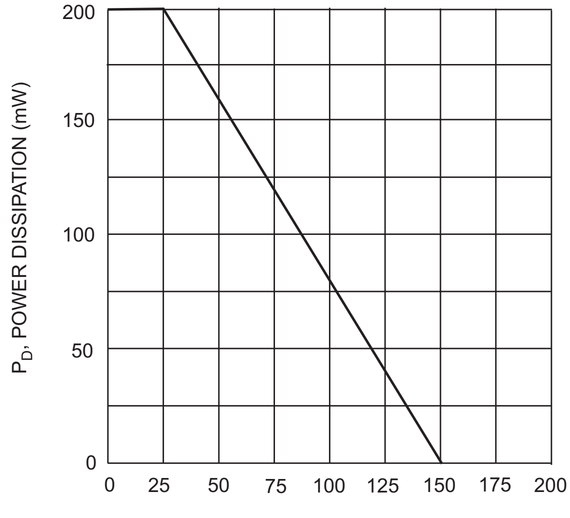

Fig. 1, Max Power Dissipation vs Ambient Temperature

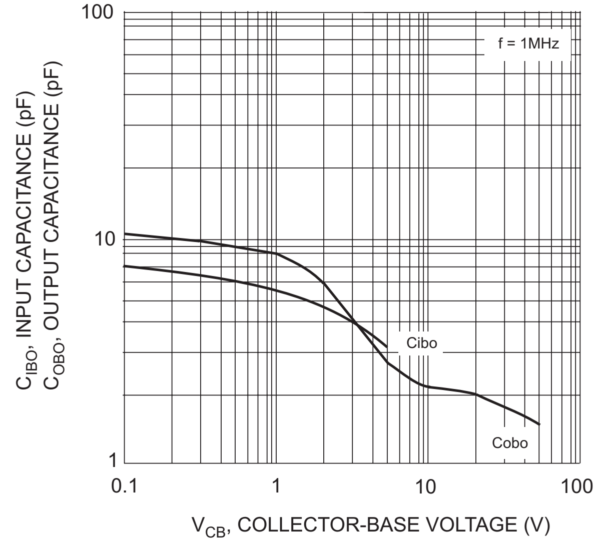

Fig. 2, Input and Output Capacitance vs. Collector-Base Voltage

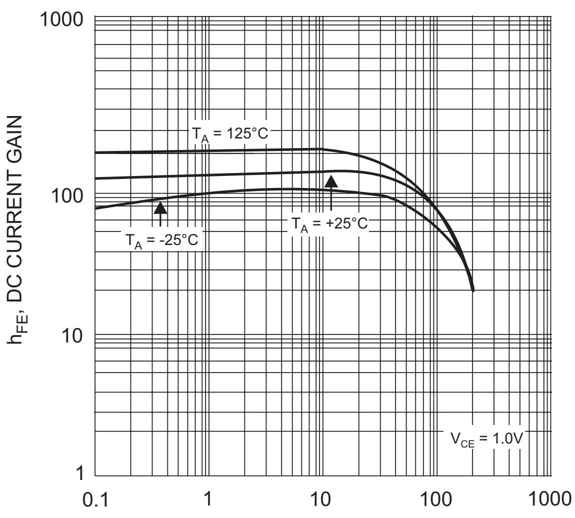

Fig. 3, Typical DC Current Gain vs Collector Current

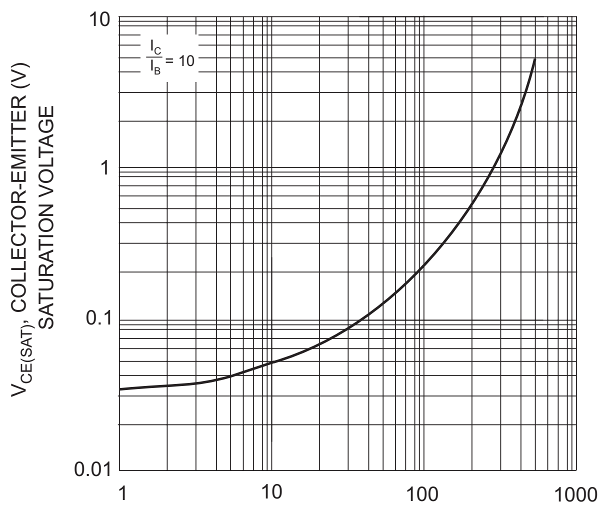

Fig. 4, Typical Collector-Emitter Saturation Voltage vs. Collector Current

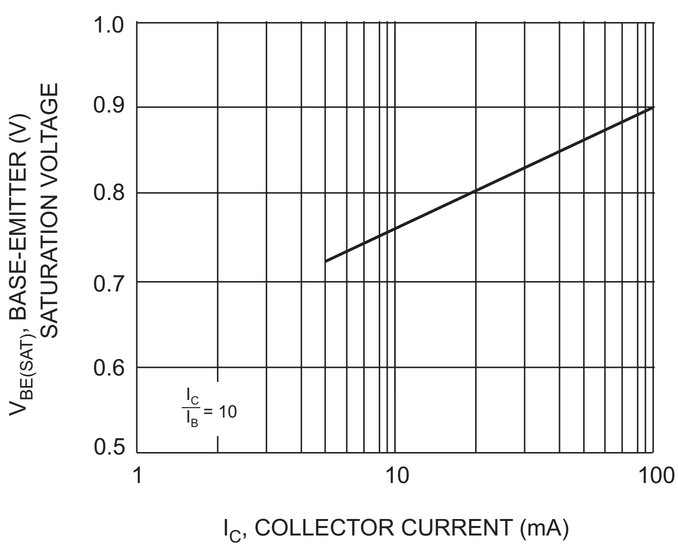

Fig. 5, Typical Base-Emitter Saturation Voltage vs. Collector Current

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