FAIRCHILD SEMICONDUCTOR®

September 2008

SG6521 — PC Power Supply Supervisors

Features

- Two 12V Sense Input Pins: VS12 and VS12B
- Over-Voltage Protection (OVP) for 3.3V, 5V, and two 12V
- Over-Current Protection (OCP) for 3.3V, 5V, and two 12V
- Under-Voltage Protection (UVP) for 3.3V, 5V, and two 12V
- Open-Drain Output for PGO and FPO Pins
- 300ms Power-Good Delay
- 2.8ms PSON Control to FPO Turn-off Delay
- 48ms PSON Control Delay
- No Lock-up During the Fast AC Power On/Off
- Wide Supply Voltage Range: 4V to 15V
- Over-Temperature Protection (OTP)
- Additional Protection Input (Pext)

Applications

- Switch-Mode Power Supplies with Active PFC
- Servo System Power Supplies
- PC-ATX Power Supplies

Description

The SG6521 is designed to provide the supply voltage, current supervisor, remote on/off (PSON), power good (PGO) indicator, and fault protection (FPO) functions for switching power systems.

For supervisory functions, it provides the over-voltage protection (OVP) for 3.3V, 5V, and two 12V; over-current protection (OCP) for 3.3V, 5V, and two 12V; under-voltage protection (UVP) for 3.3V, 5V, and two 12V. When 3.3V, 5V, or 12V voltage decreases to 2.3V, 3.5V, and 9V, respectively, the under-voltage protection function is enabled. FPO is set HIGH to turn off the PWM controller IC. The voltage difference across external current shunt is used for OCP functions. An external resistor can be used to adjust protection threshold. An additional protection input pin provides the flexibility for designing protection circuits.

The power supply is turned on after a 48ms delay when PSON signal is set from HIGH to LOW. To turn off the power supply, the PSON signal is set from LOW to HIGH with a delay of 48ms. The PGI circuitry provides a power-down warning signal for PGO. When PGI input is lower than the internal 1.25V reference voltage, PGO signal is pulled LOW.

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method
SG6521DZ	-40°C to +85°C	RoHS	16-pin Dual In-Line Package (DIP)	Rail
SG6521SZ	-40°C to +85°C	RoHS	16-pin Small Outline Package (SOP)	Tape & Reel

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Application Diagram

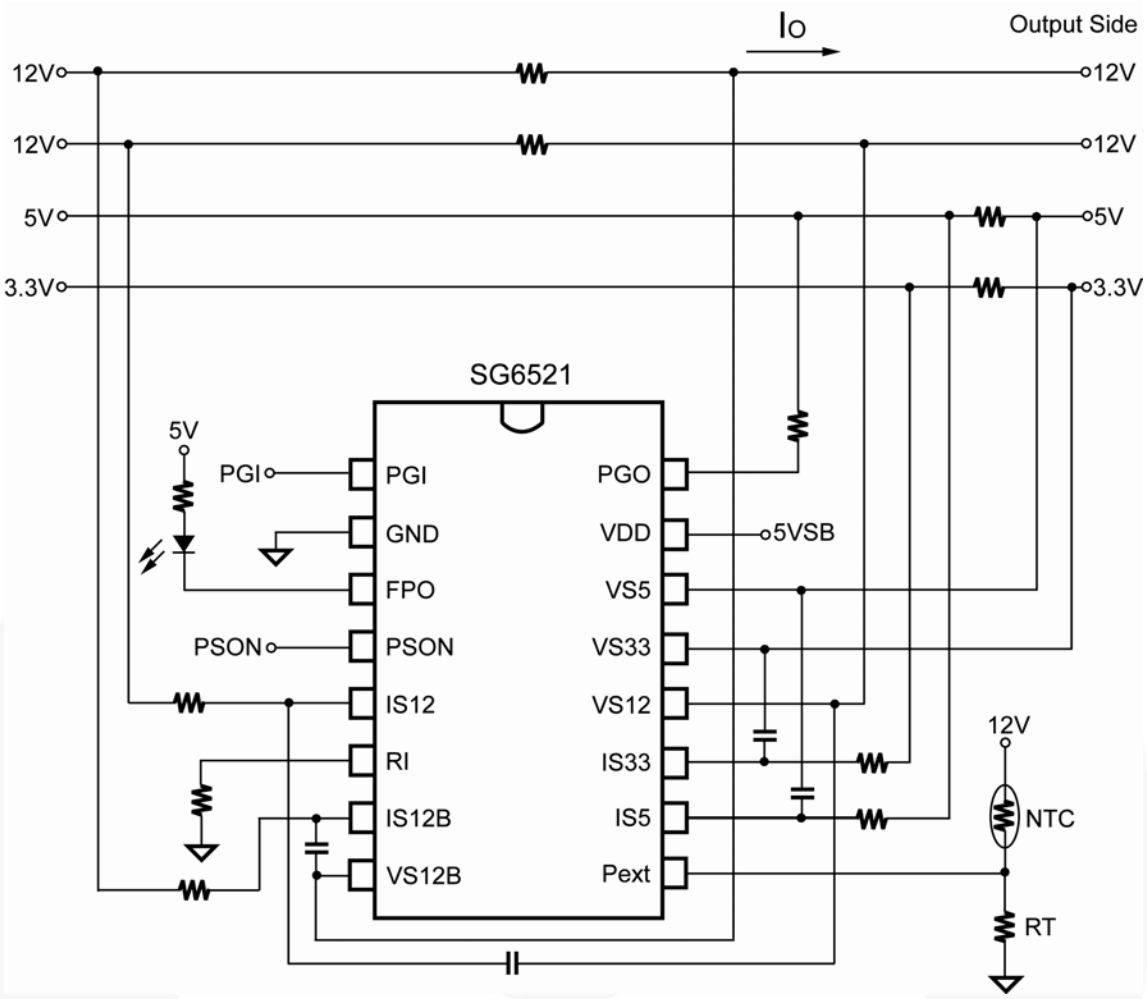

Figure 1. Typical Application

Block Diagram

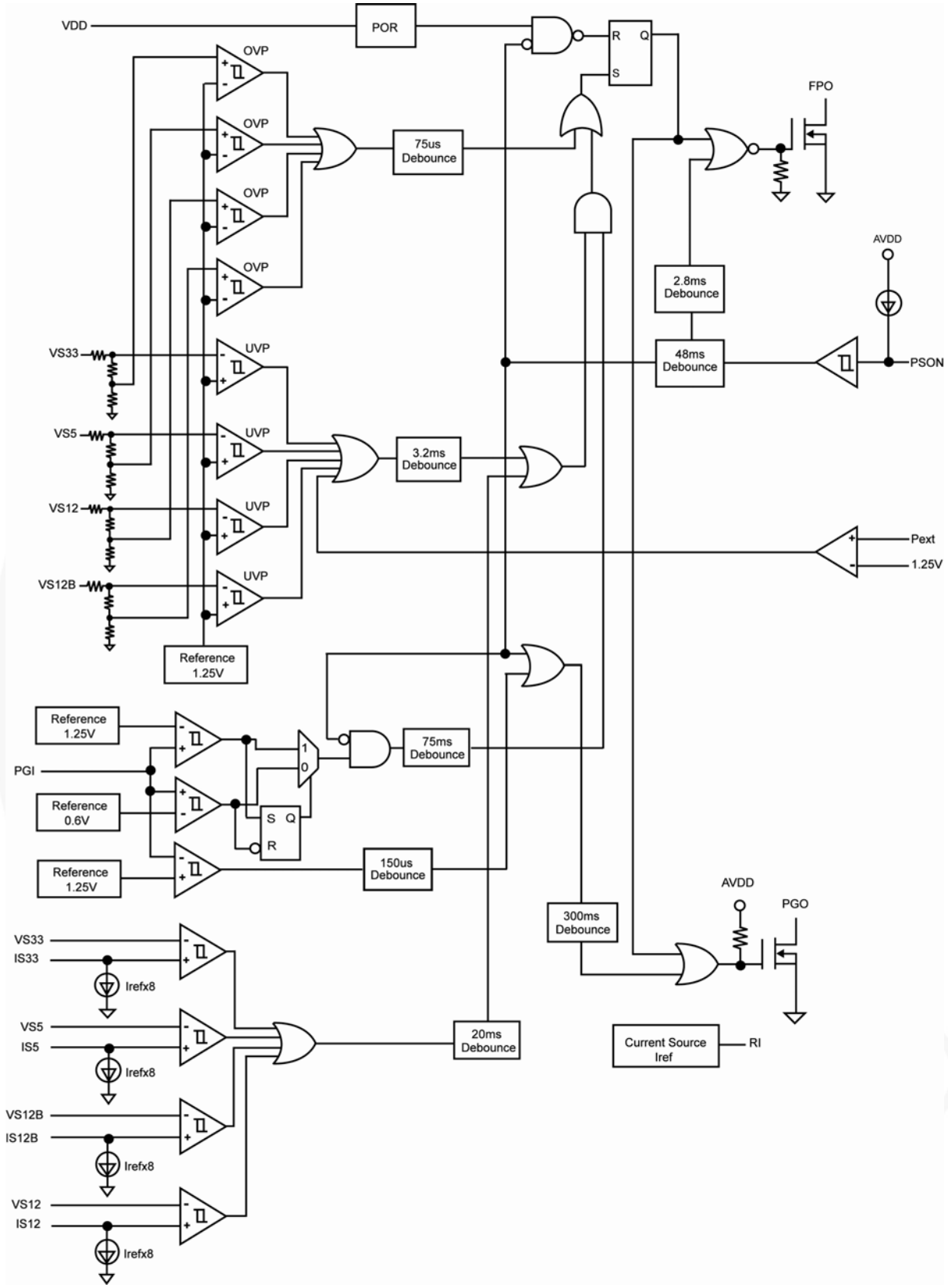

Figure 2. Function Block Diagram

Pin Configuration

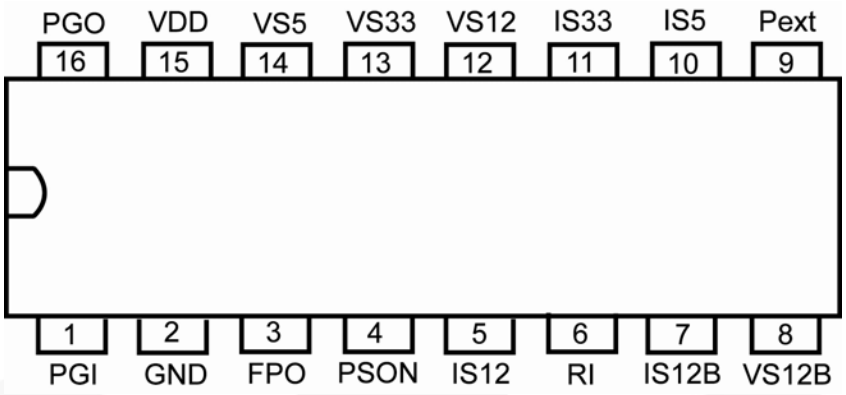

Figure 3. Pin Configuration(Top View)

Pin Definitions

Pin #	Name	Description
1	PGI	**Power Good Input**. For ATX SMPS, it detects AC line voltage through the main transformer.
2	GND	**Ground**.
3	FPO	**Fault Protection Output**. Output signal to control the primary PWM IC through an opto-coupler. When FPO is low, the PWM IC is enabled.
4	PSON	**Remote On/Off Logic Input from CPU or Main Board**. The power supply is turned on/off after a 48ms delay.
5	IS12	**12V Over-Current Protection Sense Input**. For typical applications, this pin is connected to the positive end of a current shunt through one resistor. When the voltage on IS12 is higher than that of VS12 by 5mV, OCP is enabled.
6	RI	**Reference Setting**. One external resistor RI connected between the RI and GND pins determines a reference current, I_{REF} = 1.25/R_I, for OCP programming.
7	IS12B	**12V Over-Current Protection Sense Input**. For typical application, this pin is connected to the positive end of a current shunt through one resistor. When the voltage on IS12 is higher than that of VS12 by 5mV, OCP is enabled.
8	VS12B	**Second 12V Over/Under-Voltage Control Sense Input**.
9	Pext	**External Protection Detects Input**.
10	IS5	**5V Over-Current Protection Sense Input**.
11	IS33	**3.3V Over-Current Protection Sense Input**.
12	VS12	**12V Over/Under-Voltage Control Sense Input**.
13	VS33	**3.3V Over/Under-Voltage Control Sense Input**.
14	VS5	**5V Over/Under-Voltage Control Sense Input**.
15	VDD	**Supply Voltage**. 4.2V ~ 15V. For ATX SMPS, it is connected to 5V-standby and 12V through diodes, respectively.
16	PGO	**Power-Good Logic Output**. 0 or 1 (open-drain). Power good=1 means that the power supply is good for operation. The power good delay is 300ms.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter			Min.	Max.	Unit
V_{DD}	DC Supply Voltage				16	V
V_{IN}	Input Voltage	PSON, PGI, VS5, IS5, VS33, IS33, Pext		-0.3	7.0	V
		VS12, VS12B, IS12, IS12B		-0.3	15.0	V
V_{OUT}	Output Voltage	FPO, PGO		-0.3	8.0	V
T_J	Operating Junction Temperature			-40	+125	°C
T_{STG}	Storage Temperature Range			-55	+150	°C
T_L	Lead Temperature (Soldering)				+260	°C
ESD	Electrostatic Discharge Capability		Human Body Model: JESD22-A114		3.0	KV
			Machine Model: JESD22-A115		200	V

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Ambient Temperature	-40		+85	°C

Electrical Characteristics

V_{DD} = 5V, and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD} Section						
V_{DD}	DC Supply Voltage		4.2		15.0	V
I_{DD1}	Supply Current	PSON = LOW		1.7	2.6	mA
I_{DD2}	Supply Current	PSON = HIGH		1.0	1.5	mA
t_R	Supply Voltage Rising Time		1			ms
V_{ST}	V_{DD} Start Threshold Voltage				4.2	V
Over-Voltage (OVP) and Over-Current (OCP) Protections						
V_{OVP}	Over-Voltage Protection	VS33	3.7	3.9	4.1	V
		VS5	5.7	6.1	6.5	
		VS12, VS12B	13.2	13.8	14.4	
I_{REF}	Ratio of Current Sense Sink Current to Current Sense Setting Pin (RI) Source Current	R_I = 18.5kΩ ~75kΩ	7.6	8.0	8.4	
V_{OFFSET}	OCP Comparator Input Offset Voltage		-3		3	mV
$I_{LKG-FPO}$	Leakage Current (FPO)	FPO = 5V			5	µA
V_{OL-FPO}	Low-Level Output Voltage (FPO)	I_{SINK} 20mA			0.4	V
t_{OVP}	OVP Delay Time		33	75	110	µs
t_{OCP}	OCP Delay Time		12.5	20.0	27.5	ms
V_{RI}	RI Pin Voltage		0.98•Typ.	1.25	1.01•Typ.	V
I_{RI}	Output Current RI		12.5		62.5	µA
t_{ST-OCP}	Startup OCP / UVP Protection Time	0.6V < PGI < 1.25V; FPO = Low	49	75	114	ms
Under-Voltage Protection and PGI, PGO						
V_{PGI_1}	Input Threshold Voltage	PGI 1	0.98•Typ.	1.25	1.02•Typ.	V
V_{PGI_2}	Input Threshold Voltage	PGI 2	0.96•Typ.	0.60	1.03•Typ.	V
V_{UVP}	Under-Voltage Protection	VS33	2.1	2.3	2.5	V
		VS5	3.3	3.5	3.7	
		VS12, VS12B	8.5	9.0	9.5	
t_{OND}	Under-Voltage Turn-on Delay	PGI>0.6V	49	75	114	ms
t_{UVP}	UVP Delay	PGI>1.25V	2.4	3.2	4.0	ms
$I_{LKG-PGO}$	Leakage Current (PGO)	PGO = 5V			5	µA
V_{OL-PGO}	Low-Level Output Voltage (PGO)	V_{DD} = 12V; I_{SINK} 10mA			0.4	V
t_{PG}	Timing PG Delay		200	300	450	ms
t_{ND1}	Noise Deglitch Time		90	150	210	µs
PSON Control						
I_{PSON}	Input Pull-up Current	PSON = 0V		120		µA
V_{IH}	High-Level Input Voltage		2			V
V_{IL}	Low-Level Input Voltage				0.8	V
t_{PSON}	Timing PSON to On/Off	PSON LOW to FPO LOW	34	48	67	ms
		PSON HIGH to PGO LOW	34	48	67	
t_{PSOFF}	Timing PGO LOW to FPO HIGH		1.6	2.8	4.5	ms
External Protection Detect Section						
V_{TH}	Pext Threshold		1.20	1.25	1.30	V
t_{Pext}	Pext Delay Time		2.4	3.2	4.0	ms

Functional Description

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The SG6521 provides over-current protection for the 3.3V, 5V, and two 12V rails. Whenever an OCP condition occurs at any of the voltage rails, PGO is LOW and FPO is open. The internal OCP comparators have a very small offset voltage (±3mV). The sink currents of IS33, IS5, and IS12 are eight times the current at the RI pin. The current at the RI pin is V_{RI}/R_I.

Here is an example demonstrating how to set the over current protection. If $I_1 \times R_1 > I_{RI} \times R2$, OCP is active. If R_1=5mΩ, R_I=30KΩ, and the OCP active level is 35A, then the R_2 resistor is:

$$R_2 = \frac{I_1 \times R_1}{I_{RI} \times 8} = 525\Omega \quad (1)$$

where C is bypass noise, suggested value is between 1μF ~ 2.2μF

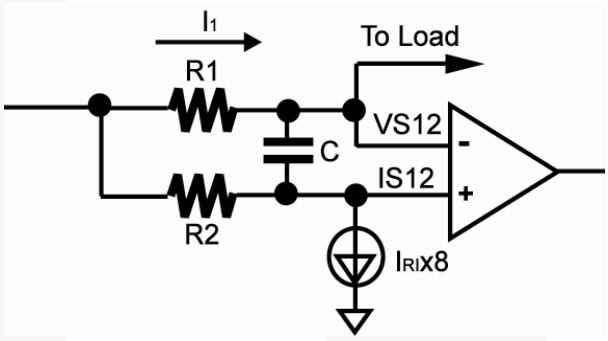


Figure 4. OCP Setup

Timing Chart

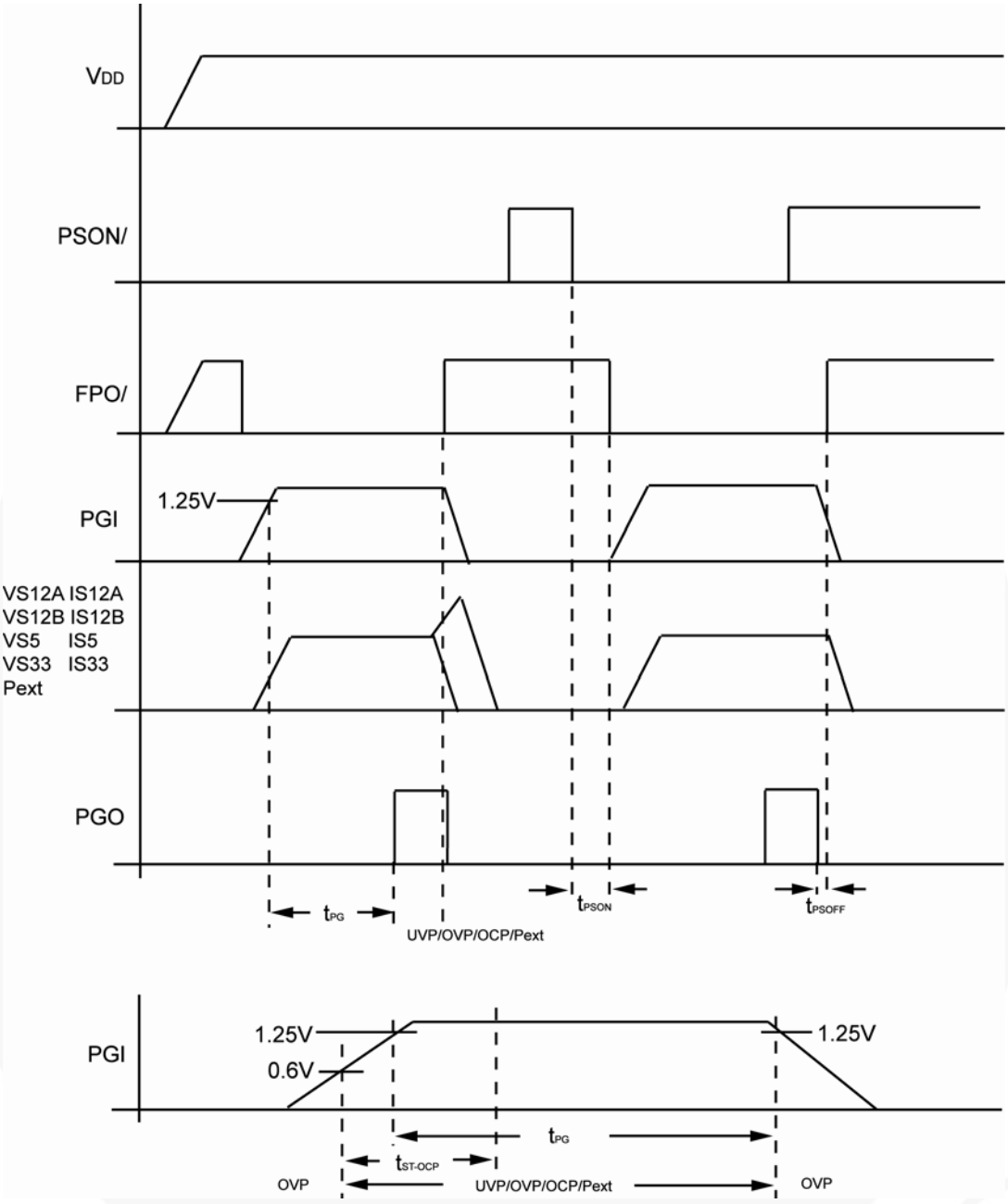


Figure 5. Timing Diagram

Typical Performance Characteristics

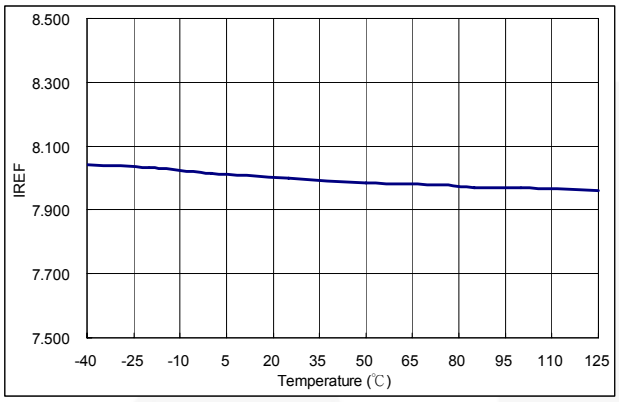


Figure 6. I_{REF} vs. T_A

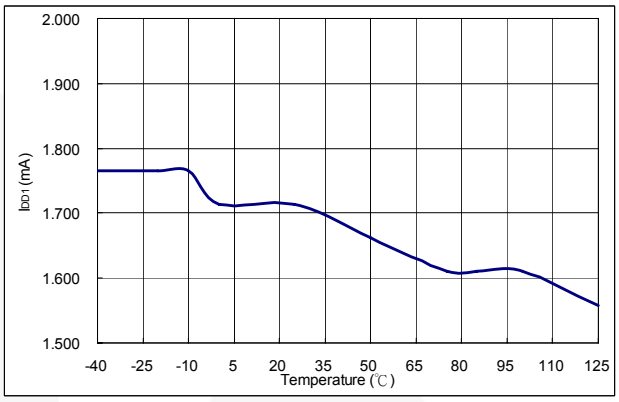


Figure 7. I_{DD1} vs. T_A

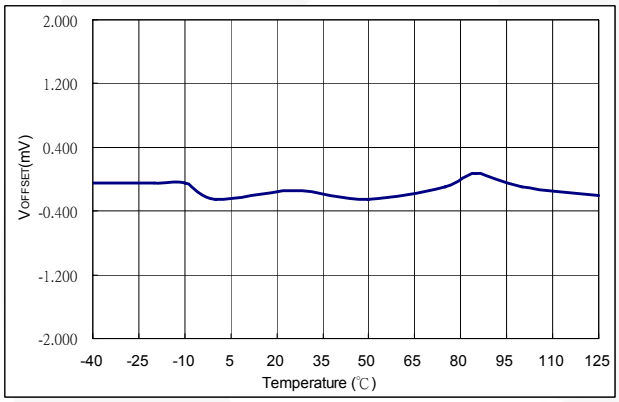


Figure 8. V_{OFFSET} vs. T_A

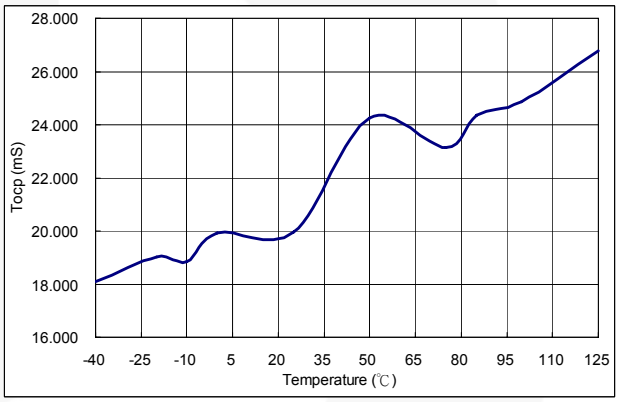


Figure 9. T_{OCP} vs. T_A

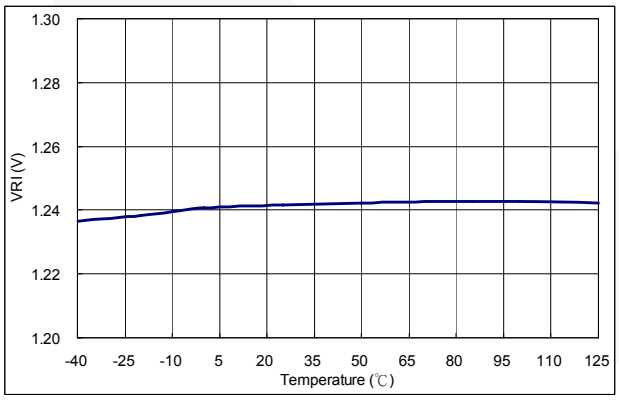


Figure 10. V_{RI} vs. T_A

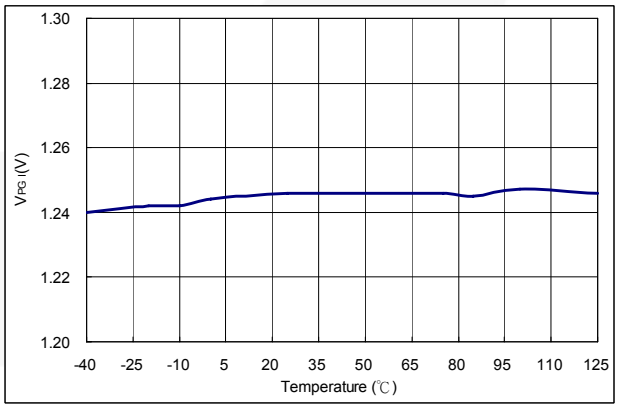
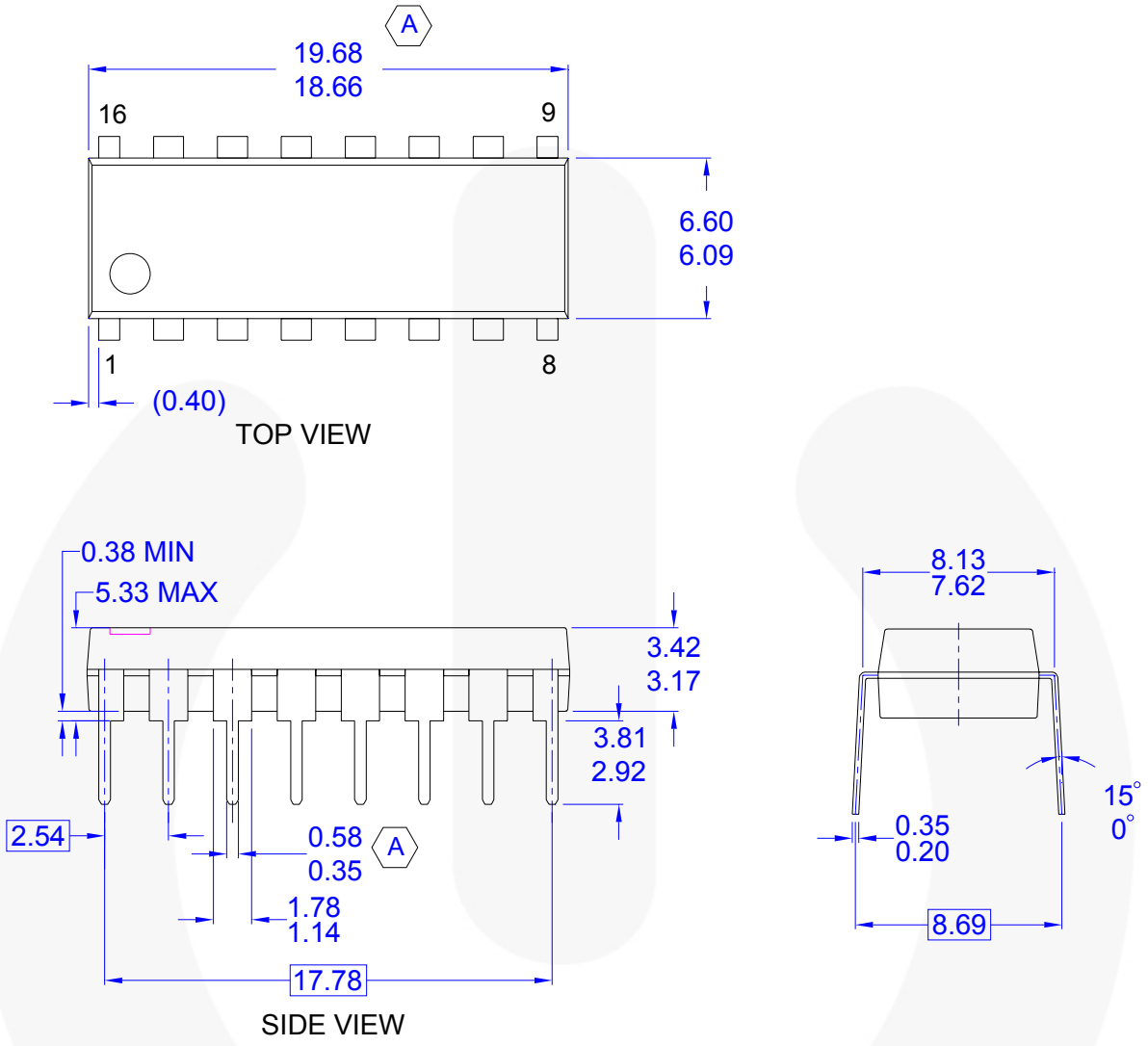


Figure 11. V_{PGI} vs. T_A

Physical Dimensions



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D) CONFORMS TO ASME Y14.5M-1994

E) DRAWING FILE NAME: N16EREV1

Figure 12. 16-Lead, Dual Inline Package (DIP)

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Physical Dimensions (Continued)

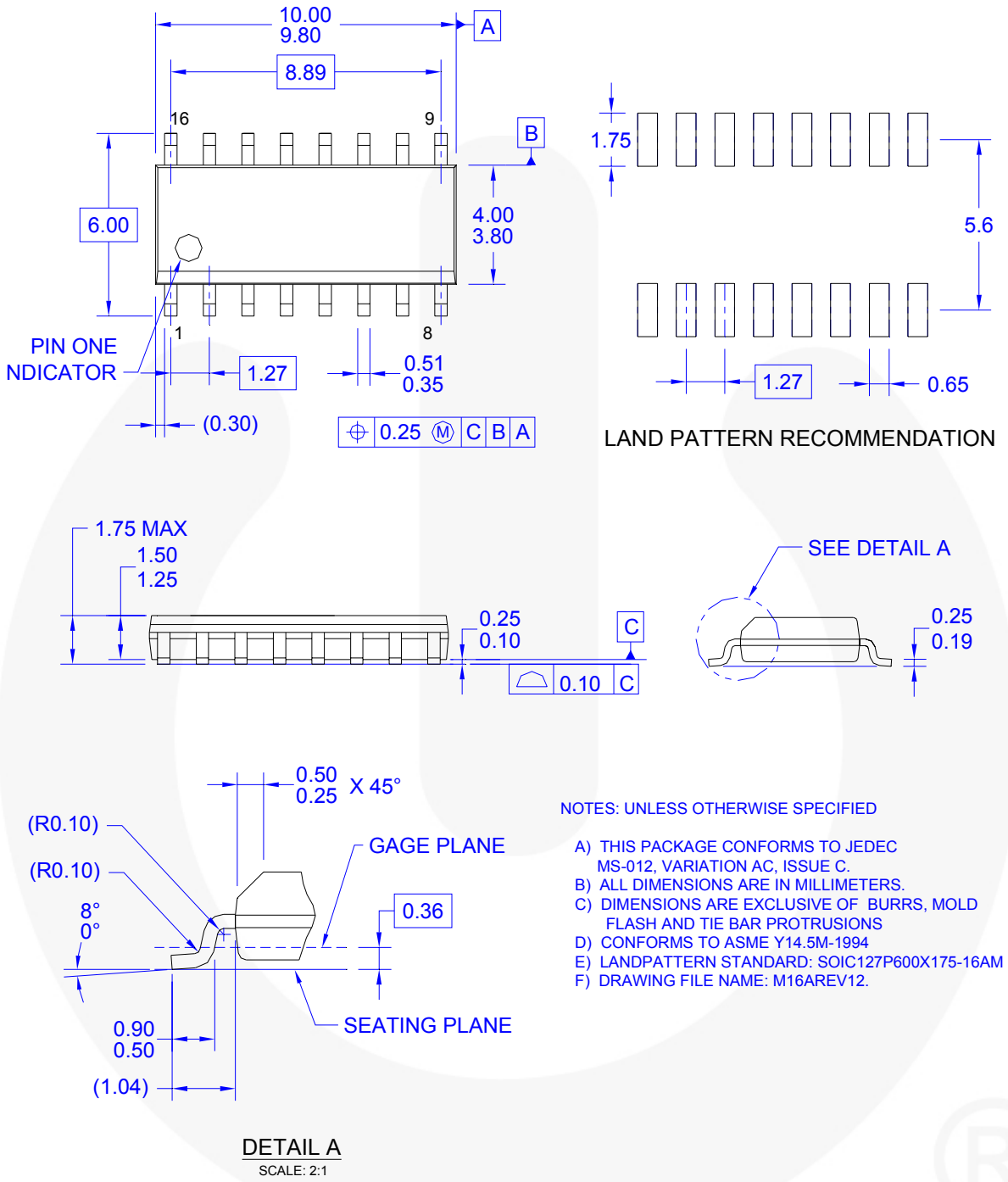

Figure 13. 16-Lead, Small Outline Integrated Circuit (SOIC)

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