Gate Driver for SiC SJT with Output and Signal Isolation

$V_{ISOLATION}$	=	3000 V
P_{DRIVE}	=	5 W
f_{max}	=	350 kHz

Features

- Requires single 12 V voltage supply
- Pin Out compatible with MOSFET driver boards
- Multiple Internal level topology for low drive losses
- High-side drive capable with 3000 V isolation
- 5000 V Signal Isolation (up to 10 s)
- Capable of high gate currents with 3 W maximum power
- RoHS Compliant

Product Image

Section I: Introduction

The GA03IDDJT30-FR4 provides an optimized gate drive solution for SiC Junction Transistors (SJT). The board utilizes DC/DC converters and FOD3182 opto-isolators making it capable of driving high and low-side devices in a half-bridge configuration as well as IXDN609 gate driver ICs providing fast switching and customizable continuous gate currents necessary for SJT devices. Its footprint and 12 V supply voltage make it a plug-in replacement for existing SiC MOSFET gate drive solutions.

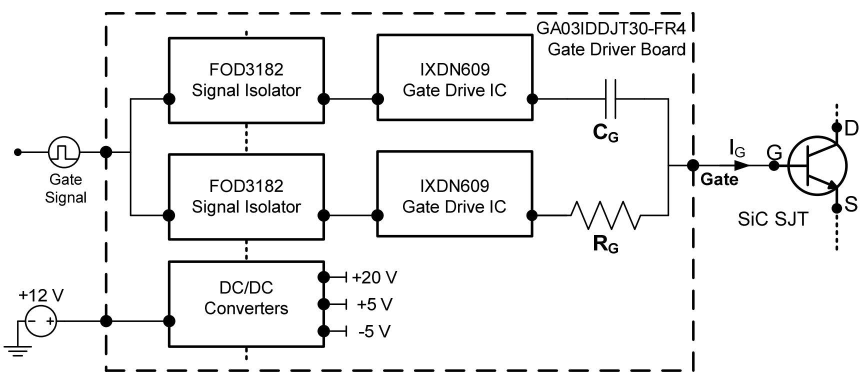

Figure 1: Simplified GA03IDDJT30-FR4 Gate Drive Board Block Diagram

Section II: Compatibility with SiC SJTs

The GA03IDDJT30-FR4 has an installed R_G of 3.75 Ω on-board which may need to be modified by the user for safe operation of certain SJT parts. Please see the table below and Section VII for more information.

Table 1: GA03IDDJT30-FR4 – SiC SJT Compatibility Information Table

SJT Part Number	Compatible	Requires R_G Modification
GA03JT12-247	Yes	Not Required
GA05JT12-247/263		Not Required
GA06JT12-247		Not Required
GA10JT12-247/263		**Recommended (see Section VII)**
GA20JT12-247/263		**Required (see Section VII)**
GA50JT12-247		**Required (see Section VII)**
GA04JT17-247		Not Required
GA16JT17-247		**Required (see Section VII)**
GA50JT17-247		**Required (see Section VII)**

Section III: Operational Characteristics

Parameter	Symbol	Conditions	Value Min.	Value Typical	Value Max.	Unit	Notes
Input Supply Voltage	V_{CC}	V_{CC} High, V_{CC} Low	10.8	12	13.2	V	
Input Signal Voltage, Off	$V_{sig,\ OFF}$		-5	0	0.8	V	
Input Signal Voltage, On	$V_{sig,\ ON}$		3.2	5.0	6.4	V	
Input Signal Current, On	$I_{sig,\ ON}$		20	36	50	mA	
Propagation Delay, Signal Turn On	$t_{d,ON}$			160	270	ns	
Propagation Delay, Signal Turn Off	$t_{d,OFF}$			187	270	ns	
Output Gate Current, Peak	$I_{G,ON}$			4	9.0	A	
Output Gate Current, Continuous	$I_{G,steady}$	D = 0.3, f < 350 kHz		0.35	1.8	A	
Output Gate Voltage Rise Time	t_r	C_{load} = 10 nF		21	35	ns	
Output Gate Voltage Fall Time	t_f	C_{load} = 10 nF		14	25	ns	
Operating Frequency	f_{sw}	Dependant on device driven and C_G			350	kHz	
Power Dissipation	P_{tot}	3.0 W (V_{GL}) + 2.0 W (V_{GH} + V_{EE})			5.0	W	
SJT Drain – Source Voltage	V_{DS}	On driven power transistor			1700	V	
Isolation Voltage, Signal	$V_{ISO\text{-}SIG}$				±5000	V	
Isolation Voltage, Voltage Supply	$V_{ISO\text{-}DC}$				±3000	V	
Storage Temperature	T		-55		100	°C	
Product Weight				19		g	

Section IV: Pin Out Description

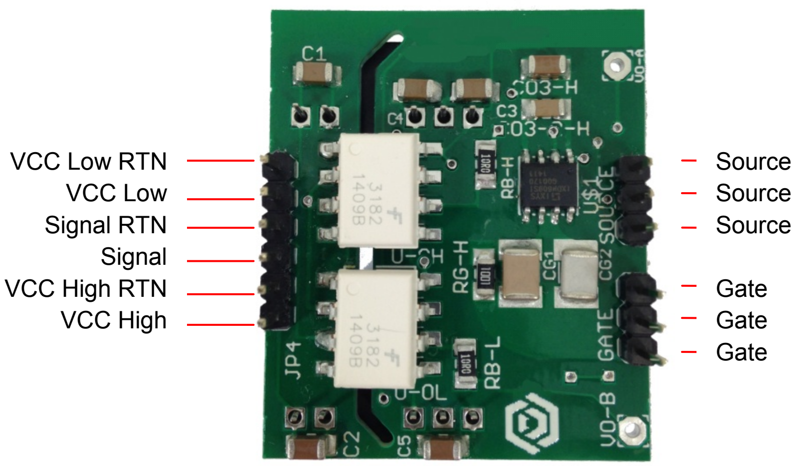

Figure 2: Gate Drive Board Top View

Table 2: GA03IDDJT30-FR4 Pin Out Connections

Header	Pin Label	Suggested Connection
JP1	VCC High	+ 12 V, > 6 W Supply
JP1	VCC High RTN	Analog Ground
JP1	Signal	Gate Drive Control Signal
JP1	Signal RTN	Analog Ground
JP1	VCC Low	+ 12 V, > 6 W Supply
JP1	VCC Low RTN	Analog Ground
Gate	Gate	SJT Gate Pin
Gate	Gate	SJT Gate Pin
Gate	Gate	SJT Gate Pin
Source	Source	SJT Source Pin
Source	Source	SJT Source Pin
Source	Source	SJT Source Pin

Section V: SJT Gate Driving Theory of Operation

The SJT transistor is a current controlled transistor which requires a positive gate current for turn-on as well as to remain in on-state. An ideal gate current waveform for ultra-fast switching of the SJT, while maintaining low gate drive losses, is shown in Figure 3. This is similar to what the GA03IDDJT30-FR4 provides.

An SJT is rapidly switched on when the necessary gate charge, Q_G, for turn-on is supplied by a burst of high gate current, $I_{G,on}$, until the gate-source capacitance, C_{GS}, and gate-drain capacitance, C_{GD}, are fully charged.

$$Q_{on} = I_{G,on} * t_1$$

$$Q_{on} \geq Q_{gs} + Q_{gd}$$

The $I_{G,pon}$ pulse should ideally terminate, when the drain voltage falls to its on-state value, in order to avoid unnecessary drive losses during the steady on-state. In practice, the rise time of the $I_{G,on}$ pulse is affected by the parasitic inductances, L_{par} in the device package and drive circuit. A voltage developed across the parasitic inductance in the source path, L_s, can de-bias the gate-source junction, when high drain currents begin to flow through the device. The applied gate voltage should be maintained high enough, above the $V_{GS,ON}$ level to counter these effects.

After the SJT is turned on, I_G may be lowered to $I_{G,steady}$ for reducing unnecessary gate drive power losses. The minimum $I_{G,steady}$ is determined by noting the DC current gain, h_{FE}, of the device from its datasheet. The desired $I_{G,steady}$ is determined by the peak device junction temperature T_J during operation, drain current I_D, DC current gain h_{FE}, and a 50 % safety margin to ensure operating the device in the saturation region with low on-state voltage drop by the equation:

$$I_{G,steady} \approx \frac{I_D}{h_{FE}(T, I_D)} * 1.5$$

For SJT turn -off, a high negative peak current, $-I_{G,off}$ at the start of the turn-off transition rapidly sweeps out charge from the gate. While satisfactory turn off can be achieved with V_{GS} = 0 V, a negative gate voltage V_{GS} may be used in order to speed up the turn-off transition. The GA03IDDJT30-FR4 provides a negative bias of -5 V during off state.

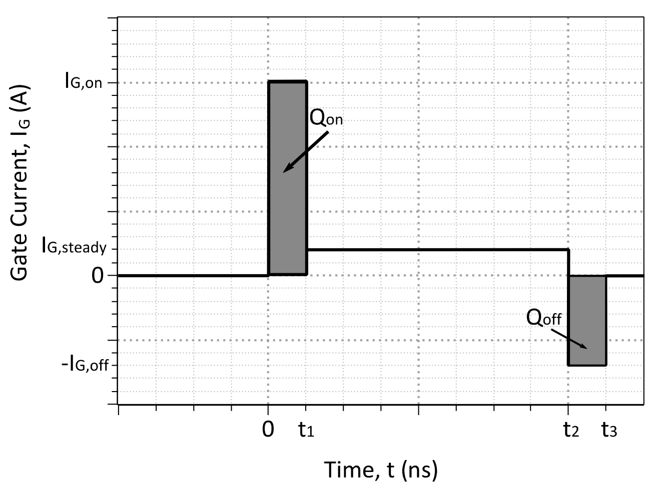

Figure 3: Idealized SJT Gate Current Waveform

Section VI: Gate Driver Implementation

The GA03IDDJT30-FR4 is a gate driver circuit which can be used to drive an SJT transistor by supplying the required gate drive current I_G in a low-power gate drive solution. This configuration features a gate capacitor C_G (CG1 and CG2 in parallel) which creates a brief current peak $I_{G,ON}$ during device turn-on and $I_{G,OFF}$ during turn-off for fast switching and a gate resistor R_G (RG1 and RG2 in parallel) to set the continuous gate current $I_{G,steady}$ required for an SJT to operate. This configuration is shown in the Figure 7 circuit diagram as well as in Figure 4 below with further details provided below. This section provides detail on selecting optimal C_G and R_G values based on the SJT, drain current, and temperature.

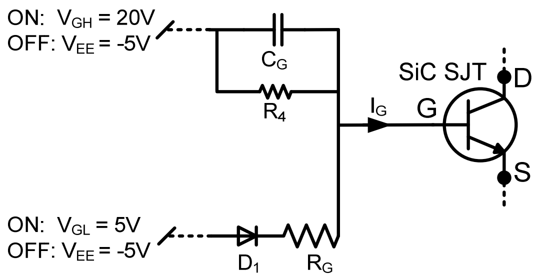

Figure 4: Primary gate drive circuit passive components with series gate resistance Schottky rectifier.

Table 3: Passive Output Component List

Symbol	Parameter	Values		
		Range	Default	Units
R_G	Gate Resistor, On Board	0 – 20	3.75	Ω
C_G	Gate Capacitor, On Board	5 – 20	10	nF
R_4	Charging Resistor	500 – 10k	1k	Ω
D_1	Schottky Diode of Gate Resistor	--	--	

A: Gate Resistor R_G Modification

The GA03IDDJT30-FR4 on board gate resistor R_G controls the continuous current $I_{G,steady}$ during steady on-state. The gate current is determined according to:

$$I_{G,steady} = \frac{V_{GL} - V_{GS,sat} - V_D}{R_G + 0.6\Omega}$$

$$I_{G,steady} = \frac{4.7\,V - V_{GS,sat}}{R_G + 0.6\Omega}$$

Where V_{GL} is the internal, low-level drive voltage (5 V), $V_{GS,sat}$ is the driven SJT saturated gate-source voltage obtained from the individual device datasheets, V_D is the Schottky diode voltage drop (approximately 0.3 V), and 0.6 Ω is added from internal GA03IDDJT30-FR4 drive components.

It is necessary for the user to reduce R_G from its pre-install value of 3.75 Ω for several SiC SJTs for safe operation with the GA03IDDJT30-FR4 under high drain current conditions. The location of RG on the circuit board is shown in Figure 5. The maximum allowable value of R_G for each device across all rated drain currents can be found in the Gate Drive section of each individual device datasheets. R_G may also be calculated from the following equation, where h_{FE} is the SJT DC current gain and $V_{GS,sat}$ is the gate-source saturation voltage. Both of these values may be taken from individual device datasheets.

$$R_{G,max} = \frac{\left(4.7V - V_{GS,sat}\right) * h_{FE}(T, I_D)}{I_D * 1.5} - 0.6\Omega$$

For some devices and drain currents it may be desired for the user to install a very low value of R_G or to short R_G (R_G = 0 Ω) to increase the gate current output. This is acceptable, but may limit the duty cycle D during operation. Please see section VII:B for more information.

B: Duty Cycle Limitation

The duty cycle *D* of the GA03IDDJT30-FR4 output may be limited by the 3 W power capability of the internal 5 V supply in some applications. If R_G remains un-changed by the user $I_{G,steady}$ will remain sufficiently low to allow 100 % duty cycle operation with an SJT. However, if R_G is shorted or reduced such that $R_G \leq 2.8$ Ω in order to drive higher current devices, the duty cycle will be limited by the following equation:

$$D \leq \frac{3W}{5V * I_{G,steady}} * 0.9$$

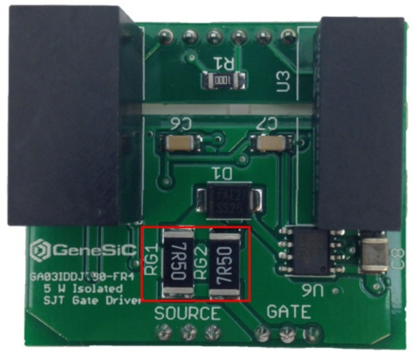

Figure 5: Location of R_G (RG1 and RG2 in parallel) on GA03IDDJT30-FR4 driver for substitution

C: Gate Capacitor C_G Modification

An external gate capacitor C_G connected directly to the device gate pin delivers the positive current peak $I_{G,ON}$ during device turn-on and the negative current peak $I_{G,OFF}$ during turn-off. A high value resistor R_4 in parallel with C_G sets the SJT gate pin to a defined potential ($-V_{EE}$) during steady off-state.

At device turn-on, C_G is pulled to the GA03IDDJT30-FR4 internal voltage level V_{GH} which produces a transient peak of gate voltage and current. This current peak rapidly charges the internal SJT C_{GS} and C_{GD} capacitances. A Schottky diode, D1, in series with R_G blocks any C_G induced current from draining out through R_G and ensures that all of the charge within C_G flows only into the device gate, allowing for an ultra-fast device turn-on. During steady on-state, a potential of $V_{GH} - V_{GS} = V_{GH} - 3$ V is across C_G. When the device is turned off, C_G is pulled to negative V_{EE} and V_{GS} is pulled to a transient peak of $V_{GS,turn\text{-}off} = V_{EE} - (V_{GH} - 3\text{ V})$, this induces the negative current peak $I_{G,off}$ out of the gate which discharges the SJT internal capacitances.

D: Voltage Supply Selection

The GA03IDDJT30-FR4 gate drive design features three internal supply voltages V_{GH}, V_{GL}, and V_{EE} (listed in Table 4) supplied through two DC/DC converters. During device turn-on, V_{GH} charges the capacitor C_G thereby delivering the narrow width, high current pulse $I_{G,ON}$ to the SJT gate and charges the SJT's internal terminal capacitances C_{GD} and C_{GS}. For a given level of parasitic inductance in the gate circuit and SJT package, the rise time of $I_{G,ON}$ is controlled by the value of V_{GH} and C_G. During the steady on-state, V_{GL} in combination with the internal and external gate resistances provides a continuous gate current for the SJT to remain on. The V_{EE} supply controls the gate negative voltage during turn-off and steady off-state for faster switching and to avoid spurious turn-on which may be caused by external circuit noise. The power rating of the provided voltage supplies are adequate to meet the gate drive power requirements as determined by

$$P_{min,VGH} = \frac{1}{2}\, C_G\, V_{GH}^2\, f_{sw}$$

$$P_{min,VEE} = \frac{1}{2}\, C_G\, V_{EE}^2\, f_{sw}$$

$$P_{min,VGL} = V_{GL} I_{G,steady}\, D$$

Table 4: GA03IDDJT30-FR4 Gate Drive Voltage Supply Component List

Symbol	Parameter	Values	
		Range	Default
V_{GH}	Supply Voltage, Gate Capacitor	15 – 20	+ 20.0
V_{GL}	Supply Voltage, Gate Resistor	5.0 – 7.0	+ 5.0
V_{EE}	Negative Supply Voltage	-10 – GND	- 5.0

E: Voltage Supply Isolation

The DC/DC supply voltage converters are suggested to provide isolation at a minimum of twice the working V_{DS} on the SJT transistor during off-state to provide adequate protection to circuitry external to the gate drive circuit. The installed DC/DC converters have an isolation of 3.0 kV and greater. Alternatively, DC/DC converter galvanic isolation may be bypassed and direct connection of variable voltage supplies may be done in a laboratory environment, this may be convenient during testing and prototyping but carries risk and is not suggested for extended usage.

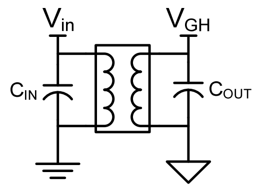

Figure 6: Typical DC/DC converter configuration

F: Signal Isolation

The gate supply signal is suggested to be isolated to twice the working V_{DS} on the SJT during off-state to provide adequate protection to circuitry external to the gate drive circuit. This may be done using opto or galvanic isolation techniques.

Section VII: Detailed Schematic and Bill of Materials

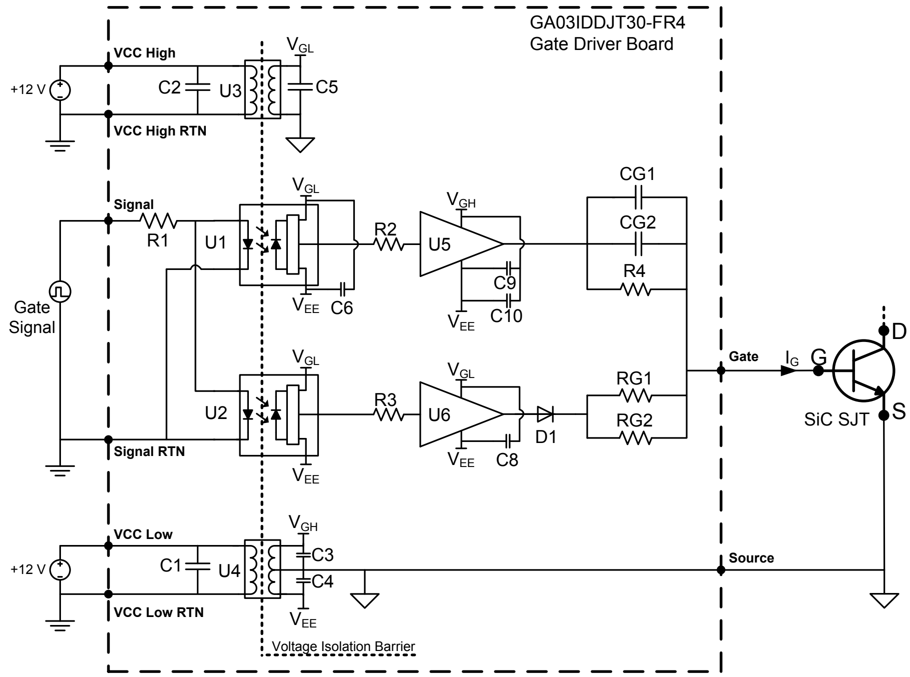

Figure 7: Gate Drive Board Detailed Block Diagram

Table 5: Gate Drive Board Bill of Materials

#ITEM	Designator	Description	Package (Metric)	Manufacturer	Manufacturer Part Number	Quantity / Board
1	C1, C2, C3, C4, C5	Capacitor, Ceramic, 1µF, 50V, 10%, X7R, 1206	3216	TDK Corporation	C3216X7R1H105K160AB	5
2	CG1, CG2	Capacitor, Ceramic, 4700pF, 250VAC, X7R, 1812	4532	Murata Electronics NA	GA343DR7GD472KW01L	2
3	C6, C7, C9	Capacitor, Ceramic, 0.1µF, 50V, 10%, X7R, 1206	3216	Yageo	CC1206KRX7R9BB104	3
4	C10	Capacitor, Ceramic, 22µF, 35V, 20%, X5R, 1206	3216	TDK Corporation	C3216X5R1V226M160AC	1
5	C8	Capacitor, Ceramic, 100µF, 16V, 20%, X5R, 1210	3225	Taiyo Yuden	EMK325ABJ107MM-T	1
6	R2, R3	Resistor, 10 Ω, 1/4W, 1%, 1206, SMD	3216	Rohm Semiconductor	MCR18ERTF10R0	2
7	R1	Resistor, 100 Ω, 1/4W, 1%, 1206, SMD	3216	Yageo	RC1206FR-07100RL	1
8	R4	Resistor, 1 KΩ, 1/4W, 1%, 1206, SMD	3216	Yageo	RC1206FR-071KL	1
9	RG1, RG2	Resistor, 7.50 Ω, 1W, 1%, 2512, SMD	6332	Vishay Dale	CRCW25127R50FKEG	2
10	D1	Schottky Diode, 60V, 2A, SMB	SMB	Fairchild Semiconductor	SS26	1
11	U1, U2	Optocoupler, 3A, 8-SMD	8-SMD	Fairchild Semiconductor	FOD3182S	2
12	GATE, SOURCE	Connector Breakaway, Header 0.100IN, 3POS, Vertical	3POS HEADER	TE Connectivity	5-146274-3	2
13	JP1	Connector Breakaway, Header 0.100IN, 6POS, Vertical	6POS HEADER	TE Connectivity	3-644456-6	1
14	U3	DC/DC Converter, 3W, V_{IN} = 12V, V_O = 5V, 7-SIP	7-SIP Module	Murata Power	MEV3S1205SC	1
15	U4	DC/DC Converter, 2W, V_{IN} = 12V, V_O = 20/- 5V Dual, 7-SIP	7-SIP Module	Murata Power	MGJ2D122005SC	1
16	U5, U6	Gate Driver IC, 9A, Non-Inverting, 8-SOIC	8-SOIC	IXYS IC	IXDN609SI	2
17	--	Gate Driver Circuit Board, 0.062" Thickness, 4oz Cu	PCB	GeneSiC Semiconductor	GA03IDDJT30-FR4	1

Section VIII: Mechanical Drawing

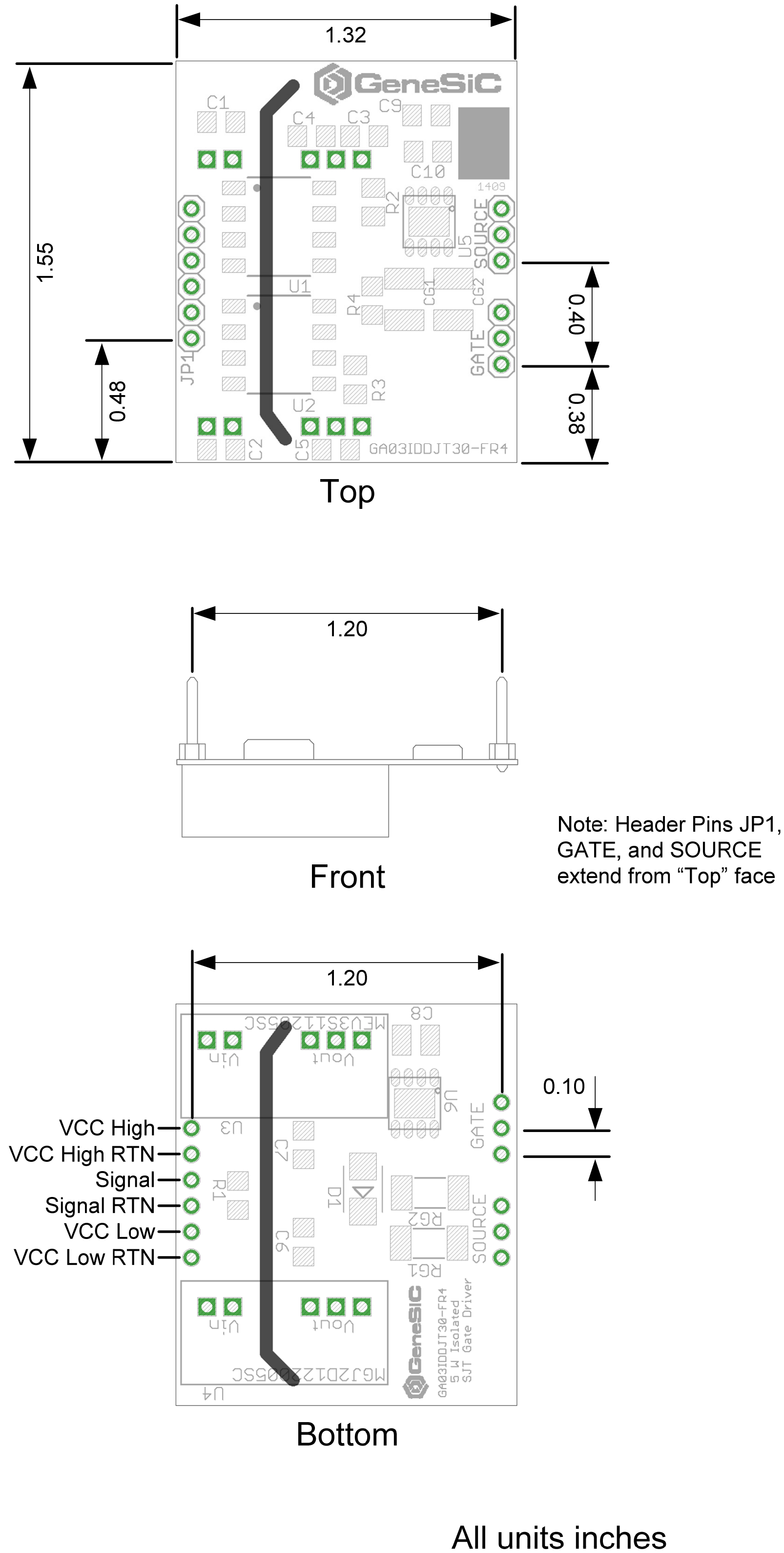

Figure 8: Gate Drive Board Mechanical Drawing

Revision History

Date	Revision	Comments	Supersedes
2014/11/14	1	Updated Characteristics	
2014/08/29	0	Initial release	

Published by
GeneSiC Semiconductor, Inc.
43670 Trade Center Place Suite 155
Dulles, VA 20166