Gate Driver for SiC SJT with Output and Signal Isolation

$V_{ISO,min}$	=	2200 V
$P_{Drive,\ cont}$	=	15 W
$P_{Drive,switch}$	=	> 3 W
f_{MAX}	=	TBD

Features

- Requires single 12 V voltage supply
- Two-voltage level topology with low drive losses
- High-side drive capable with 2200 V min. supply isolation
- 6000 V Signal Isolation (up to 10 s)
- Capable of high Gate Currents with 3 W Maximum Power

Package

- RoHS Compliant

Suitable for driving

- GA50JT12-247
- GA50JT12-247
- GA50SICP12-227
- GA100SICP12-227

Gate Drive Theory of Operation

The SJT transistor is a current controlled transistor which requires a positive gate current for turn-on as well as to remain in on-state. An ideal gate current waveform for ultra-fast switching of the SJT, while maintaining low gate drive losses, is shown in Figure 1.

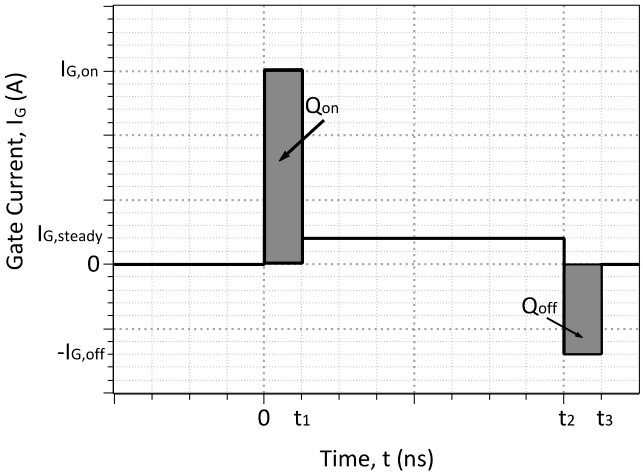

Figure 1: Idealized Gate Current Waveform

Gate Currents, $I_{G,pk}$/$-I_{G,pk}$ and Voltages during Turn-On and Turn-Off

An SJT is rapidly switched from its blocking state to on-state, when the necessary gate charge, Q_G, for turn-on is supplied by a burst of high gate current, $I_{G,on}$, until the gate-source capacitance, C_{GS}, and gate-drain capacitance, C_{GD}, are fully charged.

$$I_{G,on} * t_1 \geq Q_{gs} + Q_{gd}$$

As an example, an $I_{G,pon} \geq 3$ A is required to achieve a 25 ns V_{DS} fall time for a 800 V switching transition, due to the gate-drain charge, Q_{GD} of 77 nC for the GA20JT12-247. The $I_{G,pon}$ pulse should ideally terminate, when the drain voltage falls to its on-state value, in order to avoid unnecessary drive losses during the steady on-state. In practice, the rise time of the $I_{G,on}$ pulse is affected by the parasitic inductances, L_{par} in the TO-247 package and drive circuit. A voltage developed across the parasitic inductance in the source path, L_s, can de-bias the gate-source junction, when high drain currents begin to flow through the device. The applied gate voltage should be maintained high enough, above the $V_{GS,ON}$ level to counter these effects.

A high negative peak current, $-I_{G,off}$ is recommended at the start of the turn-off transition, in order to rapidly sweep out the injected carriers from the gate, and achieve rapid turn-off. While satisfactory turn off can be achieved with V_{GS} = 0 V, a negative gate voltage V_{GS} may be used in order to speed up the turn-off transition.

After the device is turned on, I_G may be advantageously lowered to $I_{G,steady}$ for reducing unnecessary gate drive losses. The $I_{G,steady}$ is determined by noting the DC current gain, h_{FE}, of the device.

The desired $I_{G,steady}$ is determined by the peak device junction temperature T_J during operation, drain current I_D, DC current gain h_{FE}, and a 50 % safety margin to ensure operating the device in the saturation region with low on-state voltage drop by the equation:

$$I_{G,steady} \approx \frac{I_D}{h_{FE}(T, I_D)} * 1.5$$

Implementation

Using the IXYS IX2204 Gate Driver

The IXYS IX2204 is a dual output gate drive integrated circuit which can be used to drive an SJT transistor by supplying the required gate drive current I_G in a low-power gate drive solution. This configuration features an external gate capacitor, C_G, which creates the brief current peak $I_{G,on}$ during device turn-on and $I_{G,off}$ during turn-off for fast switching and an external gate resistor $R_{G(EXT)}$ to set the continuous gate current $I_{G,steady}$ required for the device to remain on. This configuration is shown in Figure 2 with further details provided below.

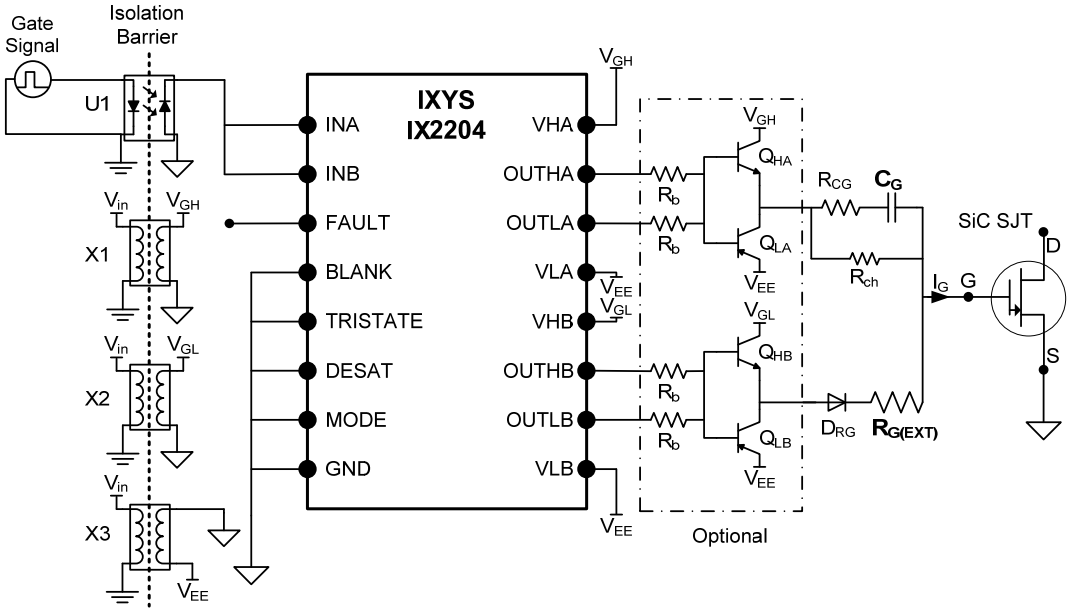

Figure 2: Gate drive configuration using an IXYS IX2204 gate drive IC.

Table 1: Recommended Component List for implementing the IX2204 based Gate Drive for the GA20JT12-247

Reference	Component	Description	Suggested Part
$R_{G(EXT)}$	Gate Resistance, External	2.2 Ω, 2 W	CRM2512-JW-2R2ELF
C_G	Gate Capacitance	10 nF	C1812C103J1GACTU
R_{CG}	Damping Resistor	1.0 Ω, 0.5 W	ERJ-1TYJ1R0U
D_{RG}	Silicon Schottky Diode	40 V, 2 A	SS24T3G
R_b	BJT Base Resistor	1.0 Ω, 0.5 W	ERJ-1TYJ1R0U
Q_{HA}, Q_{HB}	Current Boost NPN	40 V, 8 A, Silicon NPN BJT	MJD44H11
Q_{LA}, Q_{LB}	Current Boost PNP	40 V, 8 A, Silicon PNP BJT	MJD45H11
U1	Signal Isolator	Opto-Isolator –or– Transformer Isolator	ACPL-4800 / ADUM3210
X1	DC/DC Converter, V_{GH} Supply	V_{OUT} = +20 V, V_{IN} = +12 V, 2 W, V_{ISO} = 5.2 kV	MGJ2D122005SC
X2	DC/DC Converter, V_{GL} Supply	V_{OUT} = +5 V, V_{IN} = +12 V, 3 W, V_{ISO} = 3.0 kV	MEV3S1205SC
X3	DC/DC Converter, V_{EE} Supply	V_{OUT} = -5 V, V_{IN} = +12 V, 2 W, V_{ISO} = 5.2 kV	MGJ2D122005SC

Voltage Supply Selection

The IX2204 gate drive design requires three supply voltages V_{GH}, V_{GL}, and V_{EE} (listed in Table 2) optionally supplied through DC/DC converters. During device turn-on, V_{GH} charges the external capacitor C_G thereby delivering the narrow width, high current pulse $I_{G,on}$ to the SJT gate and

charges the SJT's internal terminal capacitances C_{GD} and C_{GS}. For a given level of parasitic inductance in the gate circuit and SJT package, the rise time of $I_{G,on}$ is controlled by the choice of V_{GH} and C_G. During the steady on-state, V_{GL} in combination with the internal and external gate

resistances provides a continuous gate current for the SJT to remain on. The V_{EE} supply sets the gate negative during turn-off and steady off-state for faster switching and to avoid spurious turn-on which may be caused by external circuit noise. The power rating of the voltage supplies should be adequate to meet the gate drive power requirements as determined by

$$P_{min,VGH} = \frac{1}{2}\, C_G\, V_{GH}^2\, f_{sw}$$

$$P_{min,VEE} = \frac{1}{2}\, C_G\, V_{EE}^2\, f_{sw}$$

$$P_{min,VGL} = V_{GL} I_{G,steady}\, D$$

Table 2: IX2204 Gate Drive Example Component List

Symbol	Parameter	Values	
		Range	Typical
V_{GH}	Supply Voltage, Driver Output A	15 – 20	+ 20.0
V_{GL}	Supply Voltage, Driver Output B	5.0 – 7.0	+ 5.0
V_{EE}	Negative Supply Voltage	-10 – GND	- 5.0

Gate Capacitor C_G Selection

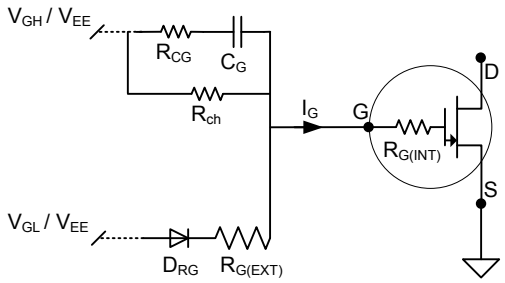

Figure 3: Primary gate drive circuit passive components with series gate resistance Schottky rectifier.

An external gate capacitor C_G connected directly to the device gate pin delivers the positive current peak $I_{G,on}$ during device turn-on and the negative current peak $I_{G,off}$ during turn-off. A low value resistor R_{CG} is connected in series with C_G to damp potential high-frequency oscillation. A high value resistor R_{ch} in parallel with C_G sets the SJT gate to a defined potential ($-V_{EE}$) during steady off-state.

At device turn-on, C_G is pulled to V_{GH} which produces a transient peak of gate voltage and current. This current peak rapidly charges the internal SJT C_{GS} and C_{GD} capacitances. A Schottky diode, D_{RG}, in series with $R_{G(EXT)}$ blocks any C_G induced current from draining out through $R_{G(EXT)}$ and ensures that all of the charge within C_G flows only into the device gate, allowing for an ultra-fast device turn-on. During steady on-state, a potential of V_{GH} - V_{GS} = V_{GH} – 3 V is across C_G. When the device is turned off, C_G is pulled to negative V_{EE} and V_{GS} is pulled to a transient peak of $V_{GS,turn-off}$ = V_{EE} – (V_{GH} – 3 V), this induces the negative current peak $I_{G,off}$ out of the gate which discharges the SJT internal capacitances.

External Gate Resistor $R_{G(EXT)}$ Selection

An external gate resistor $R_{G(EXT)}$ connected directly to the SJT gate pin acts to deliver a continuous current $I_{G,steady}$ during steady on-state. The gate current is determined by:

$$I_{G,steady} = \frac{V_{GL} - V_{GS(FWD)} - V_{Sch}}{R_{G(EXT)} + R_{G(INT)}}$$

The on-state gate-source voltage $V_{GS(FWD)}$ can be approximated to 3 V and the Schottky on-state voltage V_{Sch} can be approximated to 0.3 V which simplifies the equation to:

$$I_{G,steady} = \frac{V_{GL} - 3.3V}{R_{G(EXT)} + R_{G(INT)}}$$

The desired $I_{G,steady}$ is determined by the peak device junction temperature T_J during operation, drain current I_D, DC current gain β, and a 50 % safety margin to avoid operating the device in saturation. $I_{G,steady}$ may also be approximated from the temperature dependent on-state curves of the device, provided that a 50 % increase is given.

Table 3: Passive Output Component List

Symbol	Parameter	Values		
		Range	Typical	Units
C_G	Gate Capacitor, External	5 – 20	10	nF
R_{CG}	Damping Resistor of Gate Capacitor	0.5 – 2.0	1.0	Ω
R_{ch}	Charging Resistor	500 – 10k	1k	Ω
$R_{G(EXT)}$	Gate Resistor, External	0.5 – 10	2.0	Ω
$R_{G(INT-ON)}$	Gate Resistance, Internal, On-State	0.05 – 0.2	0.13	Ω
D_{RG}	Schottky Diode of Gate Resistor	--	--	

Optional Gate Current Boost Network

An optional output totem-pole network may be attached to the IX2204 output pins as shown in Figure 2 using either silicon BJTs (shown) or MOSFETs. This configuration allows the IX2204 to directly drive the BJT bases or MOSFET gates and not supply the full peak and steady state gate current entering the SJT gate. The primary gate current delivery device is transferred to the discrete components which have higher power dissipation ratings than the IX2204.

Voltage Supply Isolation

The DC/DC supply voltage converters are suggested to provide isolation at a minimum of twice the working V_{DS} on the SJT transistor during off-state to provide adequate protection to circuitry external to the gate drive circuit. Suggested DC/DC converters have an isolation of 3.0 kV or greater. Alternatively, DC/DC converter galvanic isolation may be bypassed and direct connection of variable voltage supplies may be done, this may be convenient during testing and prototyping but carries risk and is not suggested for extended usage.

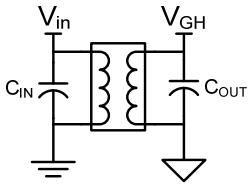

Figure 4: Typical DC/DC converter configuration

Signal Isolation

The gate supply signal is suggested to be isolated to twice the working V_{DS} on the SJT during off-state to provide adequate protection to circuitry external to the gate drive circuit. This may be done using opto or galvanic isolation techniques.

Additional Features

The IX2204 has additional functionality available which is unused in the given configuration. Desaturation detection and fault status monitoring may be implemented by un-grounding the DESAT, BLANK, and TRISTATE pins and configuring them as recommended in the IX2204 datasheet, available from IXYS. Active miller clamping is also available on other gate drive ICs which may also be desired in some SJT switching applications but is not required, refer to specific gate drive IC datasheets for more information.

Revision History			
Date	Revision	Comments	Supersedes
2014/09/15	0	Initial release	

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