HI-8456, HI-8457, HI-8458

Octal ARINC 429 Line Receivers with Integrated DO-160G Level 3 Lightning Protection

September 2017

GENERAL DESCRIPTION

Holt's family of octal ARINC 429 line receivers, HI-8456, HI-8457 and HI-8458 include internal lightning protection circuitry which ensures compliance with RTCA/DO-160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B) without the use of any external components. Each device contains 8 independent ARINC 429 line receivers. Pin surge levels for Level 3 are summarized below.

Waveform 3	Waveform 4	Waveform 5A	Waveform 5B
VOC/ISC	VOC/ISC	VOC/ISC	VOC/ISC
600V/24A	300V/60A	300V/300A	300V/300A

The devices are designed to operate from either a 5V or 3.3V supply in a high noise environment, with an input common mode voltage range of ±30V. Each receiver channel translates incoming ARINC 429 data bus signals to a pair of TTL / CMOS outputs.

In the case of HI-8456 and HI-8458, the TESTA and TESTB inputs bypass the analog inputs for testing purposes. They force the outputs of all eight receivers to the specified ZERO, ONE or NULL state. The ARINC inputs are ignored when the devices are in test mode. The HI-8456 has a single test port which controls all 8 channels simultaneously. The HI-8458 has two independent test ports, each controlling a bank of 4 channels. Test inputs are not implemented on HI-8457 and are internally connected to logic 0. The truth table for the TESTA and TESTB inputs is shown in Table 1.

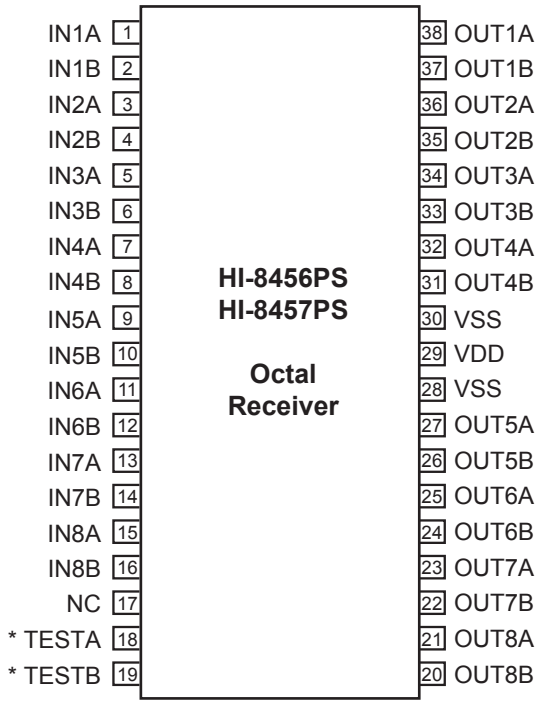
The HI-8456 and HI-8457 are exact drop in replacements for DEI1046 and DEI1047 respectively. The HI-8458 is pin-to-pin compatible with Holt's HI-8448 and is also a drop-in replacement for the DEI1148 (44-pin PQFP). A part number cross reference is included in Table 2.

The parts are available in Industrial -40°C to +85°C, or Extended, -55°C to +125°C temperature ranges. Optional burn-in is available on the extended temperature range.

FEATURES

- Internal lightning protection circuitry ensures compliance with RTCA/DO-160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B)
- Direct connection to ARINC 429 bus with no external components
- High input common mode voltage range of ±30V
- 3.3V or 5.0V single supply operation
- Test inputs bypass analog inputs and force digital outputs to a one, zero, or null state (not available on HI-8457)
- Industrial and Extended temperature ranges
- Burn-in available

PIN CONFIGURATION (TOP VIEW)



38 Pin Plastic TSSOP Package

* No Connect on HI-8457

Table 1. Function Table

ARINC INPUTS INA - INB	TESTA(1)	TESTB(1)	OUTA	OUTB
-2.5 to +2.5V	0	0	0	0
< -6.5V	0	0	0	1
> +6.5V	0	0	1	0
x	0	1	0	1
x	1	0	1	0
x	1	1	0	0

Note (1): Not available on HI-8457.

FUNCTIONAL DESCRIPTION

Figure 1 shows the general architecture of an ARINC 429 receiver. The receiver operates off the VDD supply only. The inputs INA and INB may be connected directly to the ARINC 429 bus. Internal lightning protection circuitry ensures compliance with RTCA/DO-160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B) without the use of any external components.

After level translation, the inputs are buffered and become inputs to a differential amplifier. The amplitude of the differential signal is compared to levels derived from a divider between VDD and Ground. The nominal settings correspond to a One/Zero amplitude of 6.0V and a Null amplitude of 3.3V.

The status of the ARINC receiver input is latched. A Null input resets the latches and a One or Zero input sets the latches.

The logic at the output is controlled by the test signal which is generated by the logical OR of the TESTA and TESTB pins (not available on HI-8457). If TESTA and TESTB are both One, the outputs are pulled low. This allows the digital outputs of a transmitter to be connected to the test inputs through control logic for system self-test purposes.

BLOCK DIAGRAMS

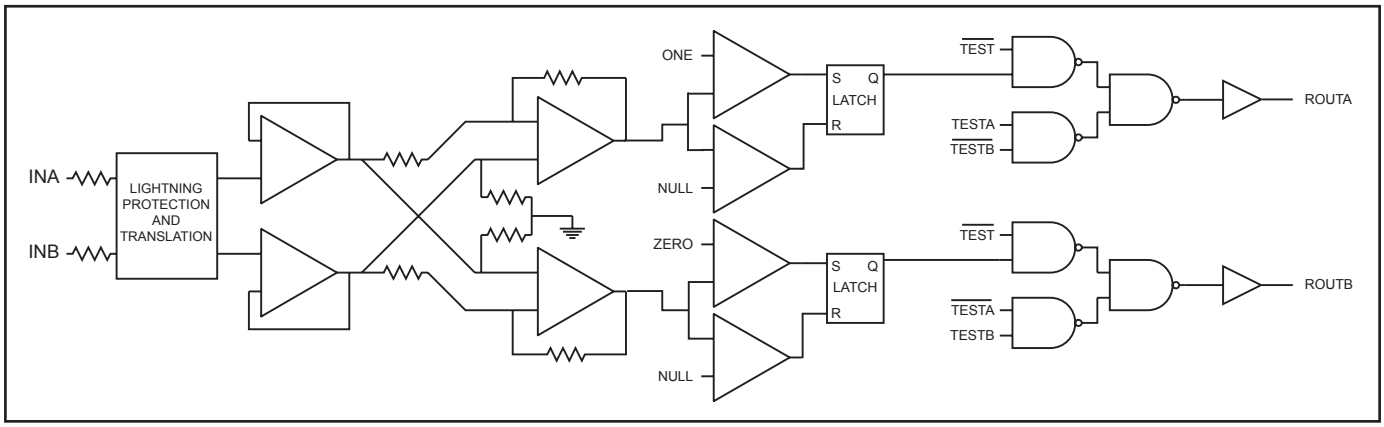


Figure 1. Line Receiver Block Diagram

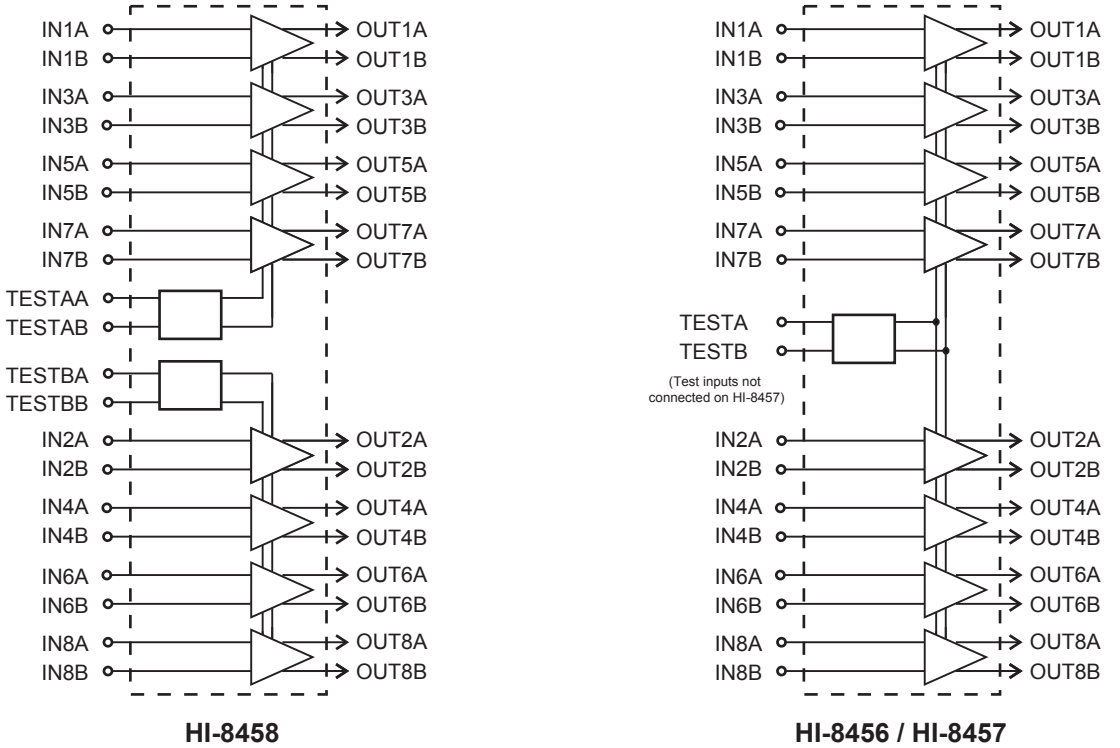


Figure 2. Block Diagrams.

Table 2. Cross Reference Table

DEI Part Number	Holt Part Number	Package	Test Inputs	Temperature Range
DEI1046-TES-G	HI-8456PSTF	38-pin TSSOP	Yes	− 55 / + 85°C
DEI1046-TMS-G	HI-8456PSTF	38-pin TSSOP	Yes	− 55 / + 125°C
DEI1047-TES-G	HI-8457PSTF	38-pin TSSOP	No	− 55 / + 85°C
DEI1047-TMS-G	HI-8457PSTF	38-pin TSSOP	No	− 55 / + 125°C
DEI1148-QES-G	HI-8458PQTF	44-pin PQFP	Yes	− 55 / + 85°C
DEI1148-QMS-G	HI-8458PQTF	44-pin PQFP	Yes	− 55 / + 125°C

PIN DESCRIPTIONS

Table 3. HI-8458 Pin Descriptions

Symbol	Function	Description
IN[8:1]A	ARINC INPUT	Receiver [8:1] positive input
IN[8:1]B	ARINC INPUT	Receiver [8:1] negative input
TESTAA	LOGIC INPUT	Positive test input A for odd channels
TESTAB	LOGIC INPUT	Negative test input A for odd channels
TESTBA	LOGIC INPUT	Positive test input B for even channels
TESTBB	LOGIC INPUT	Negative test input B for even channels
OUT[8:1]B	LOGIC OUTPUT	Receiver [8:1] “ZERO” output
OUT[8:1]A	LOGIC OUTPUT	Receiver [8:1] “ONE” output
GND	POWER	Ground supply voltage
VDD	POWER	+3.3V or +5V supply voltage
NC	No Connect	No connect

Table 4. HI-8456/HI-8457 Pin Descriptions

Symbol	Function	Description
IN[8:1]A	ARINC INPUT	Receiver [8:1] positive input
IN[8:1]B	ARINC INPUT	Receiver [8:1] negative input
TESTA	LOGIC INPUT	Positive test input (not available on HI-8457)
TESTB	LOGIC INPUT	Negative test input (not available on HI-8457)
OUT[8:1]B	LOGIC OUTPUT	Receiver [8:1] “ZERO” output
OUT[8:1]A	LOGIC OUTPUT	Receiver [8:1] “ONE” output
GND	POWER	Ground supply voltage
VDD	POWER	+3.3V or +5V supply voltage
NC	No Connect	No connect

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD})	-0.3V to +7V
Logic input voltage range	-0.3V to +5.5V
ARINC input voltage	-120V to + 120V
Solder Temperature (reflow)	260°C
Storage Temperature	-65°C to +150°C
ESD-HBM (JS-001-2012)	
Logic and supply pins	2,000V
ARINC 429 bus input pins	1,000V

RTCA/DO-160G, Section 22 pin injection	
Waveform	Voc/Isc
3	750V/40A
4	700V/100A
5A	700V/500A
5B	700V/500A

RECOMMENDED OPERATING CONDITIONS

Supply Voltages	
V_{DD}	3.0V to +5.5V
Temperature Range	
Industrial Screening	-40°C to +85°C
Extended Temp Screening ...	-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

ELECTRICAL CHARACTERISTICS

Table 5. DC Electrical Characteristics

V_{DD} = +5.0V ± 10% or +3.3V ± 10%, GND = 0V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters		Symbol	Test Conditions	Min	Typ	Max	Units
ARINC INPUTS							
Input Voltage	ONE or ZERO	V_{DIN}	Differential Input voltage	6.5	10	13	V
	NULL	V_{NIN}	Differential Input voltage			2.5	V
	Common mode	V_{COM}	With respect to GND	−30		+30	V
Input Resistance	INA to INB	R_{DIFF}	Supplies floating	280			kΩ
	Input to GND or V_{DD}	R_{SUP}	Supplies floating	140			kΩ
Input Hysteresis		V_{HYS}		0.5	1.0		V
Input Capacitance	ARINC differential	C_{AD}			5	10	pF
	ARINC single ended to GND	C_{AS}				10	pF
TEST INPUTS							
Logic Input Voltage	High	V_{IH}		2.0			V
	Low	V_{IL}				0.8	V
Logic Input Current	Sink	I_{IH}	$V_{IH} = V_{DD}$			200	µA
	Source	I_{IL}	V_{IL} = 0V	-1.0			µA
OUTPUTS							
Logic Output Voltage (CMOS)	High	V_{OHC}	I_{OH} = -100µA	V_{DD}−0.2			V
	Low	V_{OLC}	I_{OL} = 100µA			GND+0.2	V
SUPPLY CURRENT							
V_{DD} Current		I_{DD}	High-speed. 100% duty cycle. C_L = 15pF. V_{DD} = 5.5V.			18	mA

Table 6. AC Electrical Characteristics

V_{DD} = +5.0V ± 10% or +3.3V ± 10%, GND = 0V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS						
Propagation Delay IN to OUT	t_{LH}	C_L = 50pF		150	300	ns
	t_{HL}	C_L = 50pF		150	300	ns
Output Rise Time	t_R	10% to 90%		15	50	ns
Output Fall Time	t_F	90% to 10%		15	50	ns
Propagation Delay TEST to OUT	t_{TOH}			50		ns
	t_{TOL}			50		ns

LIGHTNING INDUCED TRANSIENT VOLTAGE WAVEFORMS

Waveform 3.

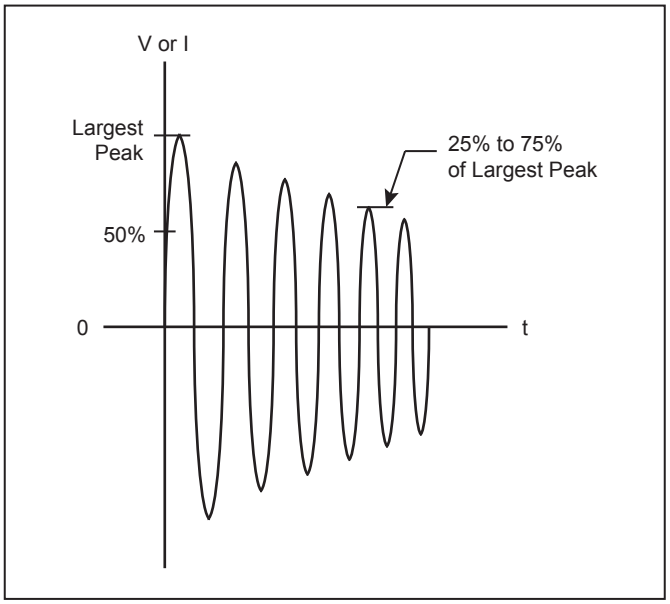


Figure 3. DO-160G Lightning Induced Transient Voltage Waveform 3.
Voc = 600V, Isc = 24A, Frequency = 1MHz ± 20%.

Waveform 4.

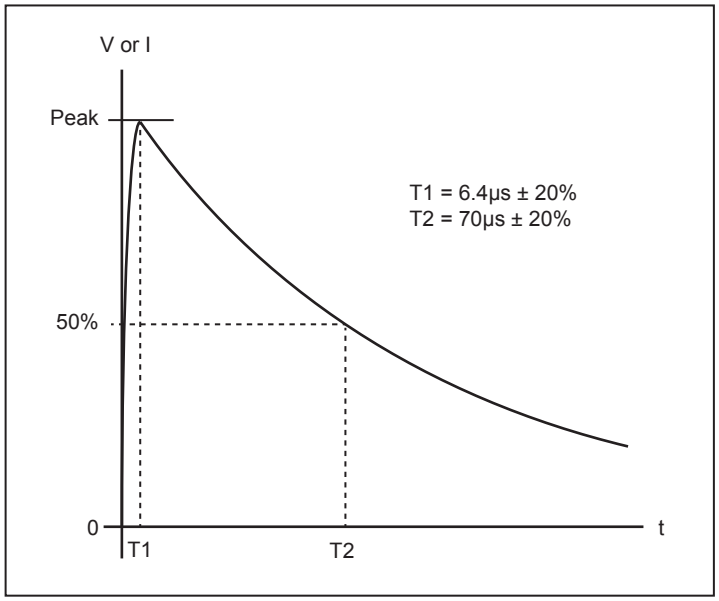


Figure 4. DO-160G Lightning Induced Transient Voltage Waveform 4.
Voc = 300V, Isc = 60A.

Waveform 5.

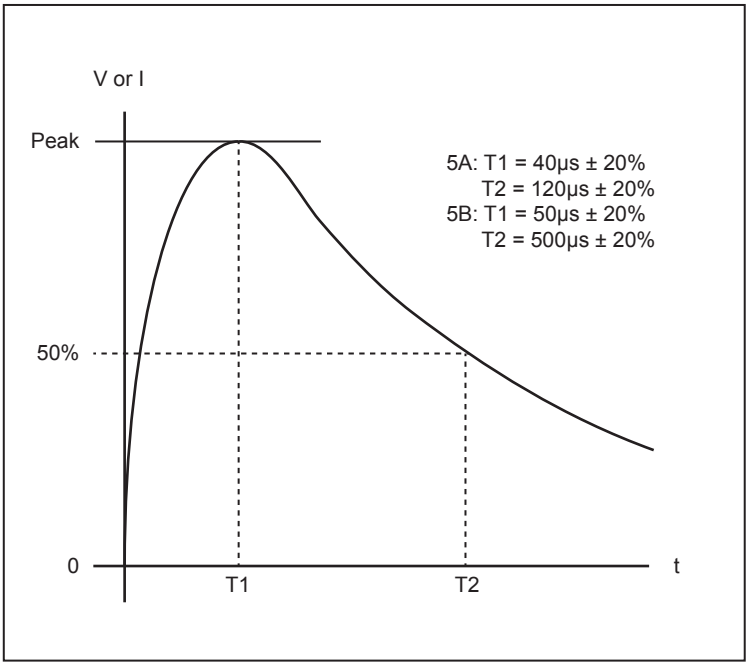
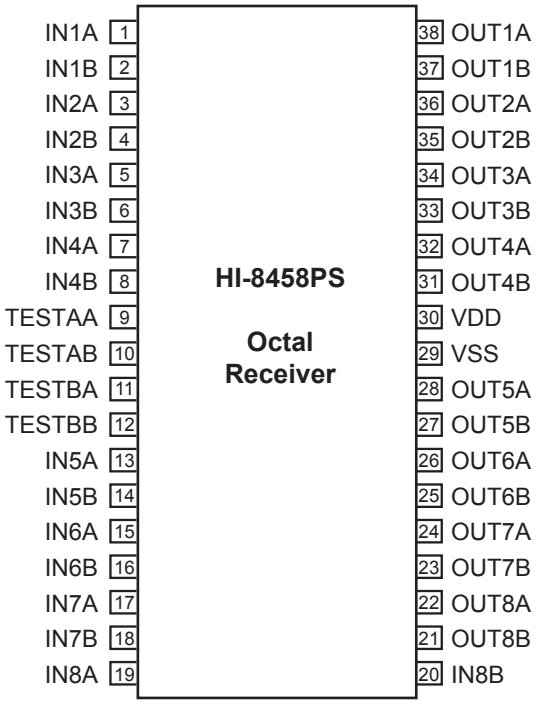
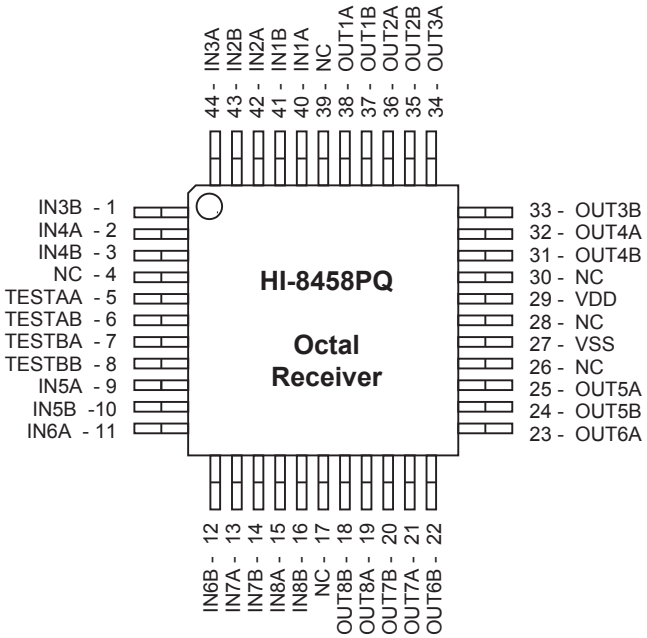


Figure 5. DO-160G Lightning Induced Transient Voltage Waveforms 5A and 5B.
Voc = 300V, Isc = 300A.

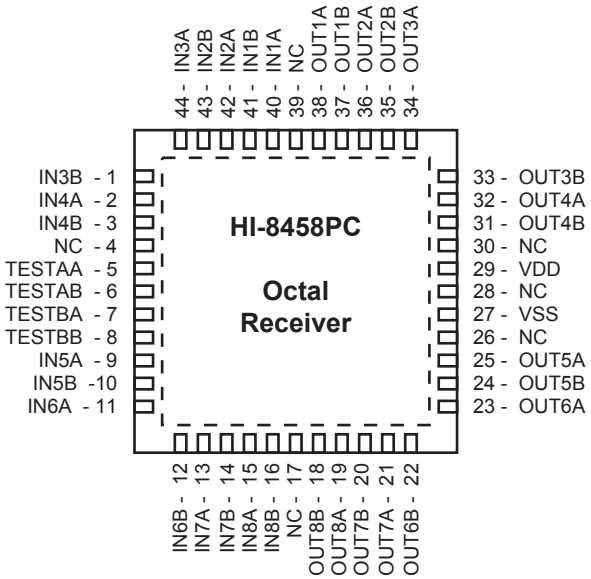
ADDITIONAL PACKAGE AND PIN CONFIGURATIONS



38 Pin Plastic TSSOP Package



44-Pin Plastic Quad Flat Pack (PQFP)



44-Pin Plastic QFN

ORDERING INFORMATION

HI - 845xxx x x (Plastic)

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No
M	-55°C to +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION	TEST PINS
8456PS	38 PIN PLASTIC TSSOP (38HS)	Y
8457PS	38 PIN PLASTIC TSSOP (38HS)	N
8458PS	38 PIN PLASTIC TSSOP (38HS)	Y
8458PQ	44 PIN PLASTIC QUAD FLAT PACK (44PMQS)	Y
8458PC	44 PIN PLASTIC QFN (44PCS)	Y

REVISION HISTORY

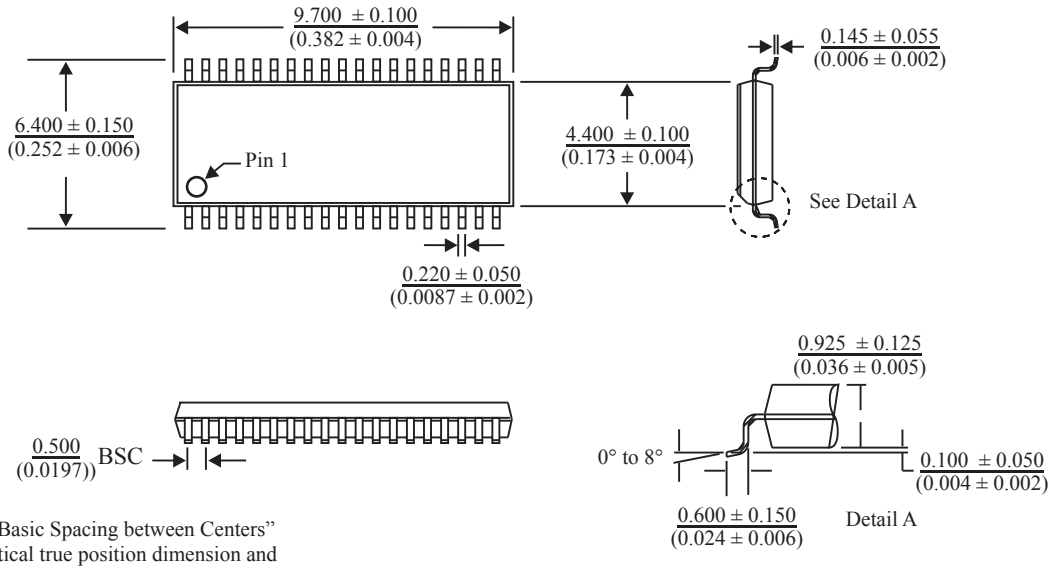
Revision	Date	Description of Change
DS8458, Rev. New.	01/27/16	Initial Release
Rev. A	04/01/16	Correct typos on 44-pin PQFP and QFN packages (Pin 26 listed twice).
Rev. B	08/11/16	Remove Logic Output Voltage spec. (VOH, VOL). Use CMOS spec. (V_{OHC}, V_{OLC}).
Rev. C	12/05/16	Remove Power Dissipation spec from “Absolute Maximum Ratings”. Update Supply Current spec in “Electrical Characteristics”.
Rev. D	06/28/17	Update lightning waveforms Voc value in “Absolute Maximum Ratings” table.
Rev. E	09/20/17	Update Functional Description.

PACKAGE DIMENSIONS

38-PIN PLASTIC TSSOP

millimeters (inches)

Package Type: 38HS

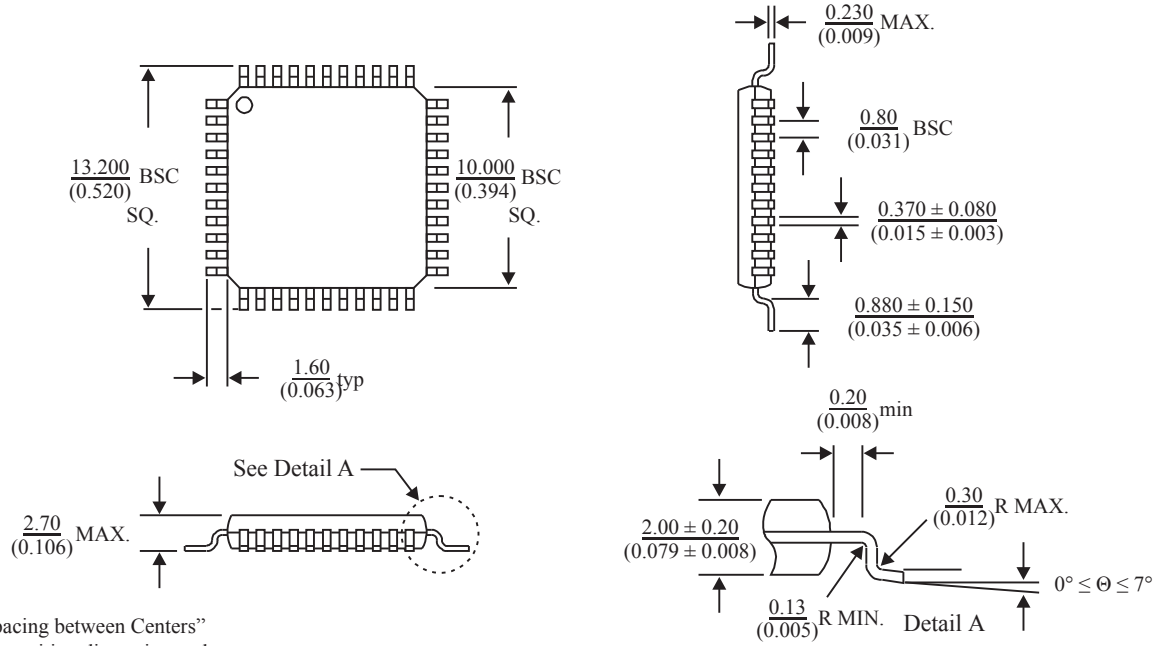


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

44-PIN PLASTIC QUAD FLAT PACK (PQFP)

millimeters (inches)

Package Type: 44PMQS

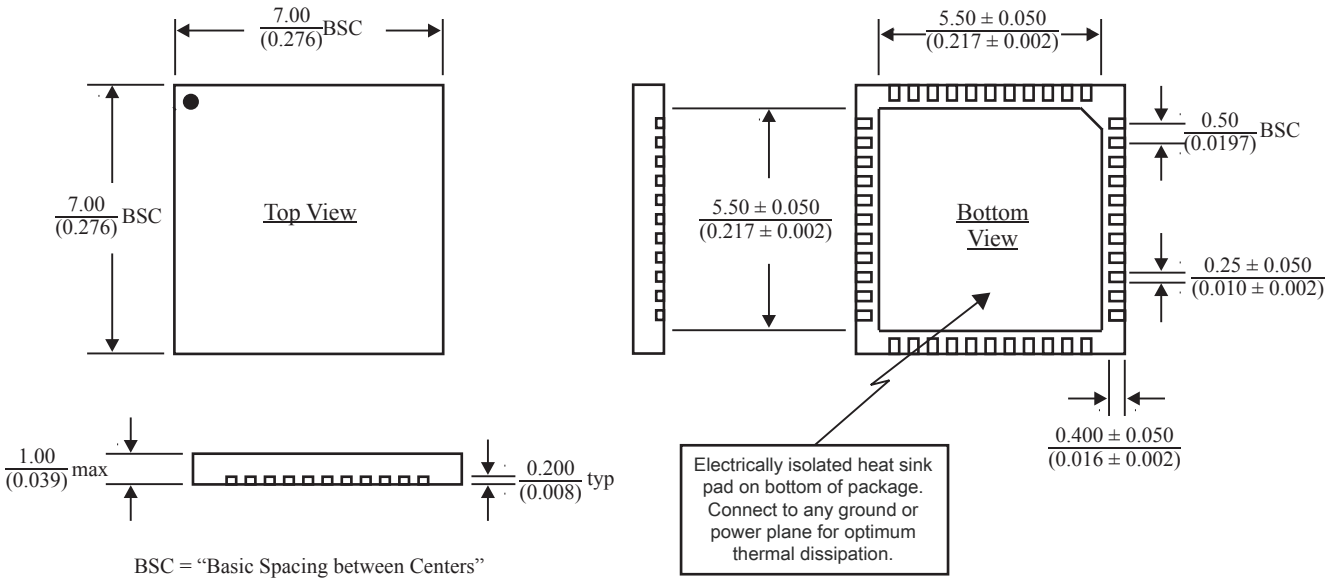


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

44-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

millimeters (inches)

Package Type: 44PCS



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)