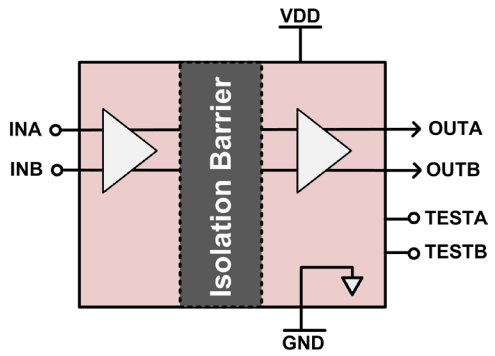
HI-8460, HI-8461

Galvanically Isolated ARINC 429 Line Receiver with Integrated DO-160 Level 3 Lightning Protection

May 2018

GENERAL DESCRIPTION

The HI-8460 and HI-8461 are galvanically isolated single ARINC 429 line receivers with internal lightning protection circuitry. The devices are available in compact 16-pin QFN and 8-pin SOIC packages. Capacitive isolation and power regulation provide 800V isolation between the line receiver and the logic interface. This is an ideal device for systems that must tolerate different grounds. Although power and ground are isolated between the line receiver and the logic interface, the IC only requires one VDD and one GND. This allows the SO-8 version of HI-8460 to be pin for pin compatible with the HI-8450, HI-8588 and HI-8591, making it easy to add galvanic isolation and lightning level 3 compliance to existing sockets.



The internal lightning protection circuitry ensures compliance with RTCA/DO-160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B) without the use of any external components. Pin surge levels for Level 3 are summarized below.

Waveform 3	Waveform 4	Waveform 5A	Waveform 5B
VOC/ISC 600V/24A	VOC/ISC 300V/60A	VOC/ISC 300V/300A	VOC/ISC 300V/300A

The devices are designed to operate from a 3.3V supply. Each receiver channel translates incoming ARINC 429 data bus signals to a pair of TTL / CMOS outputs.

The TESTA and TESTB inputs bypass the analog inputs for testing purposes. They force the receiver outputs to the specified ZERO, ONE or NULL state. The ARINC inputs are ignored when the devices are in test mode.

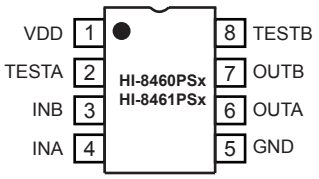
The HI-8461 produces a low output when the TESTA and TESTB inputs are held high, whereas the HI-8460 produces a high impedance output when the TESTA and TESTB inputs are held high.

The parts are available in Industrial -40°C to +85°C, or Extended -55°C to +125°C temperature ranges. Optional burn-in is available on the extended temperature range.

FEATURES

- Airbus ABD0100H specification compliant Galvanically isolated ARINC 429 receiver providing 800V isolation between the line receiver and the logic interface
- Drop-in compatible with HI-8450/51, HI-8588 and HI-8591
- Internal lightning protection circuitry ensures compliance with RTCA/DO-160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B)
- Direct connection to ARINC 429 bus with no external components
- 3.3V single supply operation
- Ultra low supply current
- Test inputs bypass analog inputs and force digital outputs to a one, zero, or null state
- Industrial and Extended temperature ranges
- Burn-in available

PIN CONFIGURATION (TOP VIEW



8-PIN PLASTIC SOIC - NB

Table 1. Function Table

ARINC INPUTS INA - INB	TESTA	TESTB	OUTA	OUTB
-2.5 to +2.5V	0	0	0	0
< -6.5V	0	0	0	1
> +6.5V	0	0	1	0
x	0	1	0	1
x	1	0	1	0
x	1	1	HI-Z (1)	HI-Z (1)
x	1	1	0 (2)	0 (2)

Note (1): HI-8460 only.

Note (2): HI-8461 only.

FUNCTIONAL DESCRIPTION

Figure 1 shows the general architecture of the galvanically isolated ARINC 429 receiver. The inputs INA and INB may be connected directly to the ARINC 429 bus. Internal lightning protection circuitry ensures compliance with RTCA/DO-160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B) without the use of any external components.

The inputs go into a differential amplifier where the signal is compared to internally generated levels. The amplifier output signal is encoded, then capacitively coupled across the galvanic isolation barrier. On the host interface side, the signal is decoded. The status of the ARINC receiver input is then latched. A Null input resets the latches and a One or Zero input sets the latches.

The logic at the output is controlled by the test signal which is generated by the logical OR of the TESTA and TESTB pins. This allows control logic to be connected to the test inputs for system self-test purposes. If TESTA and TESTB are both One, the outputs are pulled low (HI-8461 only). In the case of HI-8460, if TESTA and TESTB are both One, the outputs are high impedance (HI-Z).

BLOCK DIAGRAM

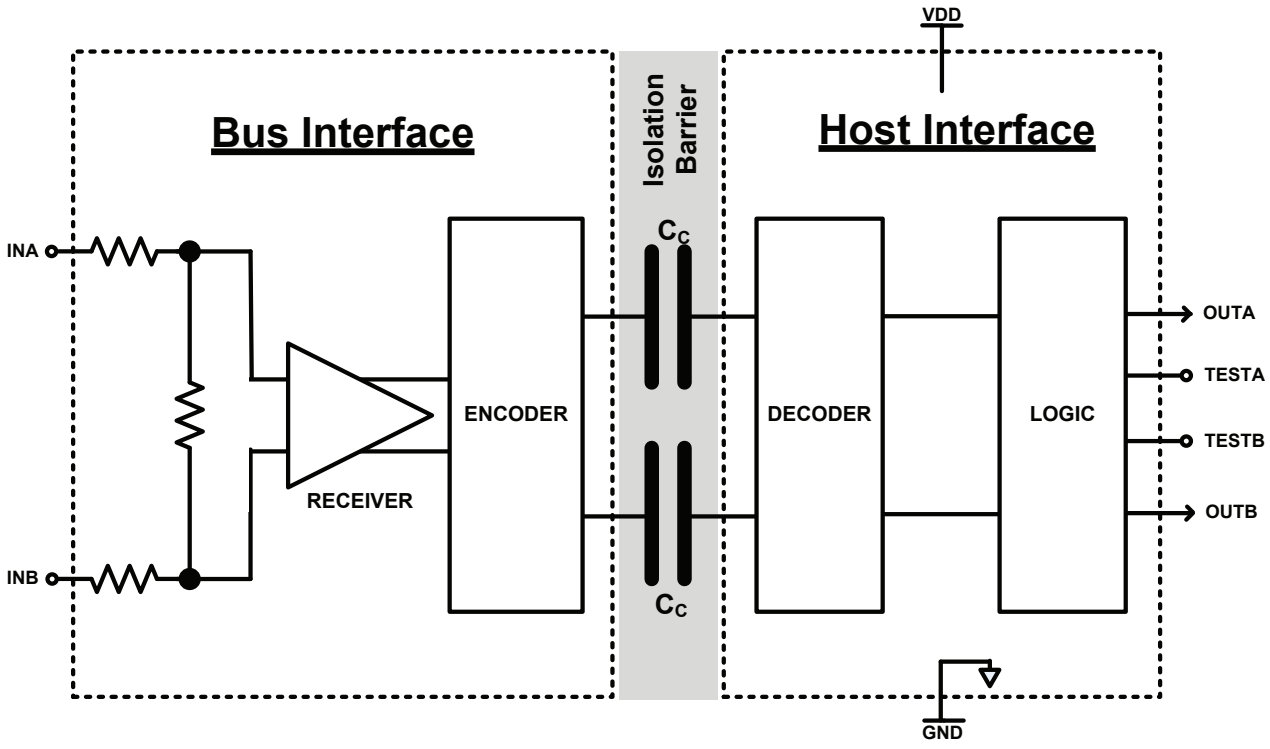


Figure 1. Galvanically Isolated Line Receiver Block Diagram

PIN DESCRIPTIONS

Table 2. Pin Descriptions

Symbol	Function	Description
VDD	POWER	+3.3V supply voltage
TESTA	LOGIC INPUT	Test input
INB	ARINC INPUT	Receiver negative input
INA	ARINC INPUT	Receiver positive input
GND	POWER	Ground supply voltage
OUTA	LOGIC OUTPUT	Receiver “ONE” output
OUTB	LOGIC OUTPUT	Receiver “ZERO” output
TESTB	LOGIC INPUT	Test input
NC	Not connected	Not connected

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD})	-0.3V to +7.0V
Logic input voltage range	-0.3V to VDD + 0.6V
Voltage at pins INA and INB	-1,000V to +1,000V
Power dissipation at 25°C	350mW
Common-Mode Input Voltage (with respect to GND)	+/- 1,000V
Solder Temperature (reflow)	260°C
Storage Temperature	-65°C to +150°C

RTCA/DO-160G, Section 22 pin injection	
Waveform	Voc/Isc
3	1,000V/40A
4	500V/100A
5A	500V/500A
5B	500V/500A

RECOMMENDED OPERATING CONDITIONS

Supply Voltages	
V_{DD}	+3.3V ± 5%
Temperature Range	
Industrial Screening	-40°C to +85°C
Extended Temp Screening ...	-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

ELECTRICAL CHARACTERISTICS

Table 3. DC Electrical Characteristics

V_{DD} = +3.3V ± 5%, GND = 0V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters		Symbol	Test Conditions	Min	Typ	Max	Units
ARINC INPUTS							
Input Voltage	ONE or ZERO	V_{DIN}	Differential Input voltage	6.5	10	13	V
	NULL	V_{NIN}	Differential Input voltage			2.5	V
	Common mode	V_{COM}	with respect to GND			± 800	V
Input Resistance	INA to INB	R_{DIFF}	Dynamic		28		kΩ
	Input to GND_{DD}	R_{SUP}		10^9			kΩ
Input Hysteresis		V_{HYS}	3.3V	0.15	0.4		V
Input Capacitance	ARINC differential	C_{AD}			19	30	pF
	ARINC single ended to GND	C_{AS}				30	pF
DC Isolation Voltage	All inputs with respect to bus pins					± 800	V
TEST INPUTS							
Logic Input Voltage	High	V_{IH}		70%V_{DD}		V_{DD} + 0.3	V
	Low	V_{IL}		-0.3		30%V_{DD}	V
Logic Input Current	Sink	I_{IH}	$V_{IH} = V_{DD}$			200	µA
	Source	I_{IL}	V_{IL} = 0V	-1.0			µA
OUTPUTS							
Logic Output Voltage (CMOS)	High	V_{OHC}	I_{OH} = -1µA	90%			V_{DD}
	Low	V_{OLC}	I_{OL} = 1µA			10%	V_{DD}
SUPPLY CURRENT							
V_{DD} Current (HI-8460, HI-8461)		I_{DD}	V_{DD} = 3.3V		200		µA

Table 4. AC Electrical Characteristics

V_{DD} = +3.3V ± 5%, GND = 0V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS						
Propagation Delay IN to OUT	t_{LH}	C_L = 50pF		0.75	1.5	µs
	t_{HL}	C_L = 50pF		0.75	1.5	µs
Output Rise Time	t_R	10% to 90%, C_L = 50pF		8	16	ns
Output Fall Time	t_F	90% to 10%, C_L = 50pF		8	16	ns
Propagation Delay TEST to OUT	t_{TOH}	C_L = 50pF		50	125	ns
	t_{TOL}	C_L = 50pF		50	125	ns
Test Mode Operating Frequency		C_L = 50pF			25	MHz

LIGHTNING INDUCED TRANSIENT VOLTAGE WAVEFORMS

Waveform 3.

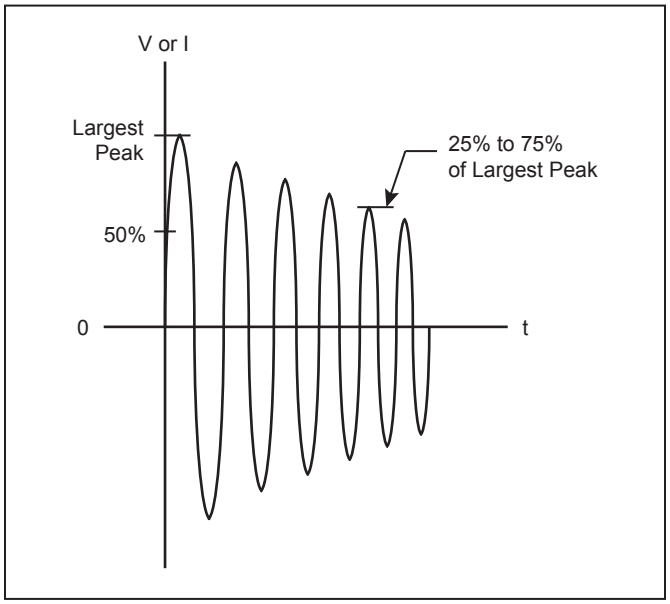


Figure 2. DO-160G Lightning Induced Transient Voltage Waveform 3.
Voc = 600V, Isc = 24A, Frequency = 1MHz ± 20%.

Waveform 4.

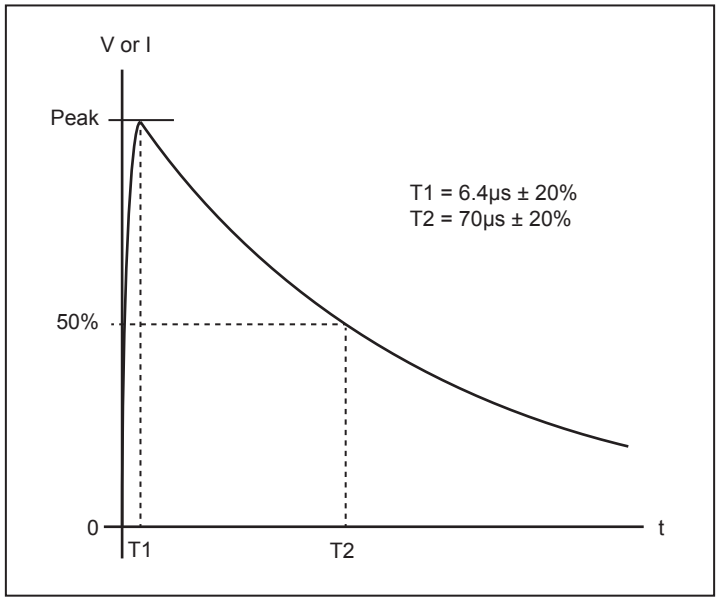


Figure 3. DO-160G Lightning Induced Transient Voltage Waveform 4.
Voc = 300V, Isc = 60A.

Waveform 5.

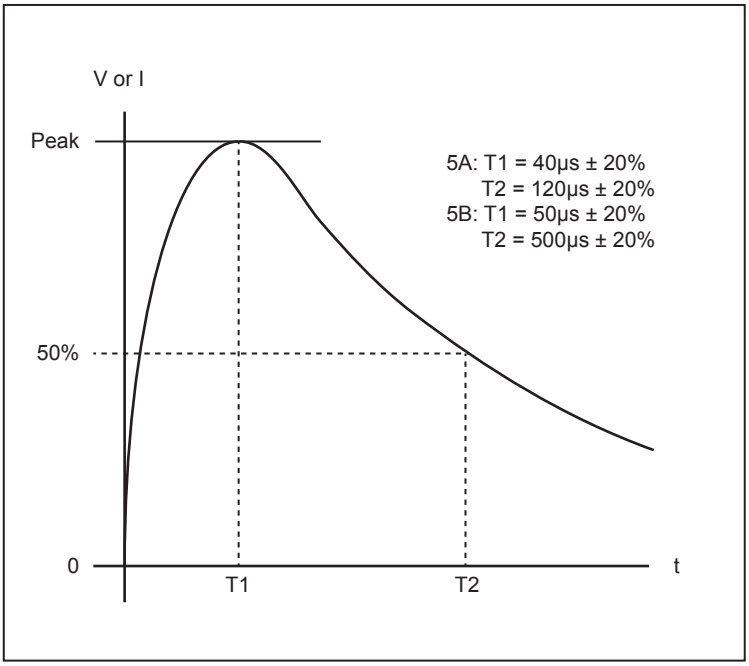
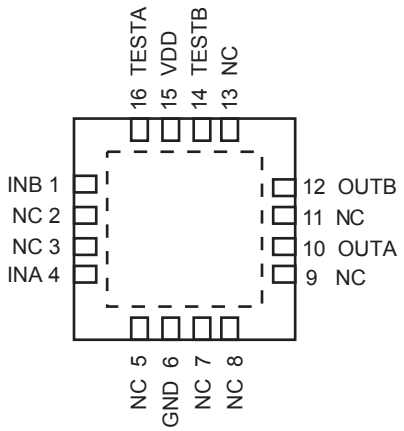


Figure 4. DO-160G Lightning Induced Transient Voltage Waveforms 5A and 5B.
Voc = 300V, Isc = 300A.

ADDITIONAL PACKAGES



16-Pin 4mm x 4mm QFN

ORDERING INFORMATION

HI - 846xxx x x (Plastic)

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No
M	-55°C to +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION
8460PS	8 PIN PLASTIC NARROW BODY SOIC (8HN)
8460PC	16 PIN PLASTIC 4x4 mm QFN (16PCS); not available with “M” flow
8461PS	8 PIN PLASTIC NARROW BODY SOIC (8HN)
8461PC	16 PIN PLASTIC 4x4 mm QFN (16PCS); not available with “M” flow

REVISION HISTORY

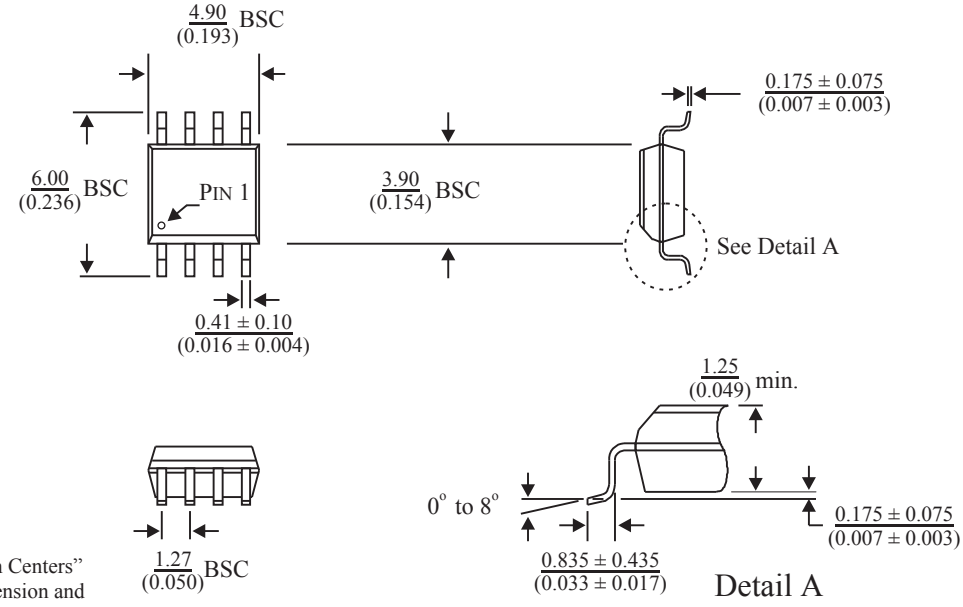
Revision	Date	Description of Change
DS8460 Rev. New.	03/17/17	Initial Release
Rev. A	05/17/17	Add “Ultra Low Supply Current” to Features.
Rev. B	05/22/18	Update Logic Output Voltage and Propagation Delays in “Electrical Characteristics”.

PACKAGE DIMENSIONS

8-PIN PLASTIC SMALL OUTLINE (SOIC) - NB
(Narrow Body)

millimeters (inches)

Package Type: 8HN

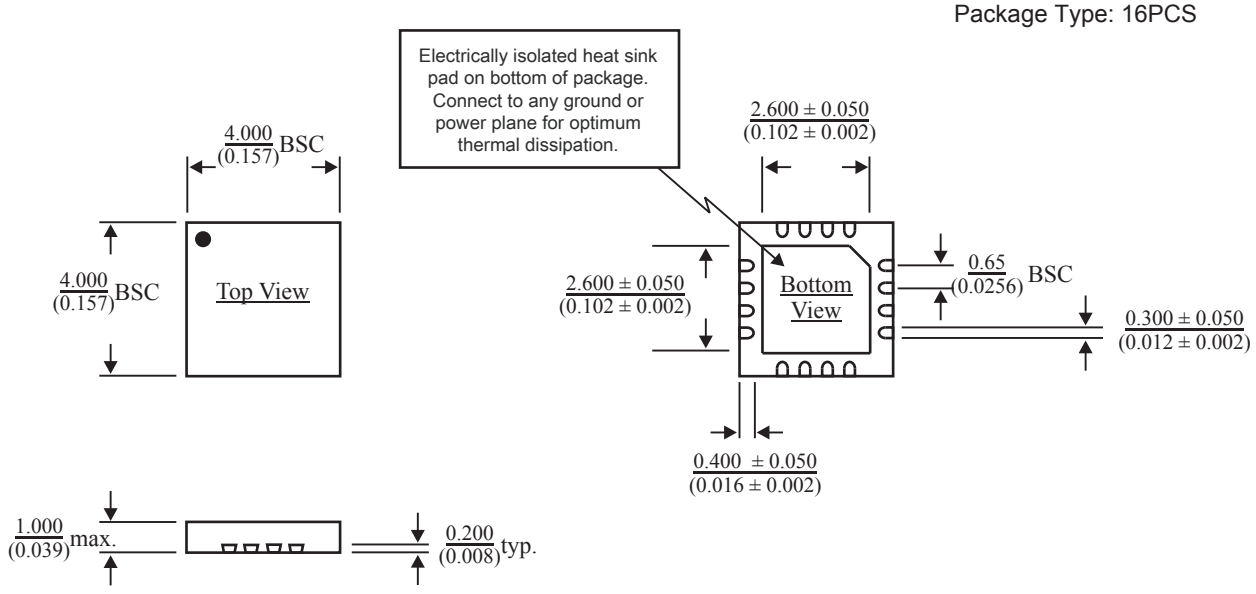


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

16-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

millimeters (inches)

Package Type: 16PCS



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