HOLT INTEGRATED CIRCUITS INC.

HI-8588-10

ARINC 429
Line Receiver

August 2014

DESCRIPTION

The HI-8588-10 ARINC 429 bus interface receiver is similar to the HI-8588 with the exception that it allows an external 10 Kohm resistor in series with each ARINC input without affecting the ARINC input thresholds. The product is especially useful in applications where lightning protection circuitry is also required. In addition, the test inputs force both of the outputs to zero instead of open circuit. The analog/digital CMOS product requires only a 5 volt supply and is available in a 8-pin SOIC package.

Each side of the ARINC bus must be connected through a 10 Kohm series resistor in order for the chip to detect the correct ARINC levels. The typical 10 volt differential signal is translated and input to a window comparator and latch. The comparator levels are set so that with the external 10 Kohm resistors they are just below the standard 6.5 volt minimum ARINC data threshold and just above the standard 2.5 volt maximum ARINC null threshold.

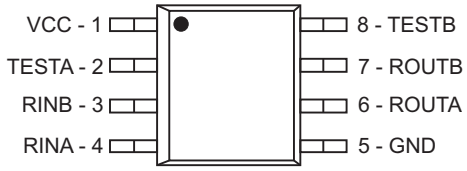
The TESTA and TESTB inputs bypass the analog inputs for testing purposes. Also if TESTA and TESTB are both taken high, the digital outputs are forced to zero.

See Holt Application Note AN-300 for more information on lightning protection.

FEATURES

- ARINC 429 line receiver interface in a small outline package
- Lightning protection simplified with the ability to add 10 Kohm external series resistors
- Receiver input hystersis at least 2 volts
- Test inputs bypass analog inputs and force digital outputs to an one, zero or null state
- Plastic and ceramic package options - surface mount and DIP

PIN CONFIGURATION



HI-8588PSI-10, HI-8588PST-10 & HI-8588PSM-10
8 - PIN PLASTIC NARROW BODY SOIC

SUPPLY VOLTAGES

VCC = 5.0V ± 5%

FUNCTION TABLE

RECEIVER

RINA	RINB	TESTA	TESTB	ROUTA	ROUTB
-1.25V to 1.25V	-1.25V to 1.25V	0	0	0	0
-3.25V to -6.5V	3.25V to 6.5V	0	0	0	1
3.25V to 6.5V	-3.25V to -6.5V	0	0	1	0
X	X	0	1	0	1
X	X	1	0	1	0
X	X	1	1	0	0

PIN DESCRIPTION TABLE

PIN	SYMBOL	FUNCTION	DESCRIPTION
1	VCC	SUPPLY	5 VOLT SUPPLY
2	TESTA	LOGIC INPUT	CMOS
3	RINB	ARINC INPUT	RECEIVER B INPUT
4	RINA	ARINC INPUT	RECEIVER A INPUT
5	GND	POWER	GROUND
6	ROUTA	LOGIC OUTPUT	RECEIVER CMOS OUTPUT A
7	ROUTB	LOGIC OUTPUT	RECEIVER CMOS OUTPUT B
8	TESTB	LOGIC INPUT	CMOS

FUNCTIONAL DESCRIPTION

RECEIVER

Figure 1 shows the general architecture of the ARINC 429 receiver. The receiver operates off the VCC supply only. The inputs RINA and RINB each require 35KΩ of resistance of which 25KΩ is internal to the chip. The series resistance is connected to level translators whose resistance to Ground is typically 10KΩ. In order for the voltage translation not to be adversely affected, an external 10KΩ series resister must be added to each ARINC input. The HI-8588-10 device is typically chosen for applications where external series resistors are required in its lightning protection circuitry.

After level translation, the inputs are buffered and become inputs to a differential amplifier. The amplitude of the differential signal is compared to levels derived from a divider between VCC and Ground. The nominal settings correspond to a One/Zero amplitude of 6.0V and a Null amplitude of 3.3V.

The status of the ARINC receiver input is latched. A Null input resets the latches and a One or Zero input sets the latches.

The logic at the output is controlled by the test signal which is generated by the logical OR of the TESTA and TESTB pins. Unlike the HI-8588, if TESTA and TESTB are both One, the HI-8588-10 outputs are pulled low instead of being tri-stated. This allows the digital outputs of a transmitter to be connected to the test inputs through control logic for self-test purposes.

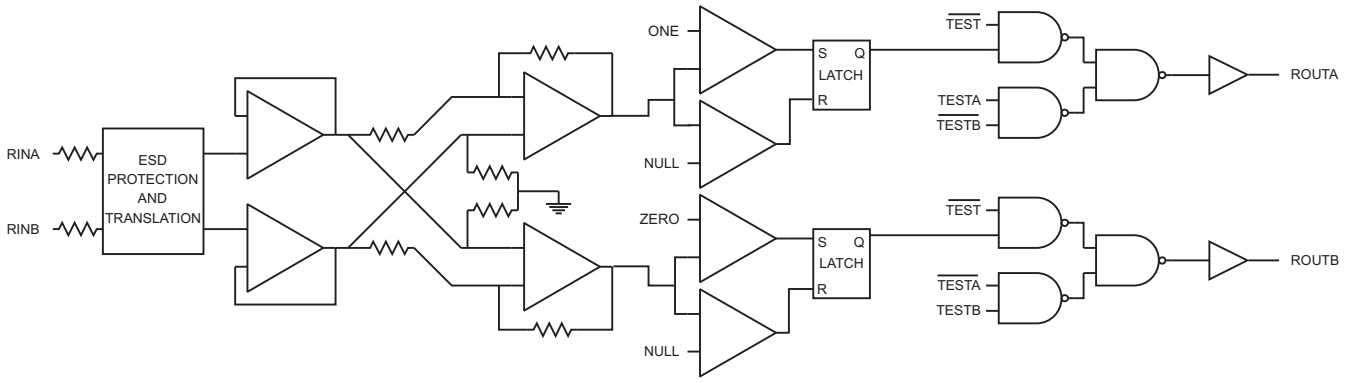


FIGURE 1 - RECEIVER BLOCK DIAGRAM

APPLICATION INFORMATION

Figure 2 shows a possible application of the HI-8588-10 interfacing an ARINC receive channel to the HI-6010 which in turn interfaces to an 8-bit bus.

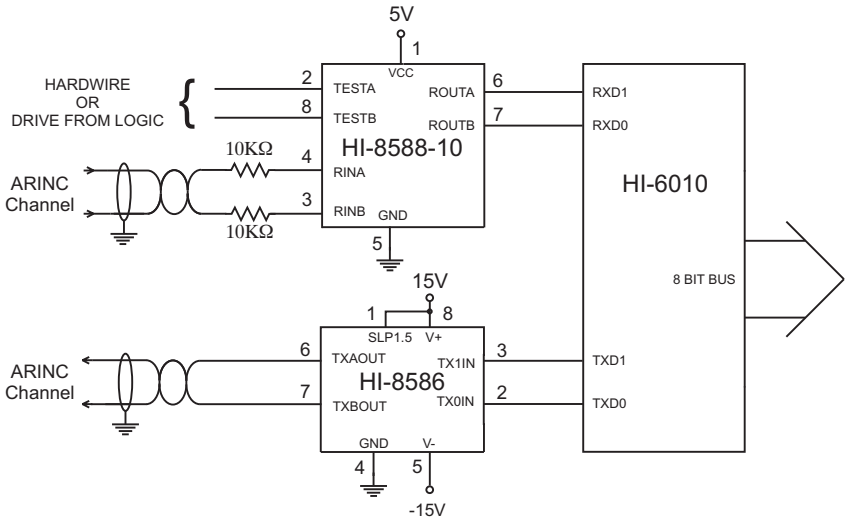


FIGURE 2 - APPLICATION DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to Ground

Supply voltages
VCC.....7V

ARINC input - pins 3 & 4
Voltage at either pin.....+120V to -120V

DC current per input pin..... ±10mA

Power dissipation at 25°C
plastic DIP.....0.7W
ceramic DIP.....0.5W

Solder Temperature (reflow) .....260°C

Storage Temperature.....-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltages
VCC.....5V ± 5%

Temperature Range
Industrial Screening.....-40°C to +85°C
Hi-Temp Screening.....-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

DC ELECTRICAL CHARACTERISTICS

OPERATING TEMPERATURE RANGE, VCC = 5.0V UNLESS OTHERWISE STATED

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ARINC input voltage						
one or zero	V_{DIN}	diff. volt. thru 10KΩ, pins 3 & 4	6.5	10	13	volts
null	V_{NIN}	" " "	-	-	2.5	volts
common mode	V_{COM}	with respect to Ground	-	-	5.0	volts
logic input voltage						
high	V_{IH}		3.5	-	-	volts
low	V_{IL}		-	-	1.5	volts
ARINC input resistance						
RINA to RINB	R_{DIFF}	supplies floating & series 10KΩ	30	75	-	Kohm
RINA or RINB to Gnd or VCC	R_{SUP}	" " "	19	40	-	Kohm
logic input current						
source	I_{IH}	V_{IN} = 0 V	-	-	0.1	μA
sink	I_{IL}	V_{IN} = 5 V	-	-	0.1	μA
logic output drive current						
one	I_{OH}	V_{OH} = 4.6V	-	-1.6	-0.8	mA
zero	I_{OL}	V_{OL} = 0.4V	3.6	5.6	-	mA
Current drain						
operating	I_{CC1}	pins 2, 8 = 0V; pins 3, 4 open	-	2.3	6.3	mA

AC ELECTRICAL CHARACTERISTICS

OPERATING TEMPERATURE RANGE, VCC = 5.0V UNLESS OTHERWISE STATED

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Receiver propagation delay		defined in Figure 3, C_L= 50pF				
Output high to low	t_{phlr}		-	600	-	ns
Output low to high	t_{plhr}		-	600	-	ns
Receiver output transition times						
Output high to low	t_{fr}		-	50	80	ns
Output low to high	t_{rr}		-	50	80	ns
Input capacitance (1)						
ARINC differential	C_{AD}		-	5	10	pF
ARINC single ended to Ground	C_{AS}		-	-	10	pF
Logic	C_{IN}		-	-	10	pF

Notes: 1. Guaranteed but not tested

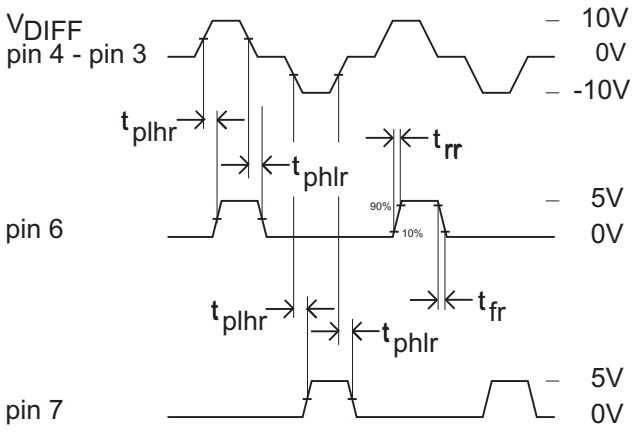


FIGURE 3 - RECEIVER TIMING

ORDERING INFORMATION

HI - 8588 xx x x - 10

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No
M	-55°C TO +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION
PD	8 PIN PLASTIC DIP (8P) not available with “M” flow
PS	8 PIN PLASTIC NARROW BODY SOIC (8HN)
CR	8 PIN CERDIP (8D) not available Pb-free

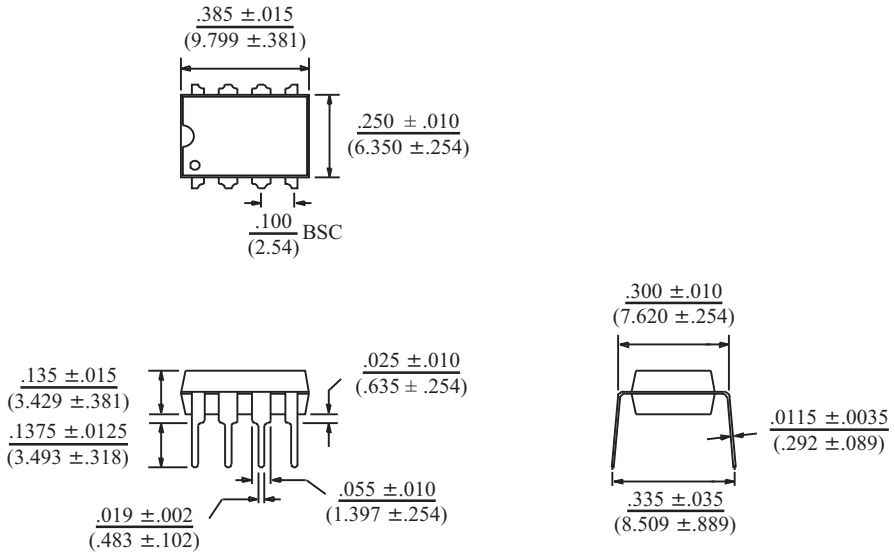
REVISION HISTORY

P/N	Rev	Date	Description of Change
DS8488-10	E	08/05/14	Update ARINC input pins 3 & 4 Absolute Maximum Rating to +/-120V. Update solder reflow temperature. Remove Mil. temperature rating. Update SOIC-8 (8HN) package drawing.

8-PIN PLASTIC DIP

inches (millimeters)

Package Type: 8P

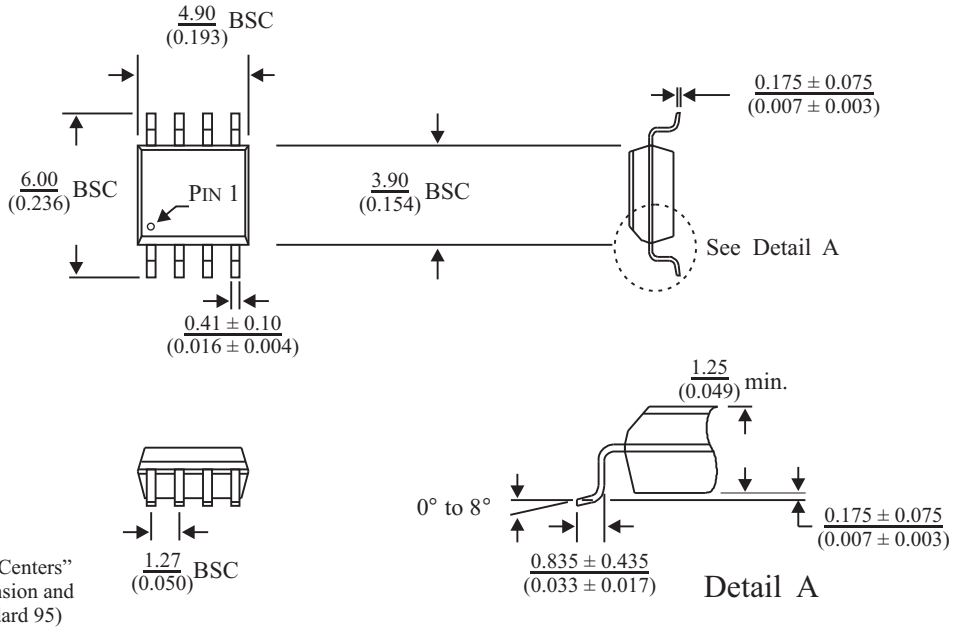


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

8-PIN PLASTIC SMALL OUTLINE (SOIC) - NB
(Narrow Body)

millimeters (inches)

Package Type: 8HN



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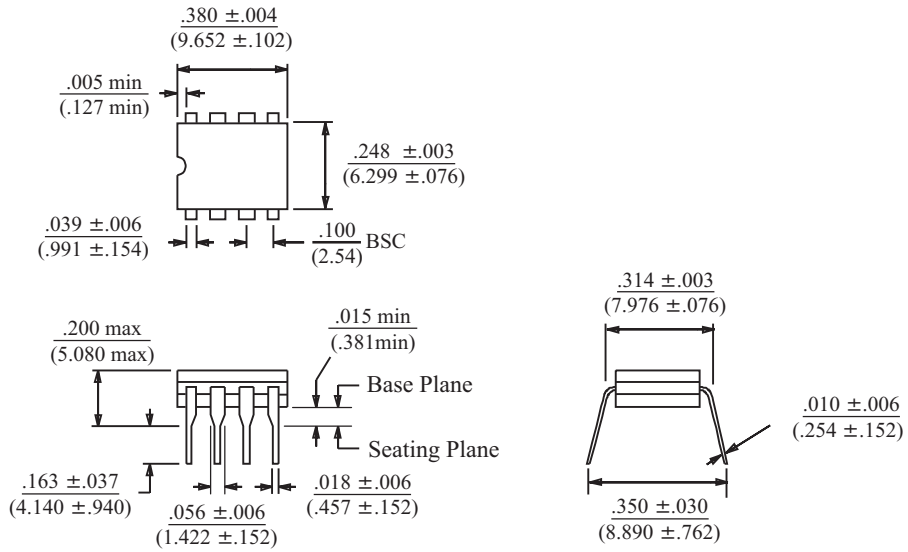
8-PIN CERDIP

inches (millimeters)

Package Type: 8D



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