HI-8425, HI-8426

8-Channel, Ground /Open, or Supply / Open Sensor
4-channel 200 mA Ground / Open Driver

March 2020

GENERAL DESCRIPTION

The HI-8425 is a combined 8-channel discrete-to-digital sensor and quad low side driver fabricated with Silicon-on-Insulator (SOI) technology for robust latch-up free operation. Sense detection can either be GND/Open or Supply/Open as configured by the SNSE_SEL pin. Supply/Open sensing is also referred to as 28V/Open sensing. The sensing circuit window comparator thresholds can be fixed at the internal programmed values or can be set externally at the HI_SET and LO_SET pins, as selected by the $\overline{\text{THS\_SEL}}$ pin. The digital SENSE outputs can be tri-stated by taking the $\overline{\text{OE}}$ pin high.

All sense inputs are internally lightning protected to DO160G, Section 22, Cat AZ, BZ and ZZ without external components.

The HI-8425 also offers four low side switches each capable of sinking 200 mA of current. Each switch transistor is controlled by its own digital input pin and is fully fault protected. Over-current conditions, such as a short circuit, are detected and inhibited while signaling the fault condition at the corresponding logic output. These four FAULT outputs are also available in a combined OR output. The outputs are fully protected from transients when driving relays.

The HI-8426 puts all of the features of the HI-8425 except the individual Fault Detection Outputs, Tri-state pin selection and fixed internal thresholds into a 32-pin Chip Scale Package (QFN) which measures only 5mm x 5mm.

Interface to the digital subsystem is simple CMOS logic inputs and outputs. The logic pins are compatible with 5V or 3.3V logic allowing direct connection to a wide range of microcontrollers or FPGAs.

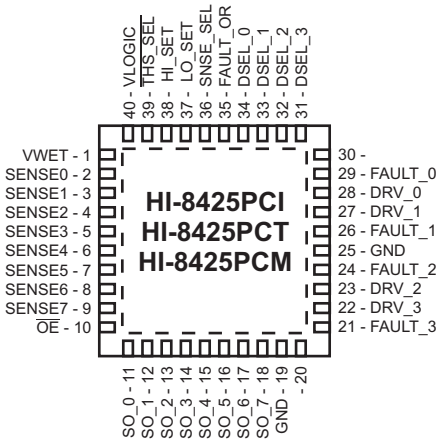
FEATURES

- Robust CMOS Silicon-on-Insulator (SOI) technology
- 8-channel Selectable Sense Operation, GND/Open or Supply/Open
- Selectable Thresholds and Hysteresis
- Sense Detection Range 3V to 22V
- Logic Operation from 3.0V to 5.5V
- Lightning Protected Sense Inputs
- Sense Inputs compliant to MIL-STD-704
- Airbus ABD0100H compliant sense inputs
- 4 Low-Side 200 mA drivers
- 4.5 Ohm On Resistance
- Over-Current Fault Detection Signaled by Logic Output
- Max Power Dissipation Automatically Limited by Fault Protection
- Diode Clamps for Discharging Inductive Loads

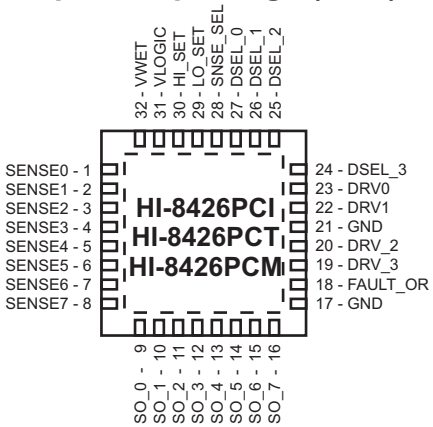
APPLICATIONS

- Avionics Discrete to Digital Sensing
- Relay Driver
- Lamp driver
- Discrete Signaling

PIN CONFIGURATIONS



40 Pin Plastic 6mm x 6mm Chip-scale package (QFN)



32 Pin Plastic 5mm x 5mm Chip-scale package (QFN)

(See page 16 for leaded QFP package options)

BLOCK DIAGRAM

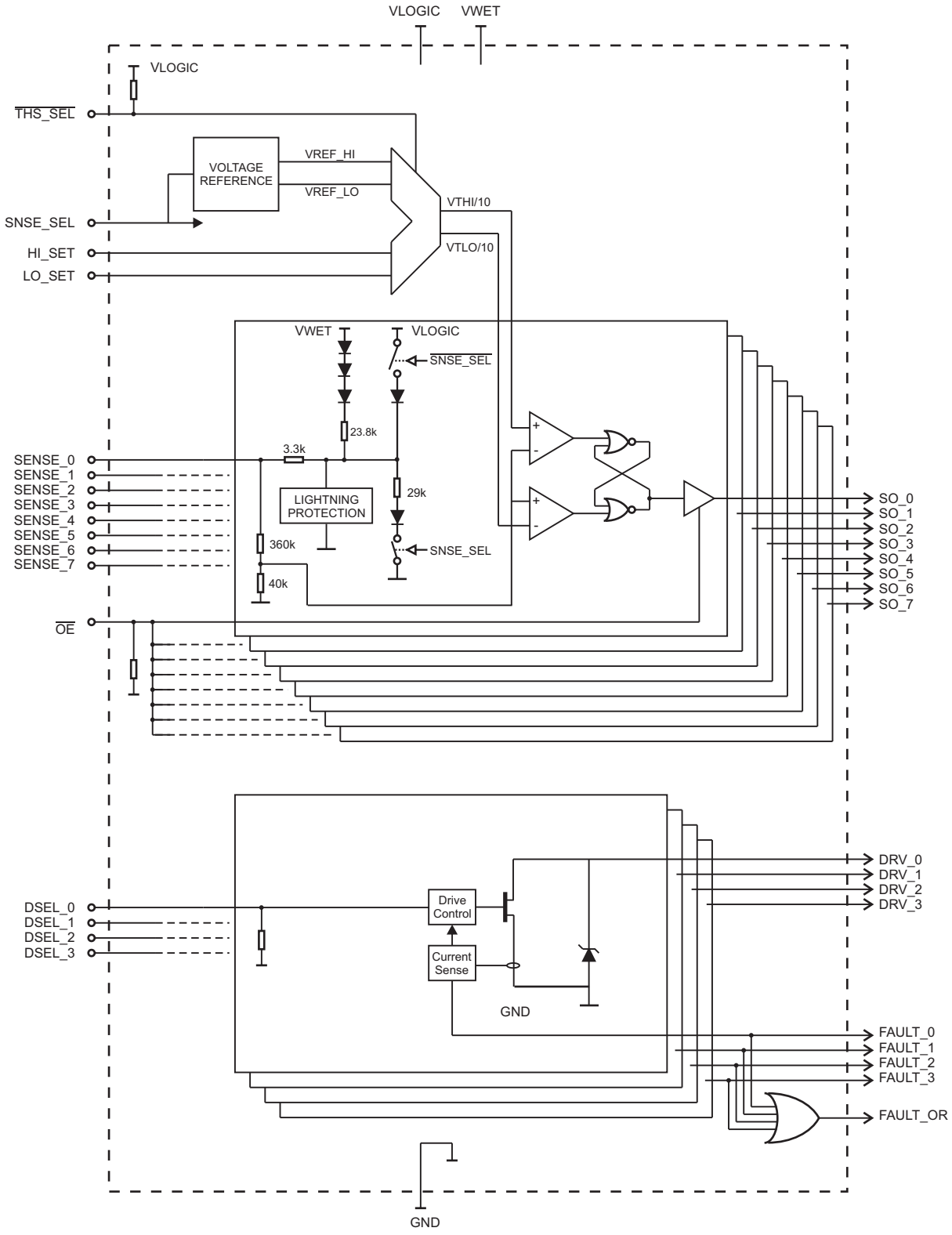


Figure 2

PIN DESCRIPTIONS

SYMBOL	FUNCTION	DESCRIPTION
VWET	Supply	Optional input to supply relay wetting current to sense lines in GND/Open operation 50kΩ to GND
SENSE0	Discrete Input	Discrete input 0. If SNSE_SEL = 0 pin senses GND/Open. If SNSE_SEL = 1, senses SUPPLY/Open
SENSE1	Discrete Input	Discrete input 1. If SNSE_SEL = 0 pin senses GND/Open. If SNSE_SEL = 1, senses SUPPLY/Open
SENSE2	Discrete Input	Discrete input 2. If SNSE_SEL = 0 pin senses GND/Open. If SNSE_SEL = 1, senses SUPPLY/Open
SENSE3	Discrete Input	Discrete input 3. If SNSE_SEL = 0 pin senses GND/Open. If SNSE_SEL = 1, senses SUPPLY/Open
SENSE4	Discrete Input	Discrete input 4. If SNSE_SEL = 0 pin senses GND/Open. If SNSE_SEL = 1, senses SUPPLY/Open
SENSE5	Discrete Input	Discrete input 5. If SNSE_SEL = 0 pin senses GND/Open. If SNSE_SEL = 1, senses SUPPLY/Open
SENSE6	Discrete Input	Discrete input 6. If SNSE_SEL = 0 pin senses GND/Open. If SNSE_SEL = 1, senses SUPPLY/Open
SENSE7	Discrete Input	Discrete input 7. If SNSE_SEL = 0 pin senses GND/Open. If SNSE_SEL = 1, senses SUPPLY/Open
$\overline{OE}$	Digital Input	If High, SO_n and fault outputs are high-impedance. $\overline{OE}$ has internal 30kΩ pull-down resistor
SO_0	Digital output	High if SNSE_SEL=0 and SENSE0 < V_{LO}, or Low if SNSE_SEL=1 and SENSE0 > V_{HI}
SO_1	Digital output	High if SNSE_SEL=0 and SENSE1 < V_{LO}, or Low if SNSE_SEL=1 and SENSE1 > V_{HI}
SO_2	Digital output	High if SNSE_SEL=0 and SENSE2 < V_{LO}, or Low if SNSE_SEL=1 and SENSE2 > V_{HI}
SO_3	Digital output	High if SNSE_SEL=0 and SENSE3 < V_{LO}, or Low if SNSE_SEL=1 and SENSE3 > V_{HI}
SO_4	Digital output	High if SNSE_SEL=0 and SENSE4 < V_{LO}, or Low if SNSE_SEL=1 and SENSE4 > V_{HI}
SO_5	Digital output	High if SNSE_SEL=0 and SENSE5 < V_{LO}, or Low if SNSE_SEL=1 and SENSE5 > V_{HI}
SO_6	Digital output	High if SNSE_SEL=0 and SENSE6 < V_{LO}, or Low if SNSE_SEL=1 and SENSE6 > V_{HI}
SO_7	Digital output	High if SNSE_SEL=0 and SENSE7 < V_{LO}, or Low if SNSE_SEL=1 and SENSE7 > V_{HI}
FAULT_3	Digital output	High if Driver 3 is attempting to sink excess current
DRV_3	Switch Output	Drain node of Ground switch driver 3
GND	Supply	Ground for logic and Analog Ground return for DRV0-3. GND pin and the isolated backside pad should be grounded for optimum performance and power dissipation.
DRV_2	Switch Output	Drain node of Ground switch driver 2
FAULT_2	Digital output	High if Driver 2 is attempting to sink excess current
FAULT_1	Digital output	High if Driver 1 is attempting to sink excess current
DRV_1	Switch Output	Drain node of Ground switch driver 1
DRV_0	Switch Output	Drain node of Ground switch driver 0
FAULT_0	Digital output	High if Driver 0 is attempting to sink excess current
DSEL_3	Digital Input	When high, turns on Driver 3. DSEL_3 has an internal 30kΩ pull-down resistor
DSEL_2	Digital Input	When high, turns on Driver 2. DSEL_2 has an internal 30kΩ pull-down resistor
DSEL_1	Digital Input	When high, turns on Driver 1. DSEL_1 has an internal 30kΩ pull-down resistor
DSEL_0	Digital Input	When high, turns on Driver 0. DSEL_0 has an internal 30kΩ pull-down resistor
FAULT_OR	Digital Output	High if any Driver is attempting to sink excess current
SNSE_SEL	Digital Input	If Low, SENSE pins are sensing Open/Gnd. If High, SENSE pins sense SUPPLY/Open
LO_SET	Analog input	If $\overline{THS\_SEL}$ is High, this pin sets the lower window comparator threshold
HI_SET	Analog input	If $\overline{THS\_SEL}$ is High, this pin sets the upper window comparator threshold
$\overline{THS\_SEL}$	Digital Input	If $\overline{THS\_SEL}$ is Low, comparator thresholds are set internally. $\overline{THS\_SEL}$ has an internal 30kΩ pull-up
VLOGIC	Supply	Logic supply. (3.0V - 5.5V)

FUNCTIONAL DESCRIPTION

SENSING

The 8 Sense Channels can be configured to meet the requirements of a variety of conditions and applications. Table 1 summarizes basic function selection and Table 2 gives more details on possible threshold values.

GND/OPEN SENSING

For GND/Open sensing, the SNS_SEL pin is connected to GND. Referring to the Block Diagram, Figure 2, this selection will connect a 3.3kΩ pull-up resistor through a diode to VLOGIC and a 23.8kΩ resistor through 3 diodes to VWET. These resistors give extra noise immunity for detecting the open state while providing relay wetting current. Configuring $\overline{\text{THS\_SEL}}$, HI_SET/LO_SEL and VWET as described below sets the window comparator thresholds, V_{THI} and V_{TLO}, the open input voltage when open, and the input current.

HI-8425 (40 pin version) - THRESHOLD SELECT

The HI-8425 offers a choice between internally fixed thresholds or external thresholds provided by the user.
With $\overline{\text{THS\_SEL}}$ set to GND, the window comparator thresholds are fixed based on an internal reference. The high threshold, V_{THI}, and the low threshold, V_{THLO} levels may be found in Table 2. When the internal references are used the HI_SET and LO_SET pins should be connected to GND.
For applications with either large GND offsets or thresholds higher than VLOGIC - 0.75V, $\overline{\text{THS\_SEL}}$ is set high and the thresholds are set externally, for example by a simple resistor divider off the VLOGIC supply. In this case V_{THI} is equal to 10X the voltage on the HI_SET pin. V_{TLO} is equal to 10X the voltage on the LO_SET pin. This mode allows the user complete flexibility to define the thresholds and hysteresis levels.

HI-8426 (32 pin version) THRESHOLD SELECT

For applications that can take advantage of the very small 32 pin chip scale package of the HI-8426, $\overline{\text{THS\_SEL}}$ is not available and an internal pull-up makes it mandatory to supply HI_SET and LO_SET externally.

OPEN INPUT VOLTAGE

For correct operation, the V_{SENSE_n} when open, must be higher than V_{THI} so SO_n will be low. This condition requires VWET to be set greater than (VTHI/0.9 + 2.25V). Various ARINC standards such as ARINC 763 define the standard “Open” signal as characterized by a resistance of 100kΩ or more with respect to signal common. The user should consider this 100kΩ to ground case when setting the thresholds.

WETTING CURRENT

For GND/Open applications with VWET open, the wetting current with the input voltage at GND is simply (VLOGIC - 0.75)/3.3k. When applying a higher voltage at the VWET pin the wetting current is (VLOGIC - 0.75)/3.3k + (VWET - 4.2)/127k. Additional wetting current can be achieved by placing an external resistor and a diode between VWET and the individual sense inputs.

SUPPLY/OPEN SENSING

The 8 Sense Channels can be configured to sense Supply/Open by connecting the SNSE_SEL pin to VLOGIC. Refering to Figure 2, a 32kΩ resistor is switched in series to provide a pull down in addition to the 400kΩ of the comparator input divider to GND. Similar to the GND/Open case configuring $\overline{\text{THS\_SEL}}$, HI_SET/LO_SEL and VWET as described below sets the window comparator thresholds, the open input voltage when open and the wetting current.

THRESHOLD SELECT

The threshold selections are handled in the same way as stated above for the GND/OPEN case.
For $\overline{\text{THS\_SEL}}$ set low, the internal reference nominally sets the window comparator. See table 2 for the V_{THI} and V_{THLO} threshold levels.
For $\overline{\text{THS\_SEL}}$ set high, the final thresholds are 10X the voltage set on the HI_SET and LO_SET pins. The VWET pin must be left open in the Supply/Open sensing case.

WETTING CURRENT

For the Supply/Open case the wetting current into the sense input is the current sunk by the effective 28kΩ to GND. For V_{SENSE_n} = 28V, I_{WET} is 1ma. See Figure 12.

Table 1. Function Table

SENSE_n	SNSE_SEL	$\overline{\text{OE}}$	SO_n
Open or > VTHI	L (GND/OPEN)	L	L
< VTLO	L (GND/OPEN)	L	H
X	L (GND/OPEN)	H	Z
Open or < VTLO	H (V+/OPEN)	L	H
> VTHI	H (V+/OPEN)	L	L
X	H (V+/OPEN)	H	Z

H = VLOGIC, L = GND, Z = Hi-Z, X = Don’t Care, V+ = V_{SUPPLY}
See Table 2 for values of VTHI/VTLO

FUNCTIONAL DESCRIPTION

Table 2. Configuration options and allowed threshold values -55C to 125C.

VLOGIC	VWET Pin	SNSE_ SEL	$\overline{\text{THS\_}}$ $\overline{\text{SEL}}$	Operation	Threshold Selected	Maximum HI_SET (VTHI = HI_SETx10)	Minimum LO_SET (VTLO = LO_SETx10)	Guaranteed High Threshold	Guaranteed Low Threshold
3.0V	OPEN	L	L	GND/OPEN	Internal	-	-	2.5V	1.0V
3.6V	OPEN	L	L	GND/OPEN	Internal	-	-	2.7V	1.0V
3.3V	28V	L	L	GND/OPEN	Internal	-	-	2.55V	1.0V
3.0V	7V	L	H	GND/OPEN	External	0.4V (4.0V)	0.3V (3.0V)	VTHI + 0.5V	VTLO - 0.5V
3.6V	7V	L	H	GND/OPEN	External	0.4V (4.0V)	0.3V (3.0V)	VTHI + 0.5V	VTLO - 0.5V
3.0V to 3.6V	28V	L	H	GND/OPEN	External	2.2V (22V)	0.3V (3.0V)	VTHI + 0.5V	VTLO - 0.5V
3.0V to 3.6V	OPEN	H	L	V+/OPEN	Internal	-	-	15.5V	11.0V
3.0V to 3.6V	OPEN	H	H	V+/OPEN	External	2.2V (22V)	0.3V (3.0V)	VTHI + 0.5V	VTLO - 0.5V
4.5V	OPEN	L	L	GND/OPEN	Internal	-	-	3.25V	1.0V
5.5V	OPEN	L	L	GND/OPEN	Internal	-	-	3.75V	1.0V
5.0V	28V	L	L	GND/OPEN	Internal	-	-	3.5V	1.0V
4.5V	7V	L	H	GND/OPEN	External	0.4V (4.0V)	0.3V (3.0V)	VTHI + 0.5V	VTLO - 0.5V
5.5V	7V	L	H	GND/OPEN	External	0.4V (4.0V)	0.3V (3.0V)	VTHI + 0.5V	VTLO - 0.5V
4.5V to 5.5V	28V	L	H	GND/OPEN	External	2.2V (22V)	0.3V (3.0V)	VTHI + 0.5V	VTLO - 0.5V
4.5V to 5.5V	OPEN	H	L	V+/OPEN	Internal	-	-	15.5V	11.0V
4.5V to 5.5V	OPEN	H	H	V+/OPEN	External	2.2V (22V)	0.3V (3.0V)	VTHI + 0.5V	VTLO - 0.5V

NOTE: VTHI = Sense pin high threshold (HI_SET x 10), VTLO = Sense pin low threshold (LO_SET x 10)

OUTPUT ENABLE

The output enable pin, $\overline{\text{OE}}$, available on the HI-8425, tri-states all Sense Outputs and Low Side Driver Fault Outputs to allow connecting the tri-state outputs in parallel with other tri-stated chips. The $\overline{\text{OE}}$ pin has a pull-down and when left open will cause these digital outputs to be driven to their logic levels. If the $\overline{\text{OE}}$ pin is High, these digital outputs are high impedance.

OUTPUT DRIVERS

LOW SIDE DRIVERS

Both product versions offer four Low Side Drivers. Each driver (NMOS switch) is capable of sinking a minimum of 200mA while exhibiting a R_{on} of 4.5Ω typical. Each output has diode clamps for protection during inductive kick-back for relay applications. Off-state leakage is typically less than 10nA at room temperature. The inputs, DSEL0 through DSEL3, have internal pull-downs which hold off the drivers until logic highs are presented.

OVER-CURRENT SHUTDOWN

Maximum DC power dissipation per driver is approximately 0.5W at room temperature. Conditions that would cause the power to exceed this amount will result in a shut down of the driver. Over-current shutdown is initiated when the driver pin voltage is more than approximately 1.5V from GND. However there is a delay of approximately 11µsec before the shutdown actually occurs giving the driver an opportunity to charge capacitive loads and thereby avoid shutdown. Similarly, if the driver is on and a high load is suddenly switched on, the over-current shutdown will be delayed in activation. Note that even when the over-current fault condition is present, the driver pin is still sinking a few milliamps. This low current condition continues until the input is taken low or the load is removed.

FAULT CONDITIONS

Each driver has a converter that translates an over-current detection into a logic high output at its FAULT output. The FAULT_OR output goes high if one or more FAULT outputs are high. These outputs can be tri-stated by setting $\overline{\text{OE}}$ high.

FUNCTIONAL DESCRIPTION

LIGHTNING PROTECTION

All SENSE_n inputs are protected to RTCA/DO-160G, Section 22, Categories AZ and BZ, Waveforms 3, 4, 5A. In addition, all inputs are also protected to ZZ, Waveforms 3 and 5B, to provide more robustness in composite airframe applications. Table 3 and Figure 3 give values and waveforms. See Application Note AN-305 for recommendations on lightning protection of Holt's family of Discrete-to-Digital devices.

Level	Waveforms			
	3/3	4/1	5A/5A	5B/5B
	Voc (V) / Isc (A)	Voc (V) / Isc (A)	Voc (V) / Isc (A)	Voc (V) / Isc (A)
2	250/10	125/25	125/125	125/125
Z	500/20	300/60	300/300	300/300
3	600/24	300/60	300/300	300/300

Table 3. Waveform Peak Amplitudes

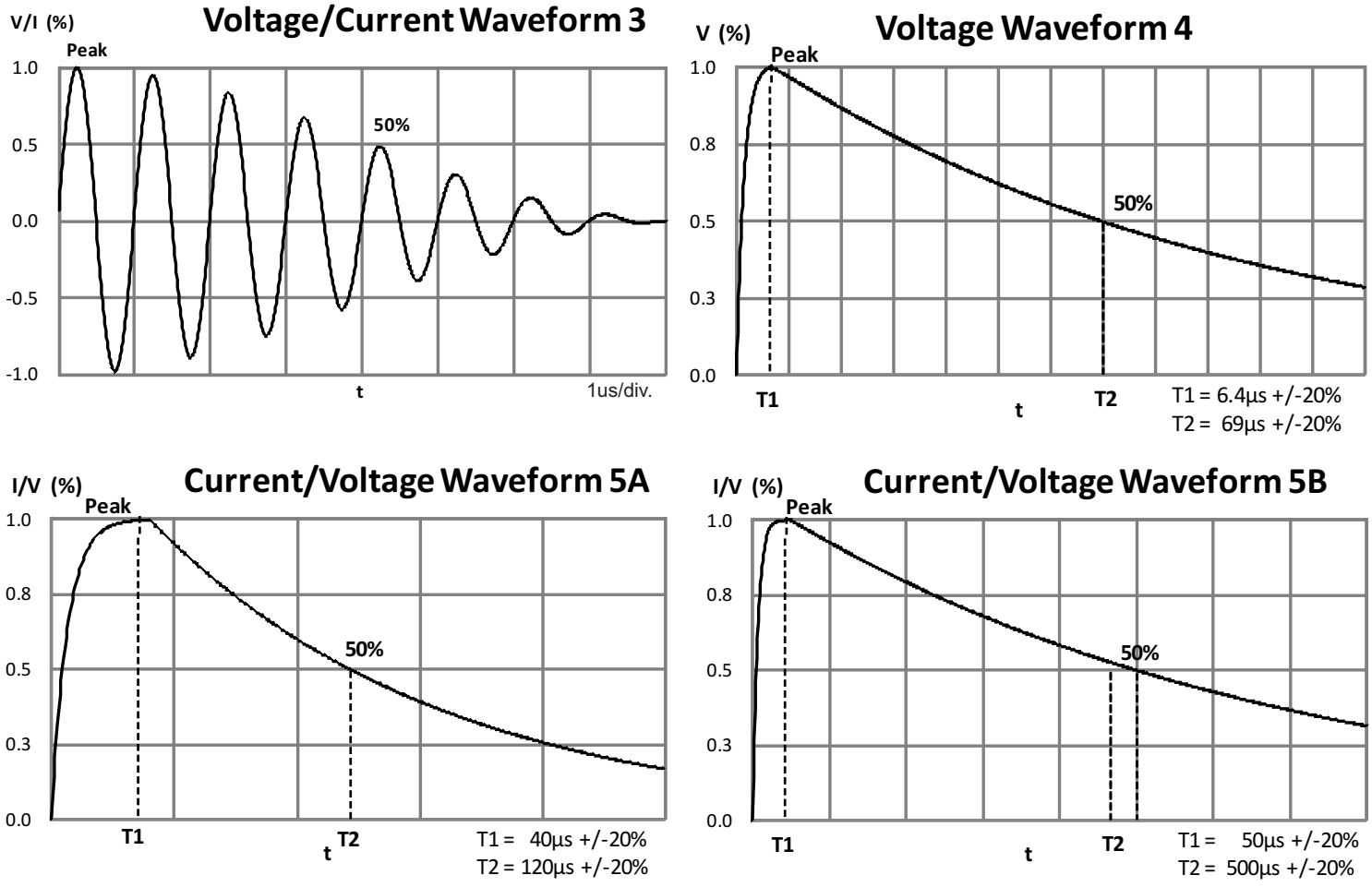


Figure 3. Lightning Waveforms

APPLICATION EXAMPLES

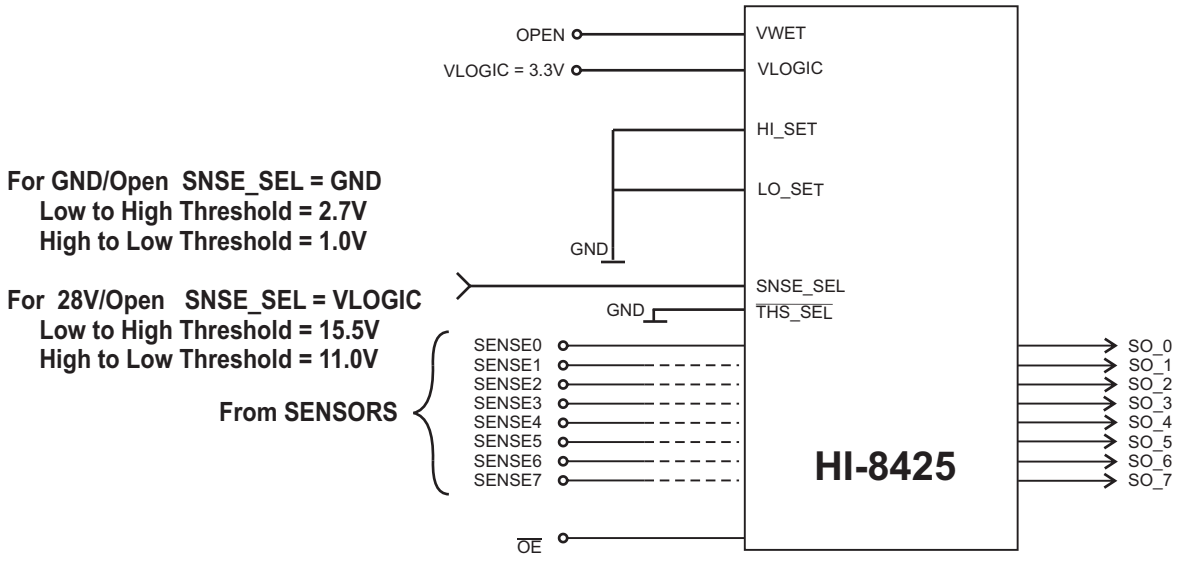


Figure 4 Input Sensing with Internal Thresholds

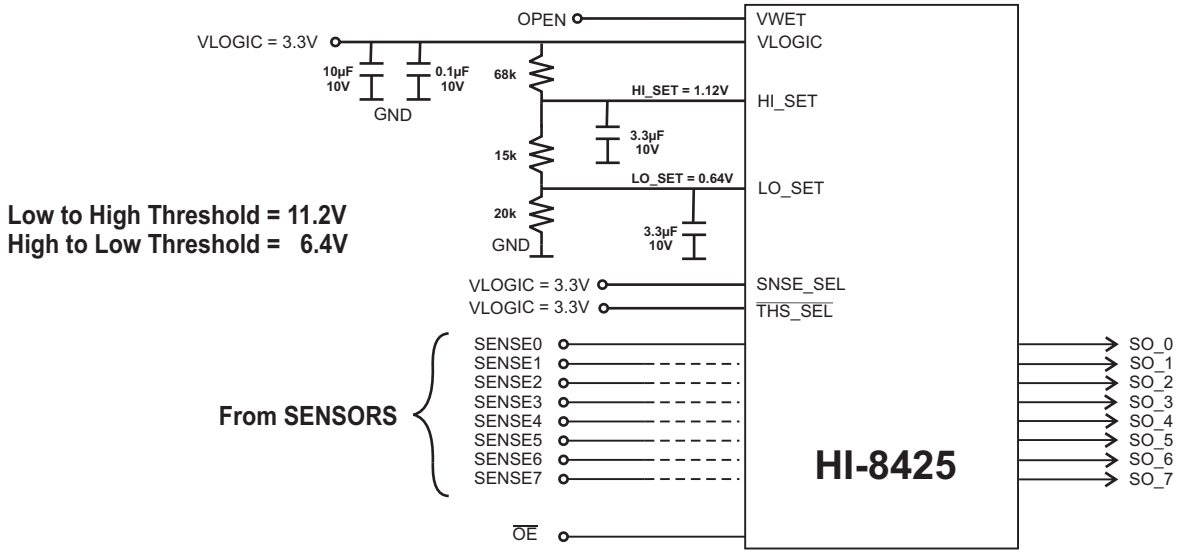


Figure 5 Input Sensing, 28V/OPEN, Typical ABD0100H Thresholds

APPLICATION EXAMPLES

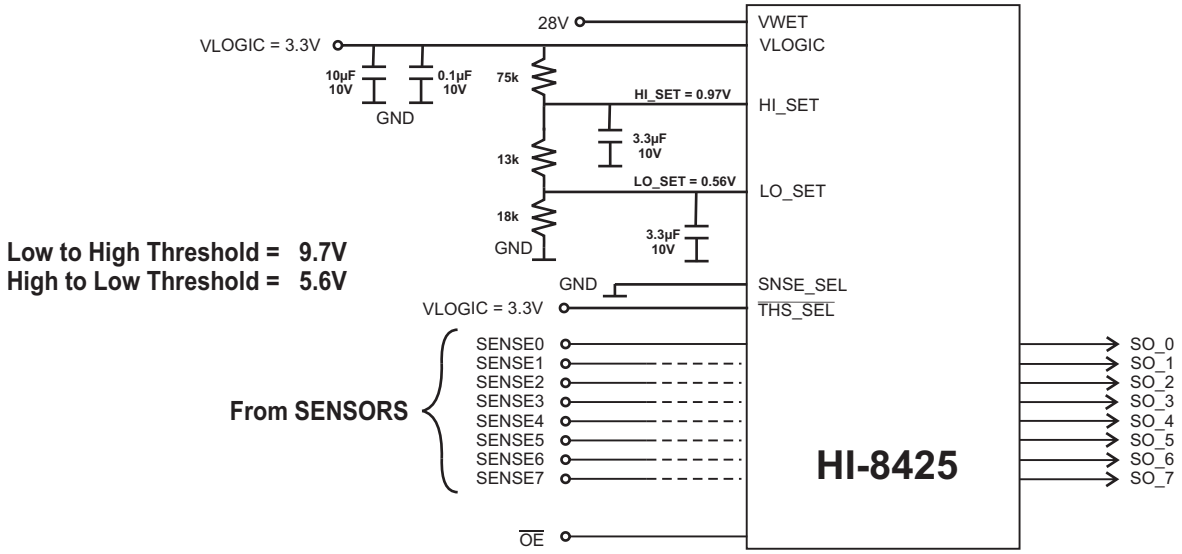


Figure 6 Input Sensing, GND/OPEN Typical ABD0100H Thresholds, 1ma wetting current

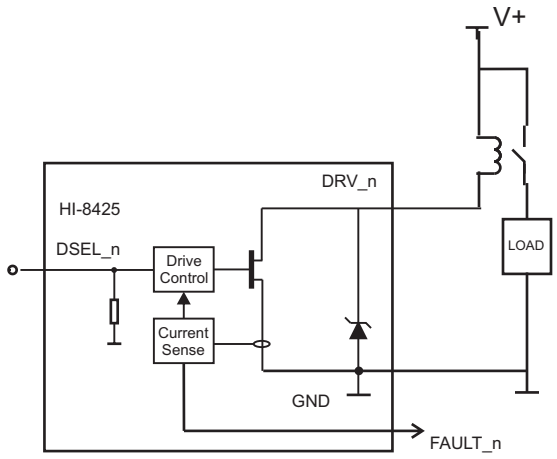


Figure 7 Lowside Output Driving Relay

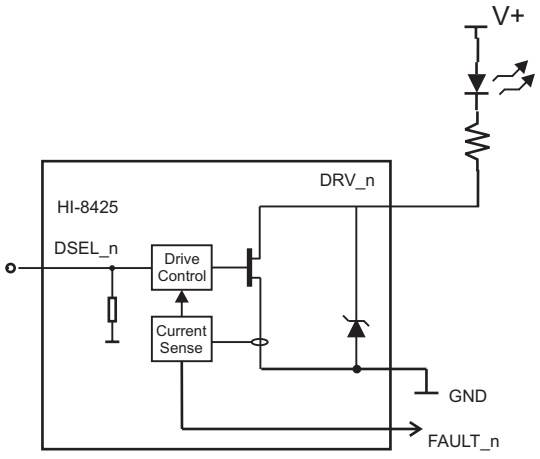


Figure 8 Lowside Output Driving LED

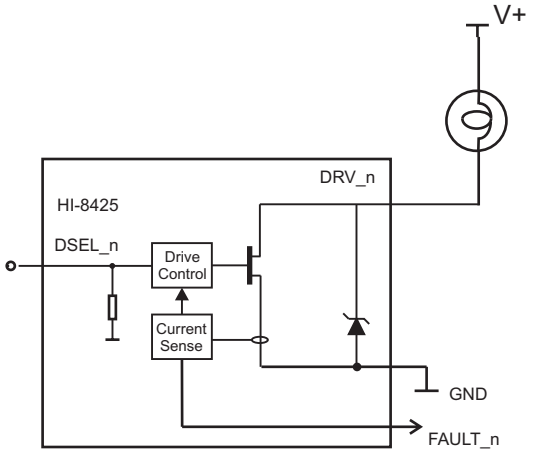


Figure 9 Lowside Output Driving Lamp

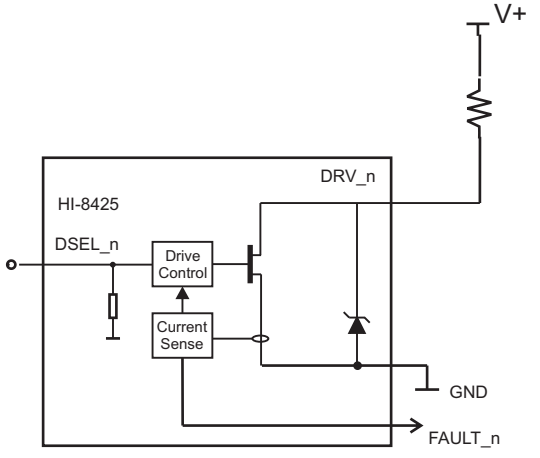


Figure 10 Lowside Output Driving Resistive Load

APPLICATION EXAMPLES

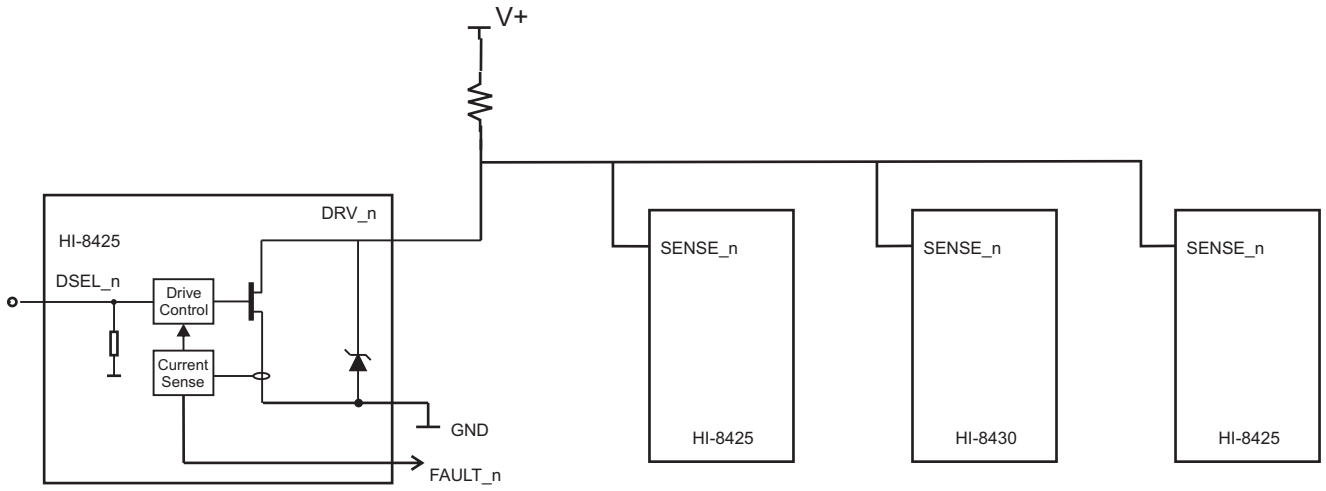


Figure 11 Lowside Output Used for Discrete Signaling with three separate users

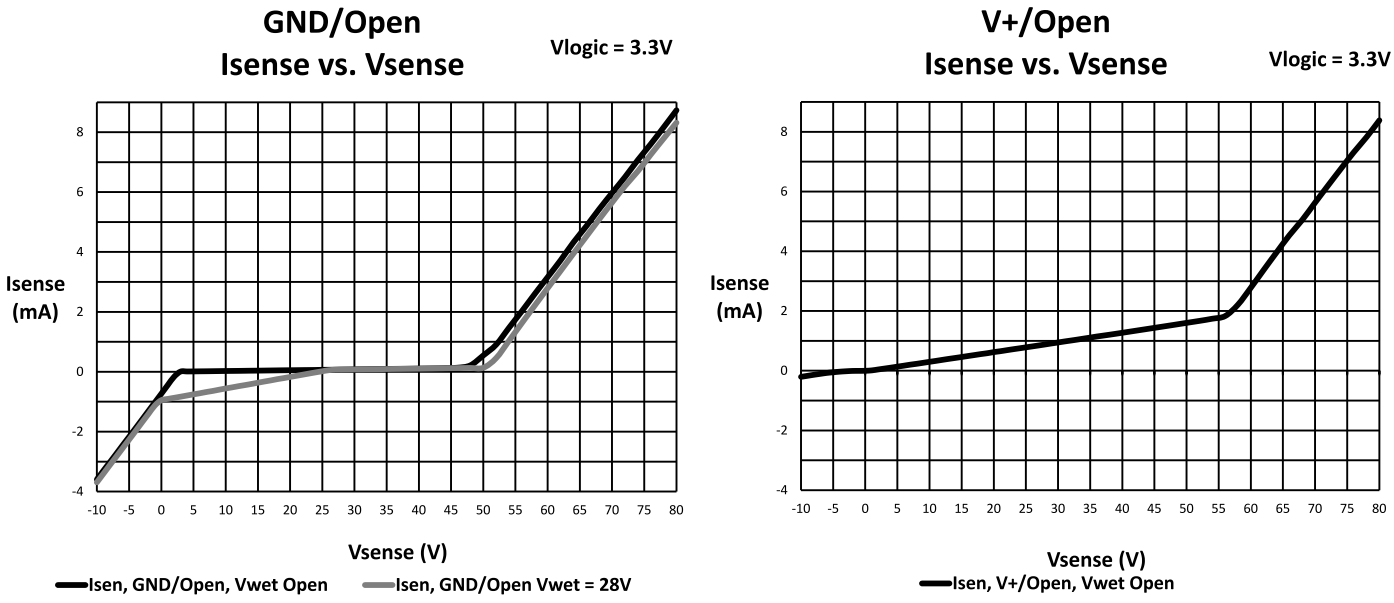


Figure 12 Input Current Vs. Input Voltage

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to Ground	
Supply Voltage (VLOGIC)	-0.3V to +7V
DRV_n	55V
VWET	-0.3V to +55V
DC Driver Current per pin	300mA
Logic Input Voltage Range	-0.3V to VLOGIC+0.3V
Discrete Input Voltage Range	-80V to +80V
Continuous Power Dissipation (TA=+70°C) QFN (derate 21.3mW/°C above +70°C) QFP (derate 10.0mW/°C above +70°C)	 1.7W 1.5W
Solder Temperature (reflow)	260°C
Junction Temperature	175°C
Storage Temperature	-65°C to -150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	
VLOGIC	3.0V to 5.5V
VWET	7.0V to 36V
Operating Temperature Range	
Industrial Screening	-40°C to +85°C
Hi-Temp Screening	-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

D.C. ELECTRICAL CHARACTERISTICS

VDD = 3.3V or 5V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
DISCRETE INPUTS						
SENSE V+/OPEN		SEN_SEL = High, VWET floating				
Resistance to Ground	R_{IN}			30		kΩ
Case 1: $\overline{\text{THS\_SEL}}$ = GND		Internal Threshold Mode				
Open State Input Voltage	V_{OS}	Input voltage to give High output			11.0	V
V+ State Input Voltage	V_{V+}	Input voltage to give Low output	15.5			V
Input Current at 28V	I_{IN28}	V_{IN} = 28V		0.95		mA
Hysteresis	V_{HY}		1.5			V
Case 2: $\overline{\text{THS\_SEL}}$ = Open or VLOGIC		HI_SET/LO_SET pin set Thresholds				
HI_SET Threshold Range	V_{THI}	HI Threshold is set to HI_SET X 10	0.4		2.2	V
LO_SET Threshold Range	V_{TLO}	LO Threshold is set to LO_SET X 10	0.3		2.1	V
Min Threshold Window	V_{THW}	HI_SET > LO_SET	0.1			V
Sense Threshold Accuracy		Voltage referred to the sense input, see table 2	V_{TLO} - 0.5		V_{THI} + 0.5	V

D.C. ELECTRICAL CHARACTERISTICS (cont)

VDD = 3.3V or 5V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
DISCRETE INPUTS						
SENSE GND/OPEN						
Resistance in series with diode to VLOGIC	R_{IN}			3.3		kΩ
Resistance in series with diode to VWET	R_W			23.8		kΩ
Case 1: $\overline{THS\_SEL}$ = GND		Internal Threshold Mode				
Ground State Input Voltage	V_{GS}	Input voltage to give High output			1.0	V
Open State Input Voltage	V_{OS}	Input voltage to give Low output VDD = 5.5V VDD = 3.0V	 3.75 2.5			V
Input Current at 0V	I_{IN28}	V_{IN} = 0V, VDD = 3.0V V_{IN} = 0V, VDD = 5.5V		-0.65 -1.65		mA mA
Hysteresis	V_{HY}		0.15			V
Case 2: $\overline{THS\_SEL}$ = Open or VLOGIC		HI_SET/LO_SET pins set Thresholds				
HI_SET Threshold Range	V_{THI}	HI Threshold is set to HI_SET X 10	0.4		2.2	V
LO_SET Threshold Range	V_{TLO}	LO Threshold is set to LO_SET X 10	0.3		2.1	V
Min Threshold Window	V_{THW}	HI_SET > LO_SET	0.1			V
Sense Threshold Accuracy		Voltage referred to the sense input, see table 2	V_{TLO} - 0.5		V_{THI} + 0.5	V

LOGIC INPUTS						
Input Voltage	V_{IH}	Input Voltage HI	80%			VLOGIC
	V_{IL}	Input Votage LO			20%	VLOGIC
Input Current, $\overline{OE}$, DSEL_n	I_{SINK}	V_{IN} = VLOGIC, 30kΩ pull down		125		µA
	I_{SOURCE}	V_{IN} = GND			0.1	µA
Input Current, $\overline{THS\_SEL}$	I_{SINK}	V_{IN} = VLOGIC	0.1			µA
	I_{SOURCE}	V_{IN} = GND , 30kΩ pull up		125		µA
Input Current, SNSE_SEL	I_{SINK}	V_{IN} = VLOGIC	0.1			µA
	I_{SOURCE}	V_{IN} = GND,	0.1			µA

D.C. ELECTRICAL CHARACTERISTICS (cont)

VDD = 3.3V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

LOGIC OUTPUTS						
Output Voltage	V_{OH}	I_{OH} = -100µA	90%			VLOGIC
	V_{OL}	I_{OL} = 100µA			10%	VLOGIC
Output Current	I_{OL}	V_{OUT}= 0.4V	1.6			mA
	I_{OH}	V_{OUT} = V_{LOGIC} - 0.4V			-1.0	mA
Tri-State Leakage Current	I_{TSL}	V_{LOGIC} > V_{out} > GND	-1.0		1.0	µA
Output Capacitance	C_O			15		pF

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
ANALOG INPUTS						
HI_SET/LO_SET Leakage Current	I_L	Max leakage for VLOGIC > V_{input} > GND	-0.1		1.0	µA
LOW SIDE DRIVERS						
On Resistance	R_{ON}	I_{SOURCE} = 200mA See Figure 16		4.5	8	Ω
Off Resistance	R_{OFF}	DRV_n = 28V, n = 0,1,2 or 3	5.0			MΩ
Over Current Threshold	V_{DCMAX}	Maximum V_{DS} before current limiting. See Figure 17	1.5			V
Over Current Delay	T_{OC}	Period that Driver sinks max current. See Figure 17	5	11		µs

SUPPLY CURRENT						
VLOGIC Current	I_{DD1}	All Sense Pins Open			10	mA
VWET Current	I_{VWET}	All Sense Inputs = 0V, VWET = 28V			12	mA

AC ELECTRICAL CHARACTERISTICS

VDD = 3.3V or 5V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
SENSE V+/OPEN						
Delay, Output going High	t_{H1}	See Figure 13, $\overline{THS\_SEL}$ = GND, 25°C		1.0		µs
Delay, Output going Low	t_{L1}	See Figure 13, $\overline{THS\_SEL}$ = GND, 25°C		1.0		µs
SENSE GND/OPEN						
Delay, Output going High	t_{H2}	See Figure 14, $\overline{THS\_SEL}$ = GND, 25°C		1.0		µs
Delay, Output going Low	t_{L2}	See Figure 14, $\overline{THS\_SEL}$ = GND, 25°C		1.0		µs
TRI-STATE DELAY						
Tri-state Delay, On	t_{TSON}	See Figure 15, $\overline{THS\_SEL}$ = GND, 25°C			40	ns
Tri-state Delay, Off	t_{TSOFF}	See Figure 15, $\overline{THS\_SEL}$ = GND, 25°C			40	ns
LOW SIDE DRIVERS						
Turn On Delay, DSEL_N	t_{SON}	See Figure 16, VLOGIC = 3.3V, 25°C	400			ns
Turn Off Delay, DSEL_N	t_{SOFF}	See Figure 16, VLOGIC = 3.3V, 25°C			900	ns
Fault Output Delay, On	t_{FON}	See Figure 17, VLOGIC = 3.3V, 25°C			15	µs
Fault Output Delay, Off	t_{FOFF}	See Figure 17, VLOGIC = 3.3V, 25°C			15	µs

TEST CIRCUIT AND TIMING DIAGRAMS

Figure 13 28V/Open Output Delay

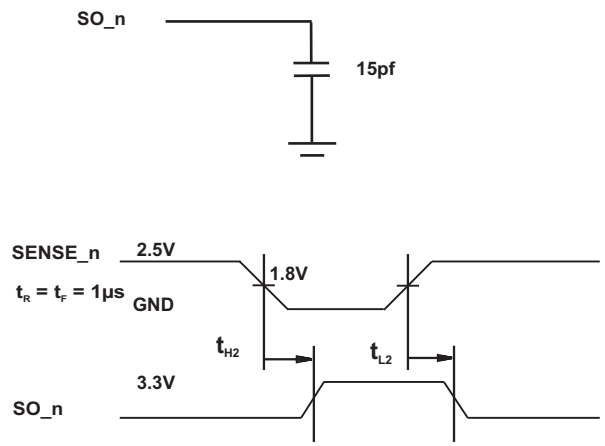


Figure 14 GND/Open Output Delay

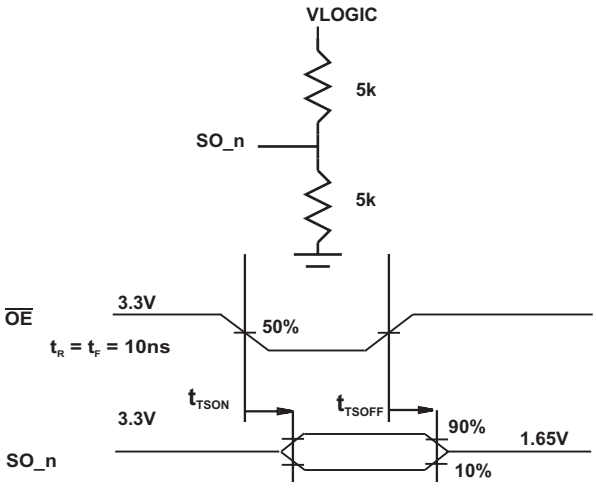


Figure 15 Sense Enable Output Delay

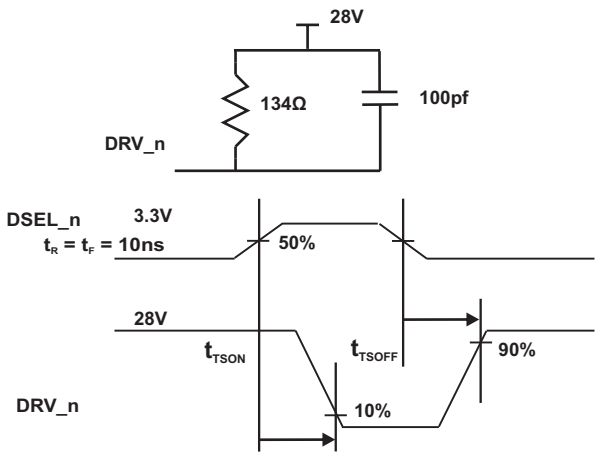


Figure 16 Low Side Driver Output Delay

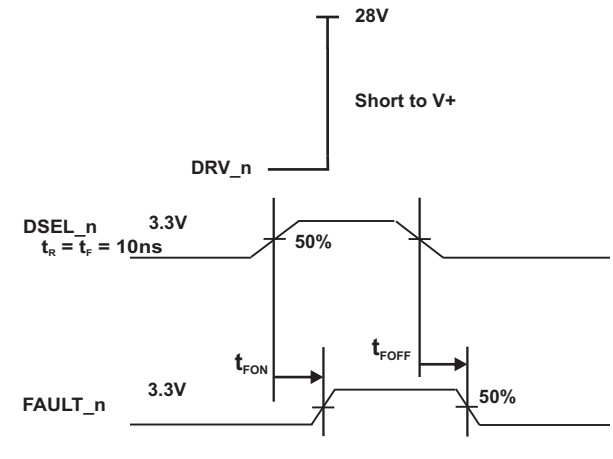


Figure 17 Low Side Driver Fault Delay

ORDERING INFORMATION

HI - 842xPQ x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn /Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO
M	-55°C TO +125°C	M	YES

PART NUMBER	PACKAGE DESCRIPTION
8425PQ	44 PIN PLASTIC QUAD FLAT PACK (44PMQS)
8426PQ	32 PIN PLASTIC QUAD FLAT PACK (32PQS)

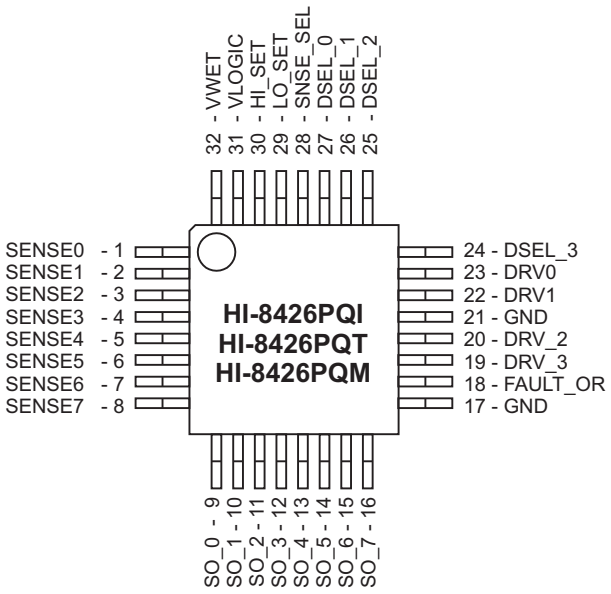
HI - 842xPC x x

PART NUMBER	LEAD FINISH
Blank	NiPdAu
F	NiPdAu (Pb-free RoHS compliant)

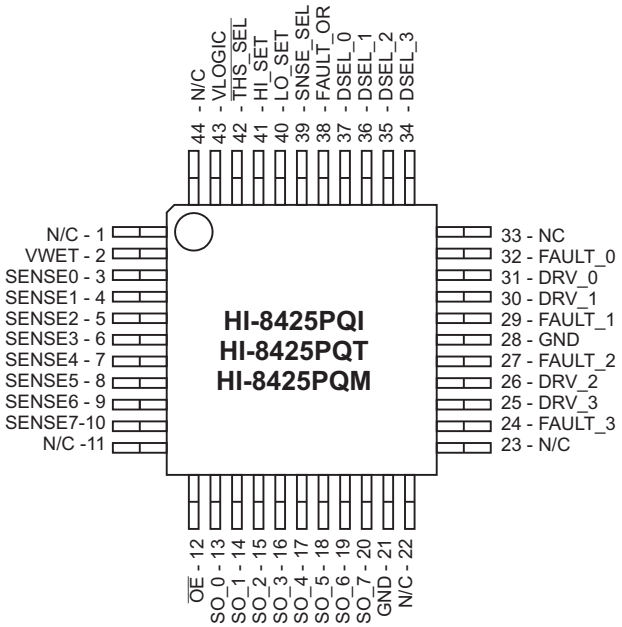
PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO
M	-55°C TO +125°C	M	YES

PART NUMBER	PACKAGE DESCRIPTION
8425PC	40 PIN PLASTIC CHIP SCALE (40PCS)
8426PC	32 PIN PLASTIC CHIP SCALE (32PCS)

ADDITIONAL PACKAGE CONFIGURATIONS



32 - Pin Plastic Quad Flat Pack (PTQFP)
7mm x 7mm body



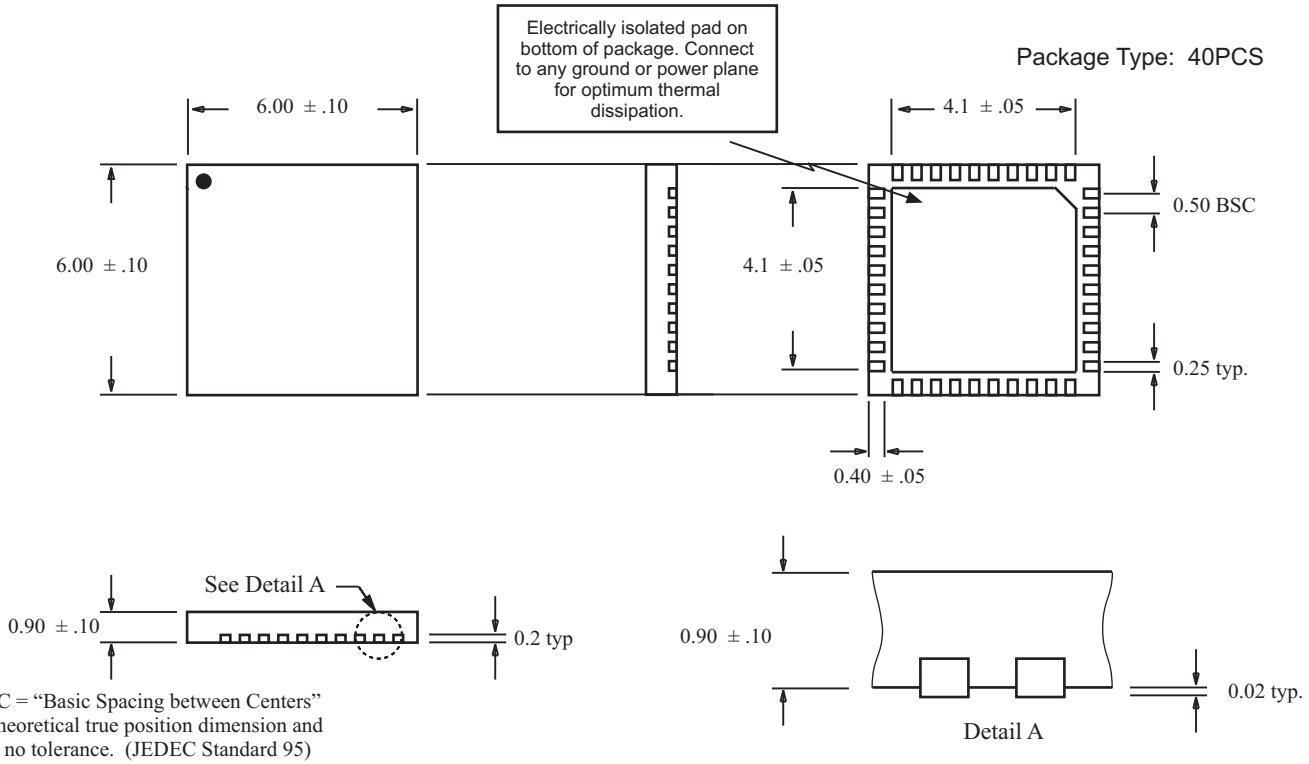
44 - Pin Plastic Quad Flat Pack (PQFP)
10mm x 10mm body

REVISION HISTORY

P/N	Rev	Date	Description of Change
DS8425	NEW	12/03/12	Initial Release
	A	03/11/13	Correct reference to pull-up resistor on inputs from 3.5k to 3.3k. Update VWET estimation formulas. Clarify VWET value for GND/Open and V+/Open sense options in DC Characteristics table. Update Figure 12 Input Current vs. Input Voltage charts. Delete Sensing Application Table. Add more detailed Table 2 instead. Updated Electrical Characteristics
	B	03/25/13	Corrected typos in internal threshold limits for V+/Open with VWET open. Was 11.5V. Should be 11.0V.
	C	08/20/13	Updated Discrete Input Voltage Range from +/-60V to +/-80V.
	D	10/23/13	Add “M-Grade” to PQFP and QFN package options. Reference AN-305 for lightning protection.
	E	02/25/15	Clarify ABD0100H compliance of sense inputs. Update QFN-32, QFP-44 and QFP-32 package drawings.
	F	11/03/15	Clarify voltage range for VWET. Clarify Sense Threshold Accuracy parameter.
	G	03/27/17	Correct Sense Threshold Accuracy from +/-25% to +/-0.5V. Correct other minor typos.
	H	02/07/18	Add MIL-STD-704 compliance statement for sense inputs.
	J	03/11/19	Change VWET max. from 20mA to 12mA. Add clarification to Lightning Protection description.
	K	09/20/19	Add parameter for OFF Resistance to DC Characteristics. Update QFN package lead finish to NiPdAu. Correct 32PCS package dimension.
	L	03/26/20	Correct typo in Over-Current Stutdown section. “sourcing” should read “sinking”.

40-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

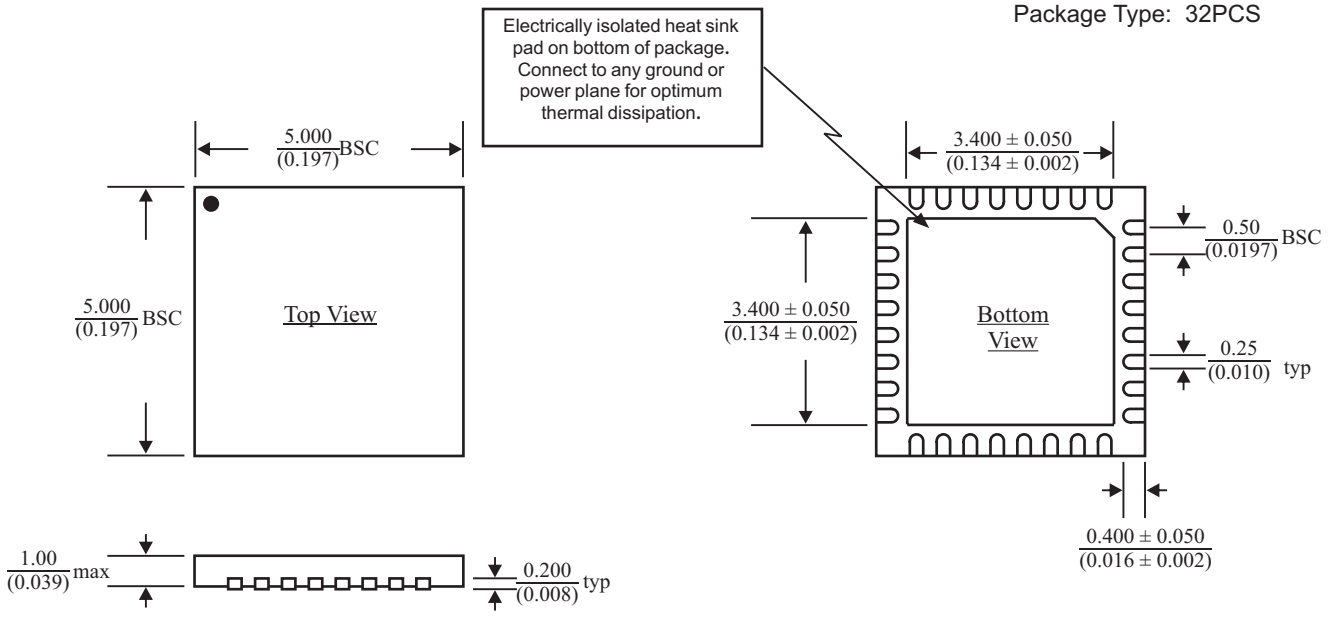
millimeters



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

32-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

millimeters (inches)

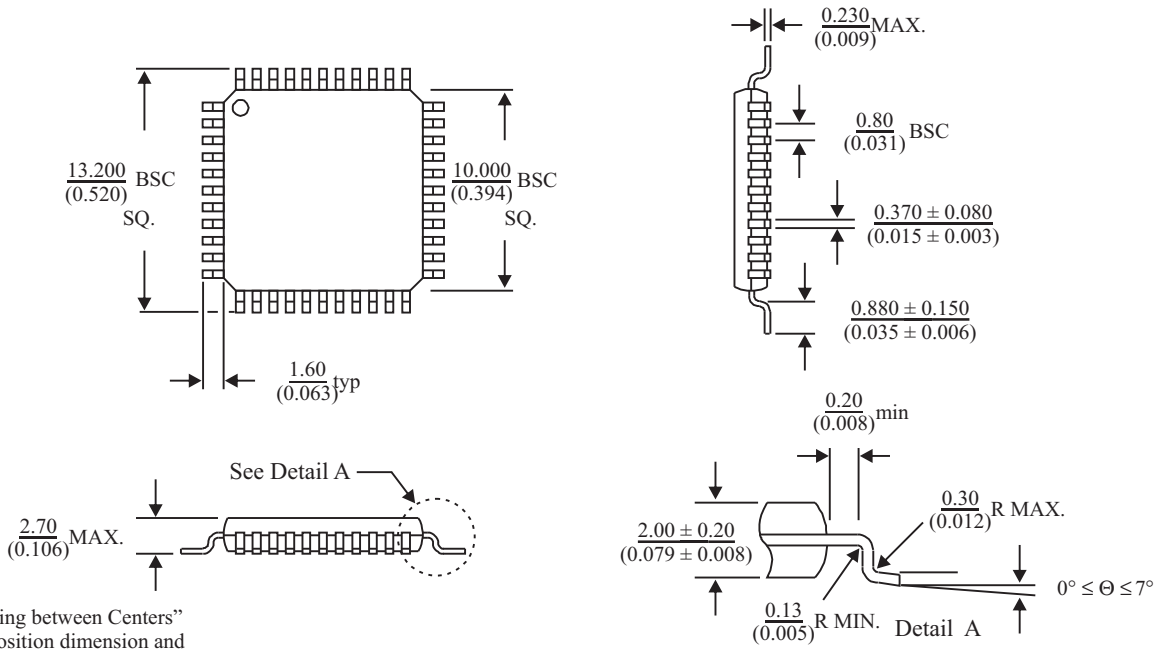


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

44-PIN PLASTIC QUAD FLAT PACK (PQFP)

millimeters (inches)

Package Type: 44PMQS

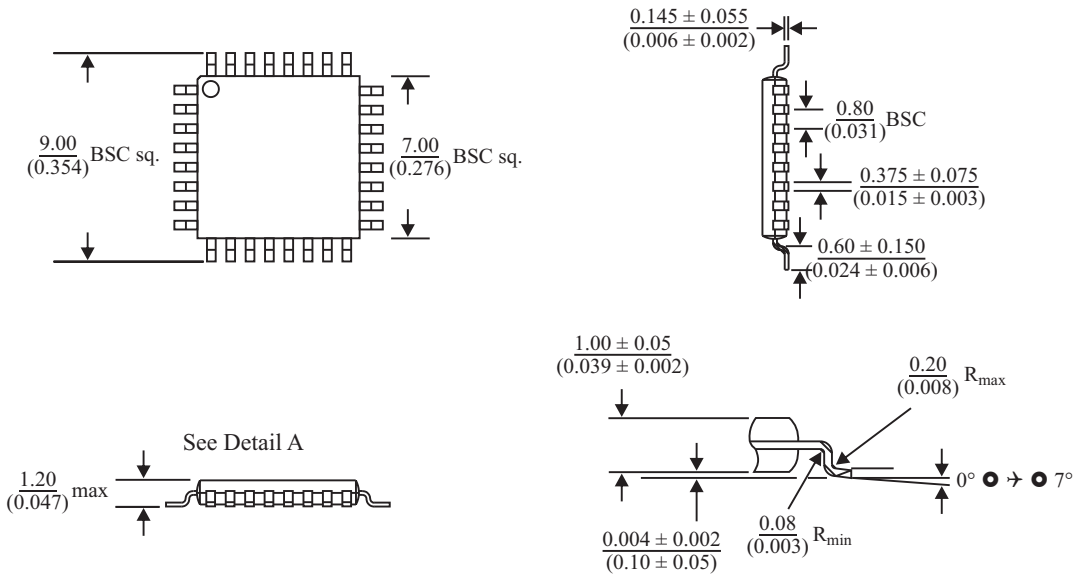


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

32 PIN PLASTIC QUAD FLAT PACK (PQFP)

millimeters (inches)

Package Type: 32PQS



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)