

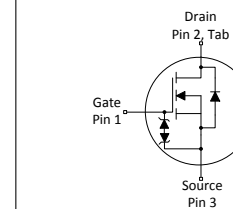
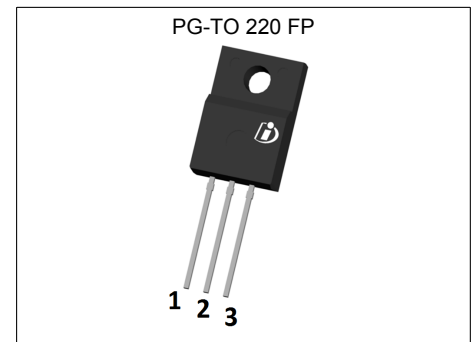
## MOSFET

### 700V CoolMOS™ P7 Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.

The latest CoolMOS™ P7 is an optimized platform tailored to target cost sensitive applications in consumer markets such as charger, adapter, lighting, TV, etc.

The new series provides all the benefits of a fast switching Superjunction MOSFET, combined with an excellent price/performance ratio and state of the art ease-of-use level. The technology meets highest efficiency standards and supports high power density, enabling customers going towards very slim designs.



### Features

- Extremely low losses due to very low FOM  $R_{DS(on)} * Q_g$  and  $R_{DS(on)} * E_{oss}$
- Excellent thermal behavior
- Integrated ESD protection diode
- Low switching losses ( $E_{oss}$ )
- Qualified for standard grade applications

### Benefits

- Cost competitive technology
- Lower temperature
- High ESD ruggedness
- Enables efficiency gains at higher switching frequencies
- Enables high power density designs and small form factors

### Applications

Recommended for Flyback topologies for example used in Chargers, Adapters, Lighting Applications, etc.

*Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.*



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_{j=25^{\circ}C}$	700	V
$R_{DS(on),max}$	0.36	$\Omega$
$Q_{g,typ}$	16.4	nC
$I_{D,pulse}$	34	A
$E_{oss} @ 400V$	1.8	$\mu J$
$V_{(GS)th,typ}$	3	V
ESD class (HBM)	2	

Type / Ordering Code	Package	Marking	Related Links
IPAN70R360P7S	PG-TO 220 FullPAK - Narrow Lead	70S360P7	see Appendix A

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## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	12.5 7.5	A	$T_C = 20^\circ\text{C}$ $T_C = 100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	34	A	$T_C=25^\circ\text{C}$
Application (Flyback) relevant avalanche current, single pulse <sup>3)</sup>	$I_{AS}$	-	-	4.5	A	measured with standard leakage inductance of transformer of $10\mu\text{H}$
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage	$V_{GS}$	-16 -30	-	16 30	V	static; AC ( $f > 1\text{ Hz}$ )
Power dissipation	$P_{tot}$	-	-	26.5	W	$T_C=25^\circ\text{C}$
Operating and storage temperature	$T_j, T_{stg}$	-40	-	150	$^\circ\text{C}$	-
Continuous diode forward current	$I_S$	-	-	5.7	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	34.0	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt <sup>4)</sup>	dv/dt	-	-	1	V/ns	$V_{DS} = 0 \dots 400\text{V}$ , $I_{SD} \leq I_S$ , $T_j=25^\circ\text{C}$
Maximum diode commutation speed <sup>4)</sup>	di/dt	-	-	50	A/ $\mu\text{s}$	$V_{DS} = 0 \dots 400\text{V}$ , $I_{SD} \leq I_S$ , $T_j=25^\circ\text{C}$
Insulation withstand voltage	$V_{ISO}$	-	-	2500	V	$V_{rms}$ , $T_C=25^\circ\text{C}$ , $t=1\text{ min}$

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction	$R_{thJC}$	-	-	4.7	$^\circ\text{C/W}$	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	80	$^\circ\text{C/W}$	leaded
Thermal resistance, junction - ambient for SMD version	$R_{thJA}$	-	-	-	$^\circ\text{C/W}$	n.a.
Soldering temperature, wavesoldering only allowed at leads	$T_{sold}$	-	-	260	$^\circ\text{C}$	1.6 mm (0.063 in.) from case for 10s

<sup>1)</sup> DPAK / IPAK equivalent. Limited by  $T_{j,max}$ .  $T_j = 20^\circ\text{C}$ . Maximum duty cycle  $D=0.5$

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Proven during verification test. For explanation please read AN - CoolMOS™ 700V P7.

<sup>4)</sup>  $V_{DClink}=400\text{V}$ ;  $V_{DS,peak} < V_{(BR)DSS}$ ; identical low side and high side switch with identical  $R_G$

### 3 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	700	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	2.50	3	3.50	V	$V_{DS}=V_{GS}, I_D=0.15mA$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu A$	$V_{DS}=700V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=700V, V_{GS}=0V, T_j=150^\circ C$
Gate-source leakage current incl. Zener diode	$I_{GSS}$	-	-	1	$\mu A$	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.30	0.36	$\Omega$	$V_{GS}=10V, I_D=3A, T_j=25^\circ C$ $V_{GS}=10V, I_D=3A, T_j=150^\circ C$
Gate resistance	$R_G$	-	30	-	$\Omega$	$f=1\text{ MHz}, \text{open drain}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	517	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Output capacitance	$C_{oss}$	-	11	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Effective output capacitance, energy related <sup>1)</sup>	$C_{o(er)}$	-	27	-	pF	$V_{GS}=0V, V_{DS}=0...400V$
Effective output capacitance, time related <sup>2)</sup>	$C_{o(tr)}$	-	329	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	19	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=2.3A, R_G=5.3\Omega$
Rise time	$t_r$	-	8	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=2.3A, R_G=5.3\Omega$
Turn-off delay time	$t_{d(off)}$	-	100	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=2.3A, R_G=5.3\Omega$
Fall time	$t_f$	-	18	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=2.3A, R_G=5.3\Omega$

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	2.3	-	nC	$V_{DD}=400V, I_D=2.3A, V_{GS}=0\text{ to }10V$
Gate to drain charge	$Q_{gd}$	-	6	-	nC	$V_{DD}=400V, I_D=2.3A, V_{GS}=0\text{ to }10V$
Gate charge total	$Q_g$	-	16.4	-	nC	$V_{DD}=400V, I_D=2.3A, V_{GS}=0\text{ to }10V$
Gate plateau voltage	$V_{plateau}$	-	4.4	-	V	$V_{DD}=400V, I_D=2.3A, V_{GS}=0\text{ to }10V$

<sup>1)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

<sup>2)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	0.9	-	V	$V_{GS}=0V, I_F=3.8A, T_j=25^{\circ}C$
Reverse recovery time	$t_{rr}$	-	210	-	ns	$V_R=400V, I_F=2.3A, di_F/dt=50A/\mu s$
Reverse recovery charge	$Q_{rr}$	-	1	-	$\mu C$	$V_R=400V, I_F=2.3A, di_F/dt=50A/\mu s$
Peak reverse recovery current	$I_{rrm}$	-	10	-	A	$V_R=400V, I_F=2.3A, di_F/dt=50A/\mu s$

**4 Electrical characteristics diagrams**

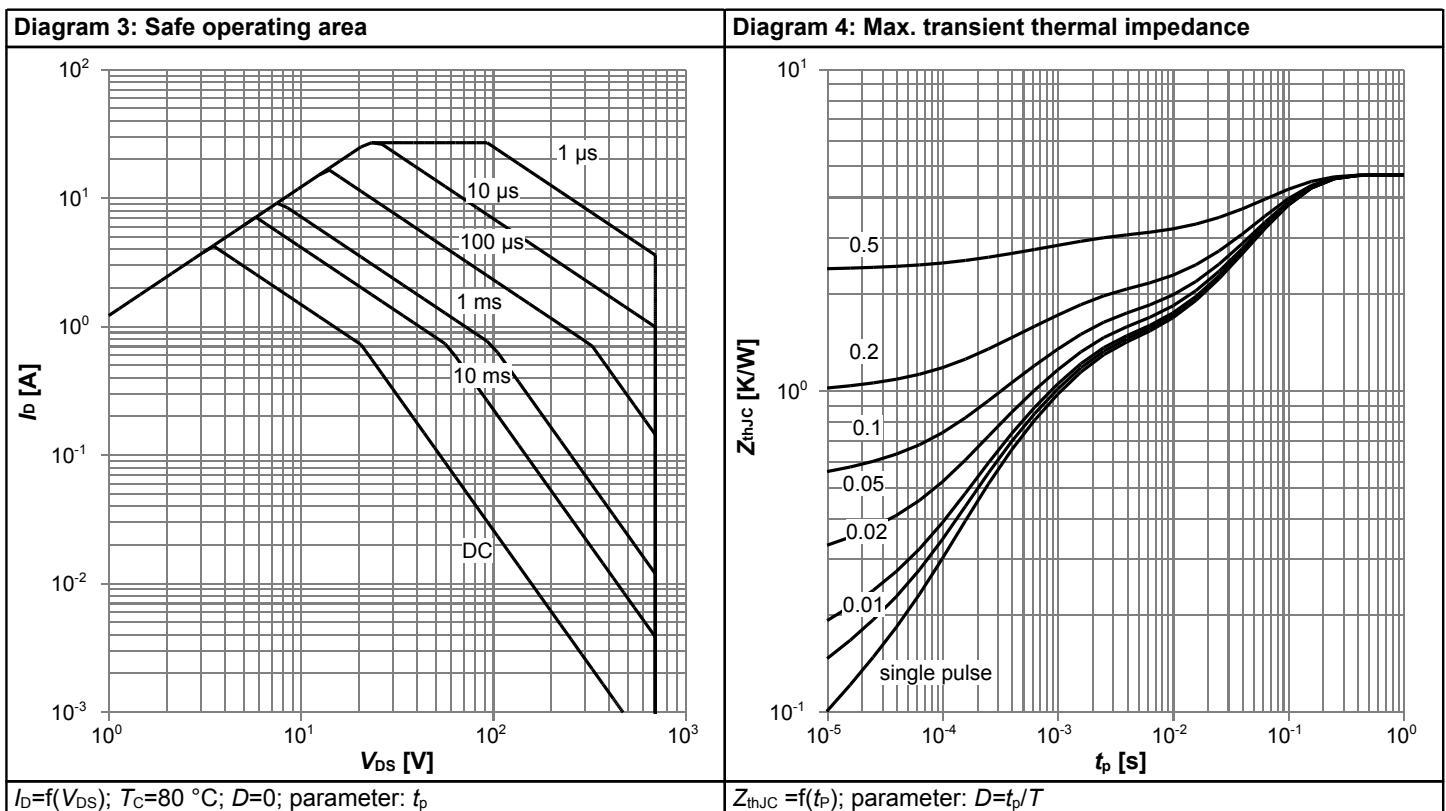
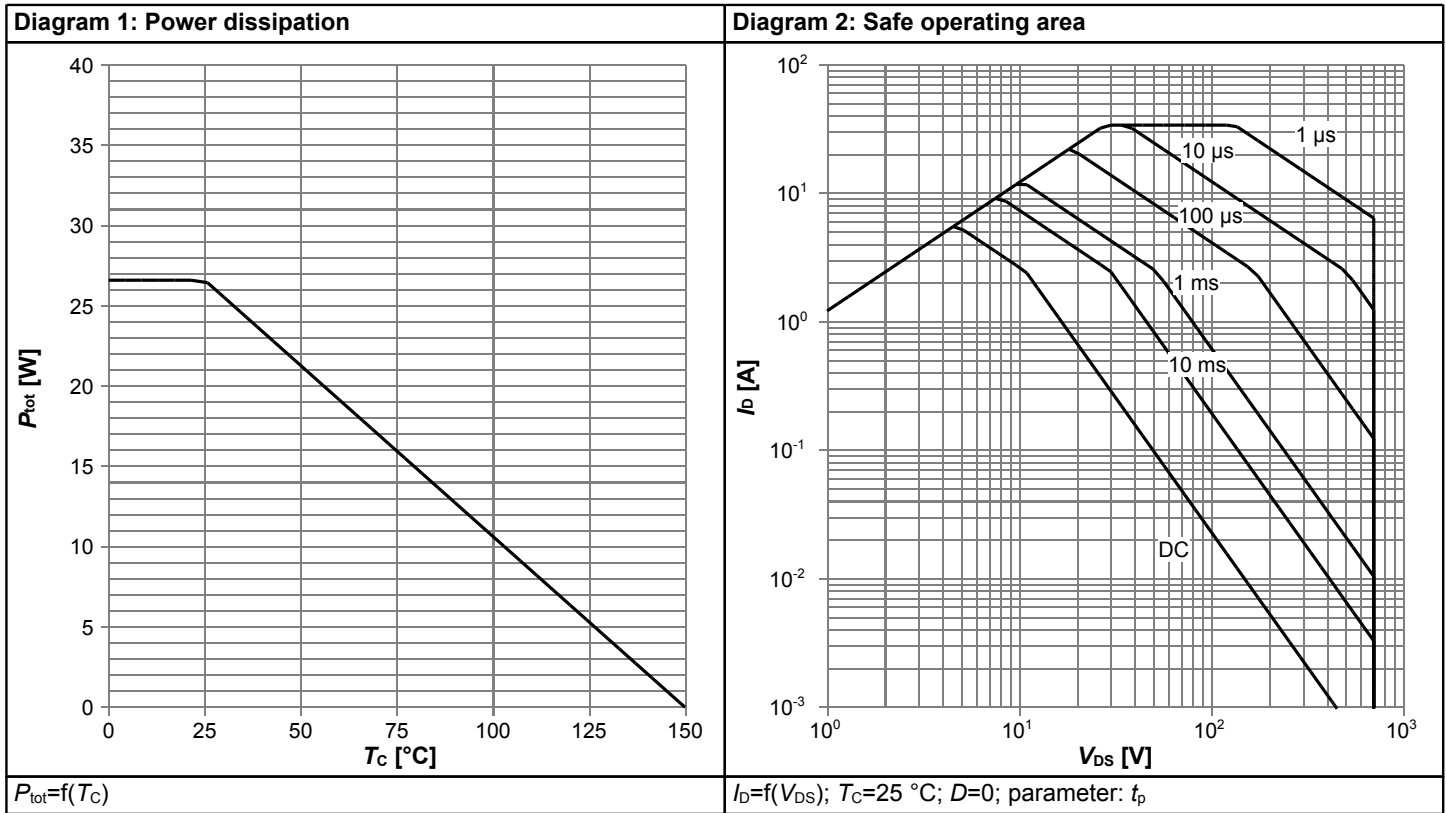
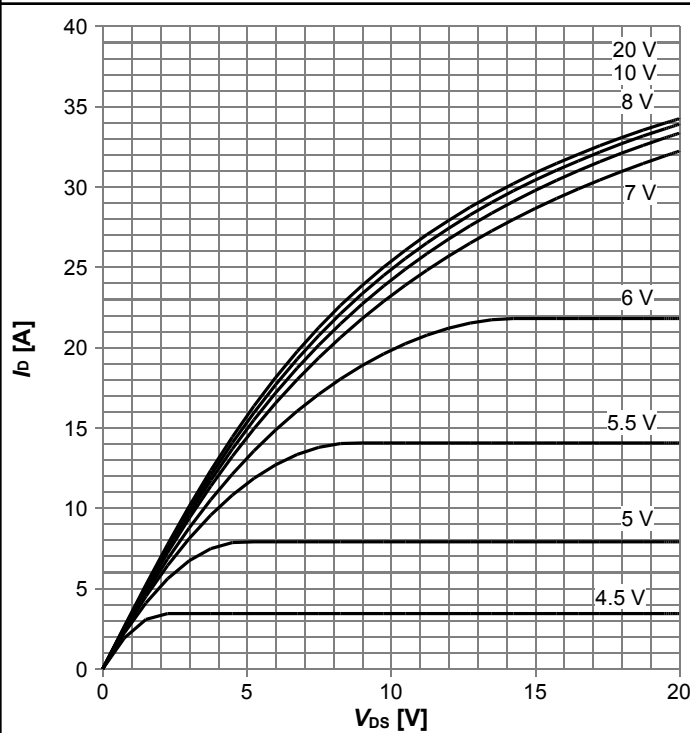
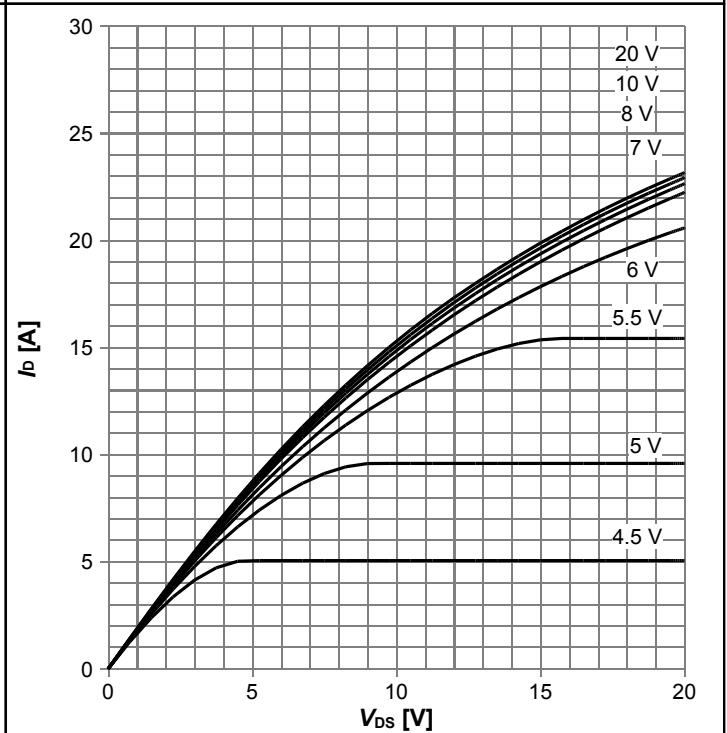


Diagram 5: Typ. output characteristics



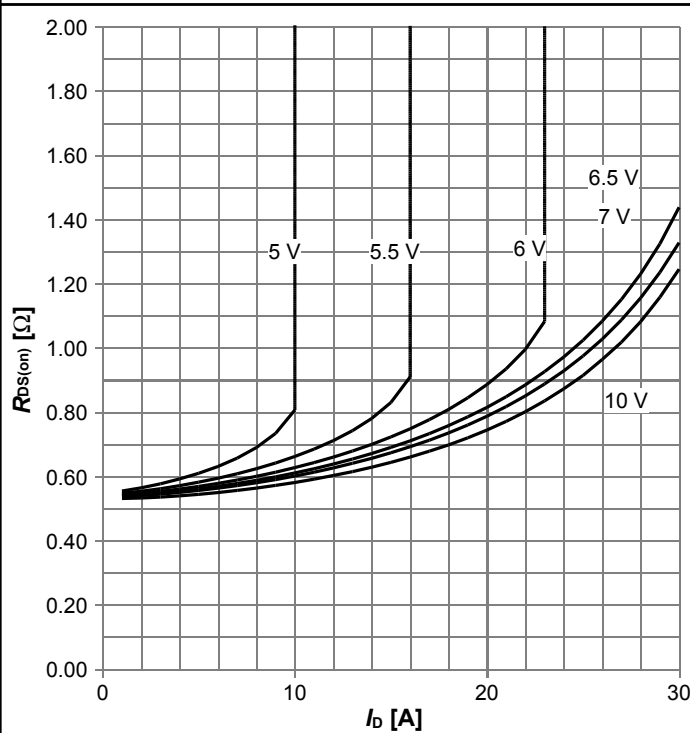
$I_D=f(V_{DS})$ ;  $T_j=25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. output characteristics



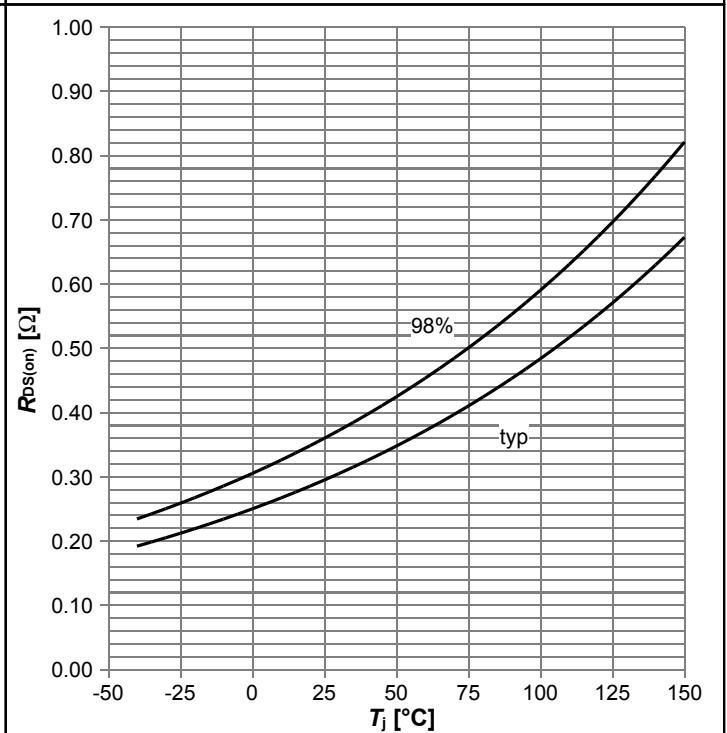
$I_D=f(V_{DS})$ ;  $T_j=125\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



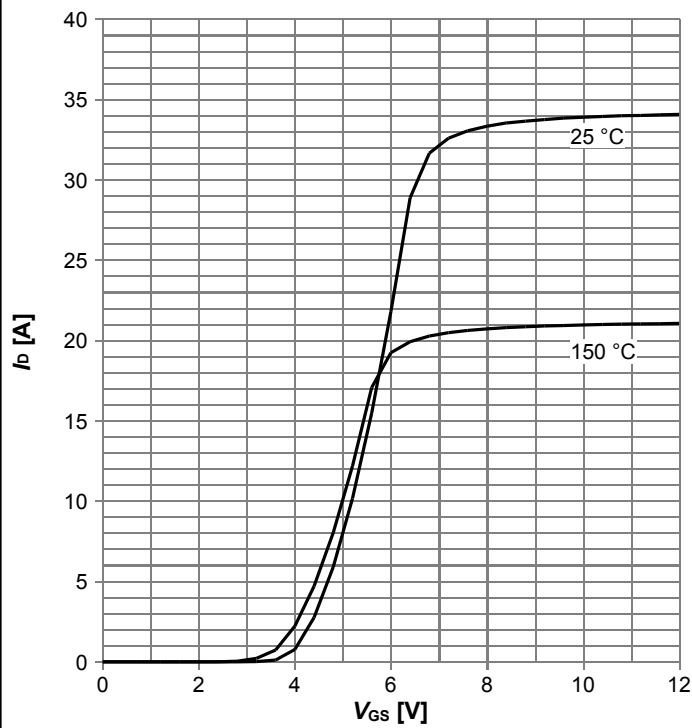
$R_{DS(on)}=f(I_D)$ ;  $T_j=125\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 8: Drain-source on-state resistance



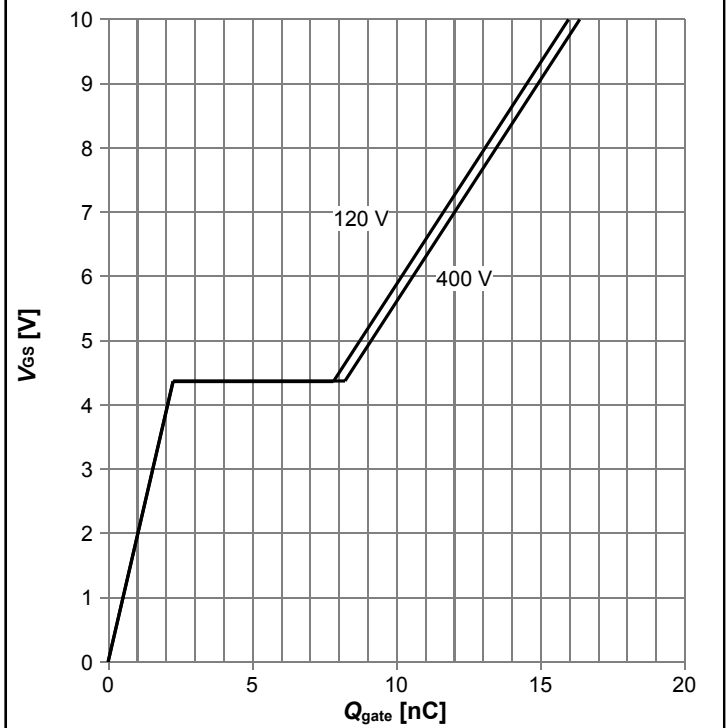
$R_{DS(on)}=f(T_j)$ ;  $I_D=3.0\text{ A}$ ;  $V_{GS}=10\text{ V}$

Diagram 9: Typ. transfer characteristics



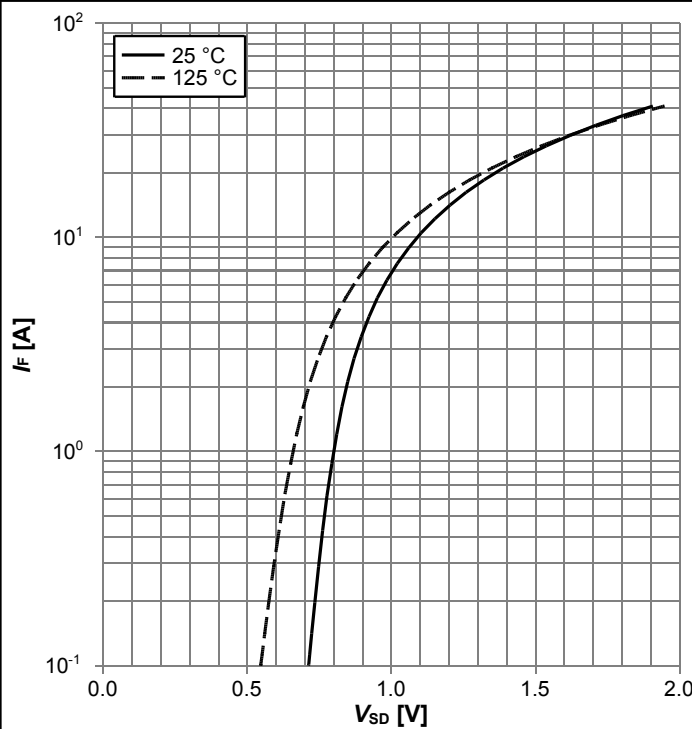
$I_D=f(V_{GS})$ ;  $V_{DS}=20V$ ; parameter:  $T_j$

Diagram 10: Typ. gate charge



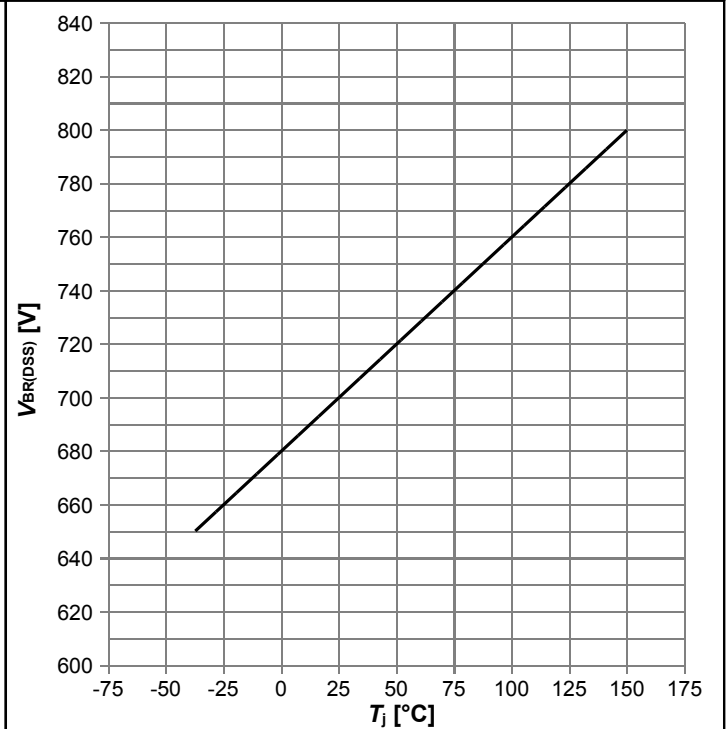
$V_{GS}=f(Q_{gate})$ ;  $I_D=2.3 A$  pulsed; parameter:  $V_{DD}$

Diagram 11: Forward characteristics of reverse diode



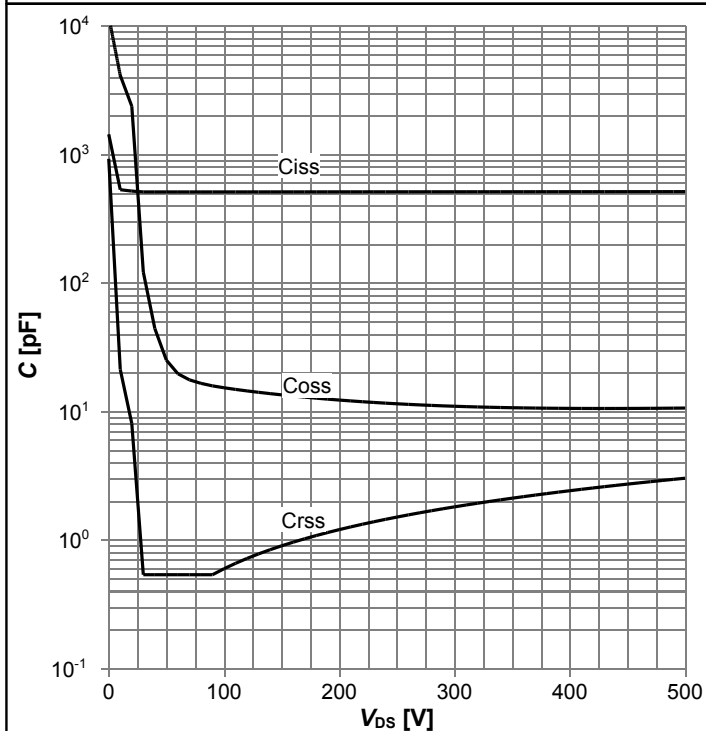
$I_F=f(V_{SD})$ ; parameter:  $T_j$

Diagram 13: Drain-source breakdown voltage



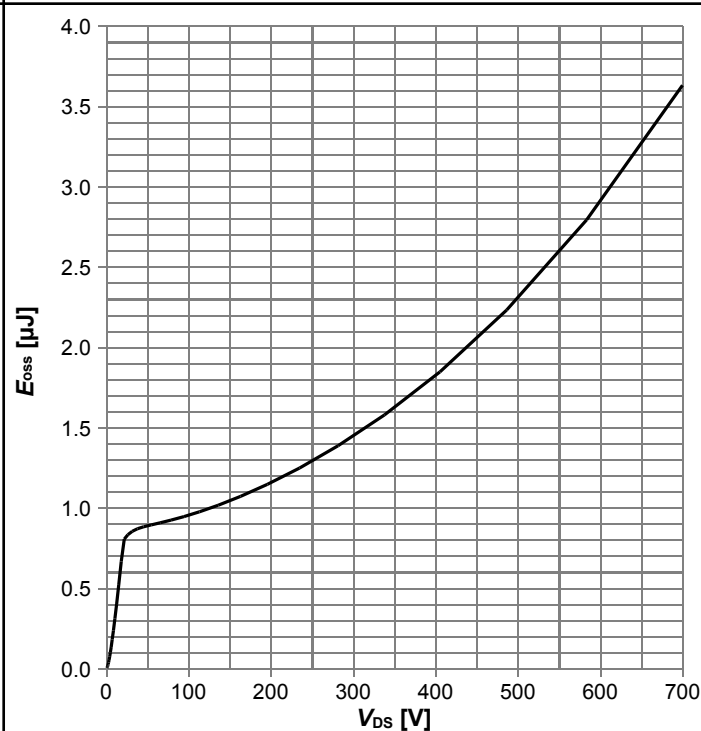
$V_{BR(DSS)}=f(T_j)$ ;  $I_D=1 mA$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0\text{ V}; f=250\text{ kHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

## 5 Test Circuits

**Table 8 Diode characteristics**

Test circuit for diode characteristics	Diode recovery waveform
<p><math>R_{g1} = R_{g2}</math></p>	<p><math>t_{rr} = t_F + t_S</math>  <math>Q_{rr} = Q_F + Q_S</math></p>

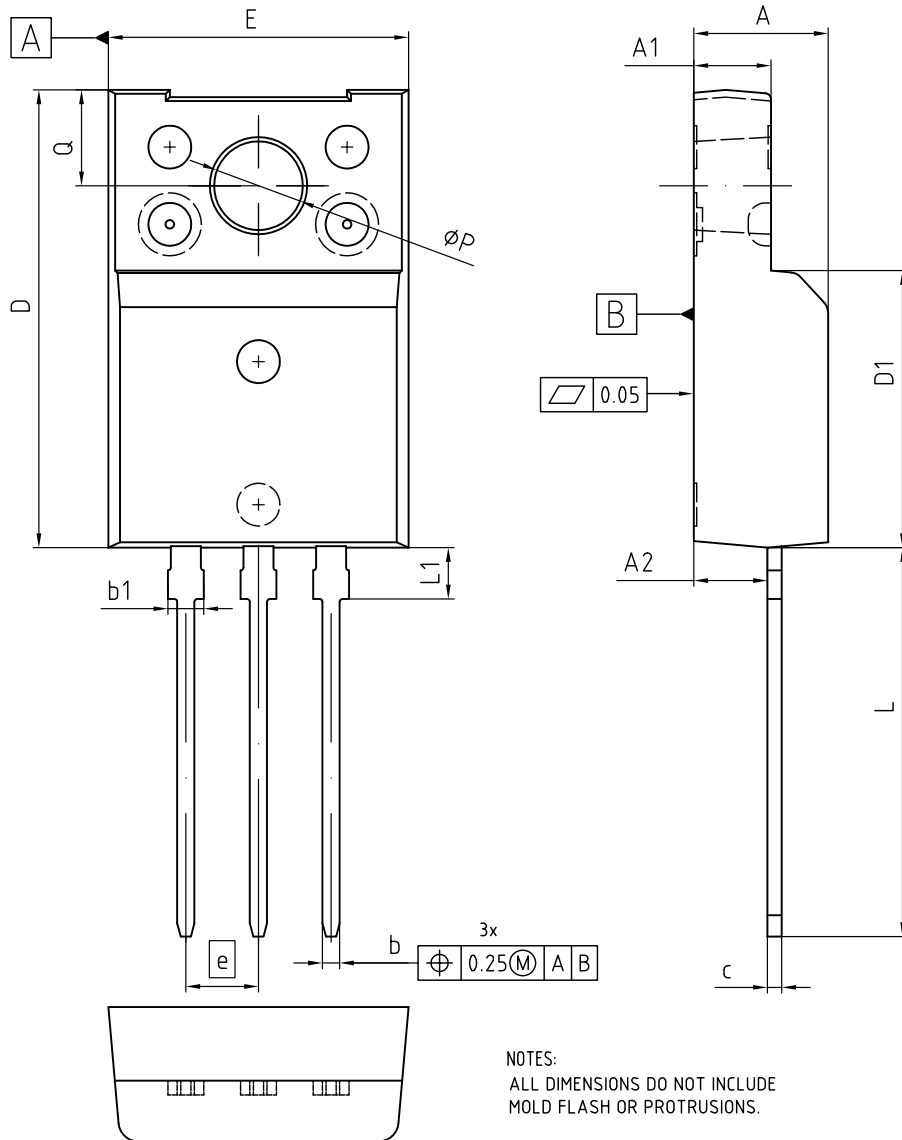
**Table 9 Switching times**

Switching times test circuit for inductive load	Switching times waveform

**Table 10 Unclamped inductive load**

Unclamped inductive load test circuit	Unclamped inductive waveform

**6 Package Outlines**



NOTES:  
 ALL DIMENSIONS DO NOT INCLUDE  
 MOLD FLASH OR PROTRUSIONS.

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.60	4.80
A1	2.60	2.80
A2	2.47	2.67
b	0.56	0.69
b1	1.01	1.15
c	0.46	0.59
D	15.90	16.10
D1	9.58	9.78
E	10.40	10.60
e	2.54	
N	3	
L	13.45	13.75
L1	1.70	1.90
øP	3.00	3.20
Q	3.25	3.45

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Figure 1 Outline PG-TO 220 FullPAK - Narrow Lead, dimensions in mm/inches

## 7 Appendix A

### Table 11 Related Links

- IFX CoolMOS™ P7 Webpage: [www.infineon.com](http://www.infineon.com)
- IFX Design tools: [www.infineon.com](http://www.infineon.com)

## Revision History

IPAN70R360P7S

Revision: 2017-02-15, Rev. 2.0

### Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2017-02-15	Release of final version

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