International
IOR Rectifier

Data Sheet No. PD60018-M

IR2121 & (PbF)

CURRENT LIMITING LOW SIDE DRIVER

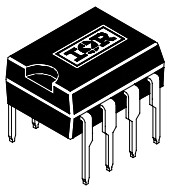
Features

- Gate drive supply range from 12 to 18V
- Undervoltage lockout
- Current detection and limiting loop to limit driven power transistor current
- Error lead indicates fault conditions and programs shutdown time
- Output in phase with input
- 2.5V, 5V and 15V input logic compatible
- Also available LEAD-FREE

Product Summary

V_{OFFSET}	5V max.
I_O+/-	1A / 2A
V_{OUT}	12 - 18V
V_{CSth}	230 mV
$t_{on/off}$ (typ.)	150 & 150 ns

Package

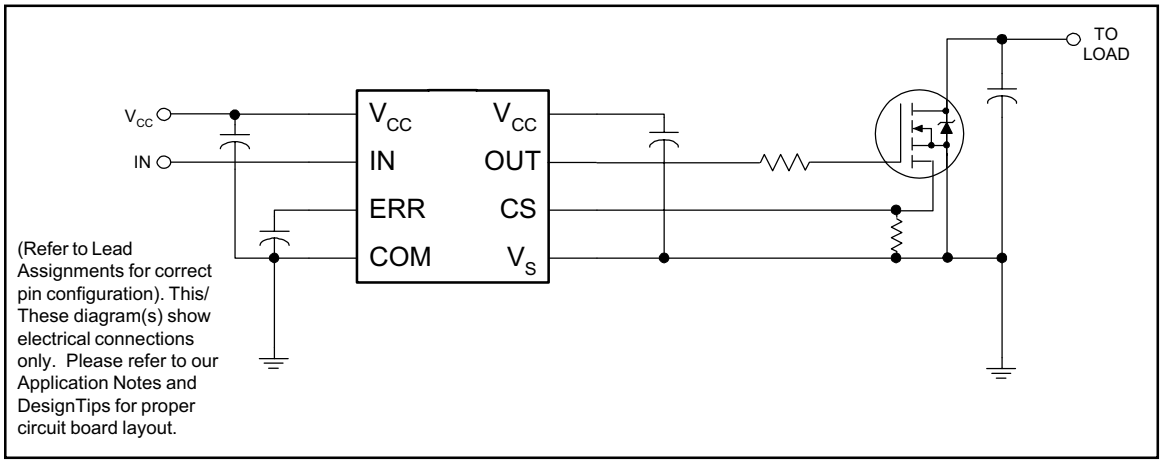


8-Lead PDIP

Description

The IR2121 is a high speed power MOSFET and IGBT driver with over-current limiting protection circuitry. Latch immune CMOS technology enables ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs, down to 2.5V logic. The output driver features a high pulse current buffer stage designed for minimum cross-conduction. The protection circuitry detects over-current in the driven power transistor and limits the gate drive voltage. Cycle-by-cycle shutdown is programmed by an external capacitor which directly controls the time interval between detection of the over-current limiting condition and latched shutdown. The output can be used to drive an N-channel power MOSFET or IGBT in the low side configuration.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/ These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Parameter		Value		
Symbol	Definition	Min.	Max.	Units
V_{CC}	Fixed Supply Voltage	-0.3	25	V
V_S	Gate Drive Return Voltage	V_{CC} - 25	V_{CC} + 0.3	
V_O	Output Voltage	V_S - 0.3	V_{CC} + 0.3	
V_{IN}	Logic Input Voltage	-0.3	V_{CC} + 0.3	
V_{ERR}	Error Signal Voltage	-0.3	V_{CC} + 0.3	
V_{CS}	Current Sense Voltage	V_S - 0.3	V_{CC} + 0.3	
P_D	Package Power Dissipation @ $T_A \leq +25°C$	—	1.0	W
Rth_{JA}	Thermal Resistance, Junction to Ambient	—	125	°C/W
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Parameter		Value		
Symbol	Definition	Min.	Max.	Units
V_{CC}	Fixed Supply Voltage	V_S + 12	V_S + 18	V
V_S	Gate Drive Return Voltage	-5	5	
V_O	Output Voltage	V_S	V_{CC}	
V_{IN}	Logic Input Voltage	0	V_{CC}	
V_{ERR}	Error Signal Voltage	0	V_{CC}	
V_{CS}	Current Sense Signal Voltage	V_S	V_{CC}	
T_A	Ambient Temperature	-40	125	°C

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}) = 15V, C_L = 3300 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are defined in Figures 2 through 5.

Parameter			Value				
Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	7	—	150	200	ns	V_{IN} = 0 & 5V
t_{off}	Turn-Off Propagation Delay	8	—	200	250		
t_{sd}	ERR Shutdown Propagation Delay	9	—	1.7	2.2	µs	
t_r	Turn-On Rise Time	10	—	43	60	ns	
t_f	Turn-Off Fall Time	11	—	26	35		
t_{cs}	CS Shutdown Propagation Delay	12	—	0.7	1.2	µs	
t_{err}	CS to ERR Pull-Up Propagation Delay	13	—	9.0	12		C_{ERR} = 270 pF

Static Electrical Characteristics

V_{BIAS} (V_{CC}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to V_S .

Parameter			Value				
Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “1” Input Voltage	14	2.2	—	—	V	
V_{IL}	Logic “0” Input Voltage	15	—	—	0.8		
V_{CSTH+}	CS Input Positive Going Threshold	16	150	230	320	mV	
V_{CSTH-}	CS Input Negative Going Threshold	17	130	210	300		
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O	18	—	—	100		I_O = 0A
V_{OL}	Low Level Output Voltage, V_O	19	—	—	100		I_O = 0A
I_{QCC}	Quiescent V_{CC} Supply Current	20	—	1.1	2.2	mA	V_{IN} = V_{CS} = 0V or 5V
I_{IN+}	Logic “1” Input Bias Current	21	—	4.5	10	µA	V_{IN} = 5V
I_{IN-}	Logic “0” Input Bias Current	22	—	—	1.0		V_{IN} = 0V
I_{CS+}	“High” CS Bias Current	23	—	4.5	10		V_{CS} = 3V or 5V
I_{CS-}	“Low” CS Bias Current	24	—	—	1.0		V_{CS} = 0V
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	25	8.3	8.9	9.6	V	
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	26	7.3	8.0	8.7		
I_{ERR}	ERR Timing Charge Current	27	65	100	130	µA	V_{IN} = 5V, V_{CS} = 3V ERR < V_{ERR+}
I_{ERR+}	ERR Pull-Up Current	28	8.0	15	—	mA	V_{IN} = 5V, V_{CS} = 3V ERR > V_{ERR+}
I_{ERR-}	ERR Pull-Down Current	29	16	30	—		V_{IN} = 0V
I_{O+}	Output High Short Circuit Pulsed Current	30	1.0	1.6	—	A	V_O = 0V, V_{IN} = 5V PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	31	2.0	3.3	—		V_O = 15V, V_{IN} = 0V PW ≤ 10 µs