

IR2213(S) & (PbF)

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
Fully operational to +1200V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 12 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible
Separate logic supply range from 3.3V to 20V
Logic and power ground $\pm 5V$ offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs
- Also available LEAD-FREE (PbF)

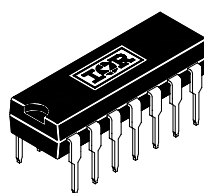
Description

The IR2213(S) is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 1200 volts.

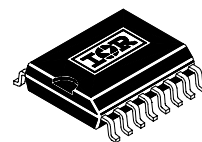
Product Summary

V_{OFFSET}	1200V max.
I_O+/-	1.7A / 2A
V_{OUT}	12 - 20V
t_{on/off} (typ.)	280 & 225 ns
Delay Matching	30 ns

Packages

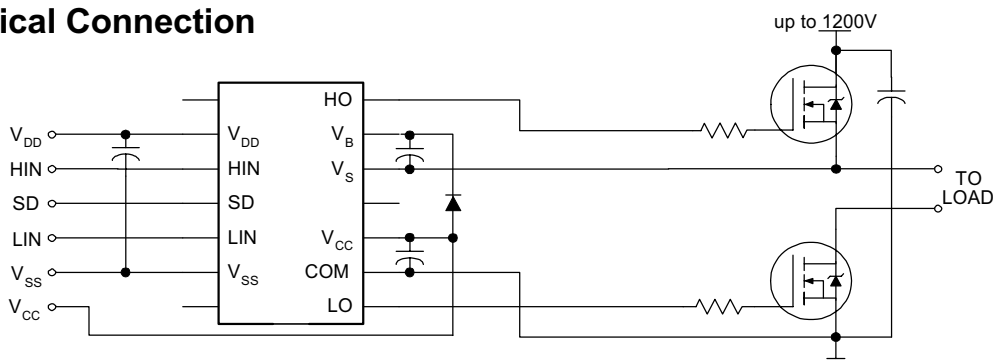


14-Lead PDIP



16-Lead SOIC
(wide body)

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

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Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V _B	High Side Floating Supply Voltage	-0.3	1225	
V _S	High Side Floating Supply Offset Voltage	V _B - 25	V _B + 0.3	V
V _{HO}	High Side Floating Output Voltage	V _S - 0.3	V _B + 0.3	
V _{CC}	Low Side Fixed Supply Voltage	-0.3	25	
V _{LO}	Low Side Output Voltage	-0.3	V _{CC} + 0.3	
V _{DD}	Logic Supply Voltage	-0.3	V _{SS} + 25	
V _{SS}	Logic Supply Offset Voltage	V _{CC} - 25	V _{CC} + 0.3	
V _{IN}	Logic Input Voltage (HIN, LIN & SD)	V _{SS} - 0.3	V _{DD} + 0.3	
dV _S /dt	Allowable Offset Supply Voltage Transient (Figure 2)	—	50	V/ns
P _D	Package Power Dissipation @ T _A ≤ +25°C	(14 Lead PDIP)	—	W
		(16 Lead SOIC)	—	
R _{THJA}	Thermal Resistance, Junction to Ambient	(14 Lead PDIP)	—	°C/W
		(16 Lead SOIC)	—	
T _J	Junction Temperature	—	125	°C
T _S	Storage Temperature	-55	150	
T _L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V _B	High Side Floating Supply Absolute Voltage	V _S + 12	V _S + 20	V
V _S	High Side Floating Supply Offset Voltage	Note 1	1200	
V _{HO}	High Side Floating Output Voltage	V _S	V _B	
V _{CC}	Low Side Fixed Supply Voltage	12	20	
V _{LO}	Low Side Output Voltage	0	V _{CC}	
V _{DD}	Logic Supply Voltage	V _{SS} + 3	V _{SS} + 20	
V _{SS}	Logic Supply Offset Voltage	-5 (Note 2)	5	
V _{IN}	Logic Input Voltage (HIN, LIN & SD)	V _{SS}	V _{DD}	

Note 1: Logic operational for V_S of -5 to +1200V. Logic state held for V_S of -5V to -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).

Note 2: When V_{DD}<5V, the minimum V_{SS} offset is limited to -V_{DD}

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15V, C_L = 1000 pF, T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	—	280	—	ns	$V_S = 0V$
t_{off}	Turn-Off Propagation Delay	—	225	—		$V_S = 1200V$
t_{sd}	Shutdown Propagation Delay	—	230	—		$V_S = 1200V$
t_r	Turn-On Rise Time	—	25	—		
t_f	Turn-Off Fall Time	—	17	—		
MT	Delay Matching, HS & LS Turn-On/Off	—	—	30		

Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" Input Voltage	9.5	—	—	V	
V_{IL}	Logic "0" Input Voltage	—	—	6.0		
V_{OH}	High Level Output Voltage, $V_{BIAS} - V_O$	—	—	1.2		$I_O = 0A$
V_{OL}	Low Level Output Voltage, V_O	—	—	0.1		$I_O = 0A$
I_{LK}	Offset Supply Leakage Current	—	—	50	μA	$V_B = V_S = 1200V$
I_{QBS}	Quiescent V_{BS} Supply Current	—	125	230		$V_{IN} = 0V$ or V_{DD}
I_{QCC}	Quiescent V_{CC} Supply Current	—	180	340		$V_{IN} = 0V$ or V_{DD}
I_{QDD}	Quiescent V_{DD} Supply Current	—	15	30		$V_{IN} = 0V$ or V_{DD}
I_{IN+}	Logic "1" Input Bias Current	—	20	40		$V_{IN} = V_{DD}$
I_{IN-}	Logic "0" Input Bias Current	—	—	1.0		$V_{IN} = 0V$
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	8.7	10.2	11.7	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	7.9	9.3	10.7		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	8.7	10.2	11.7		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	7.9	9.3	10.7		
I_{O+}	Output High Short Circuit Pulsed Current	1.7	2.0	—	A	$V_O = 0V$, $V_{IN} = V_{DD}$ $PW \leq 10 \mu s$
I_{O-}	Output Low Short Circuit Pulsed Current	2.0	2.5	—		$V_O = 15V$, $V_{IN} = 0V$ $PW \leq 10 \mu s$

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Symbol	Description
V _{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V _{SS}	Logic ground
V _B	High side floating supply
HO	High side gate drive output
V _S	High side floating supply return
V _{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

14 Lead PDIP	16 Lead SOIC (Wide Body)
IR2213	IR2213S
Part Number	

IR2213(s) & (PbF)

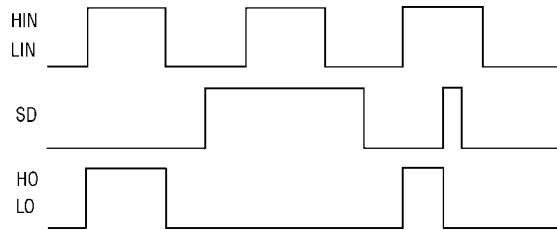


Figure 1. Input/Output Timing Diagram

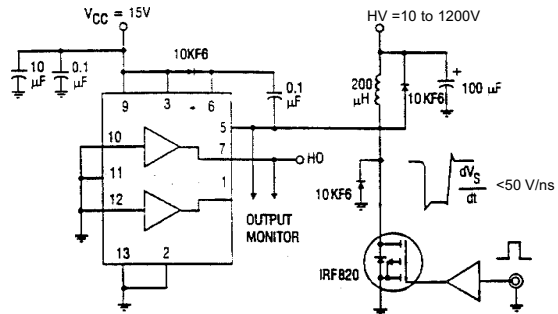


Figure 2. Floating Supply Voltage Transient Test Circuit

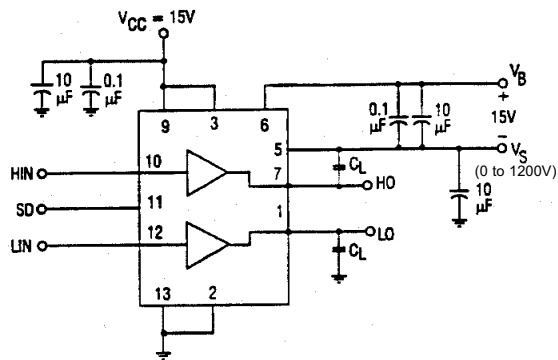


Figure 3. Switching Time Test Circuit

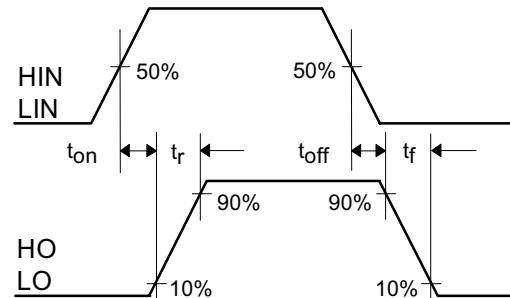


Figure 4. Switching Time Waveform Definition

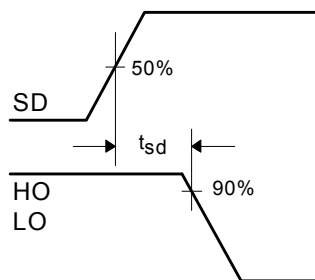


Figure 5. Shutdown Waveform Definitions

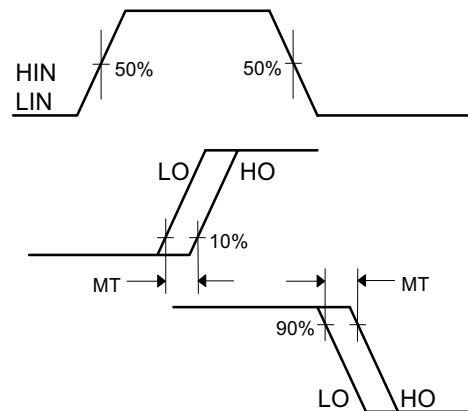


Figure 6. Delay Matching Waveform Definitions

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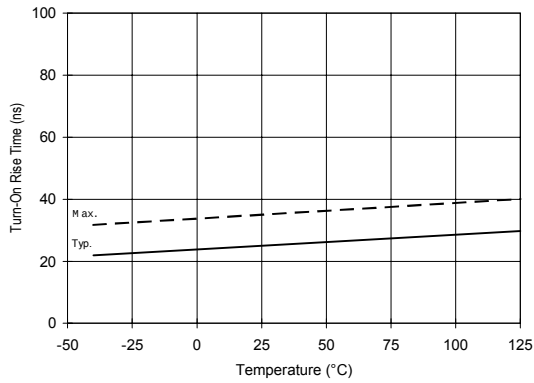


Figure 10A. Turn-On Rise Time vs. Temperature

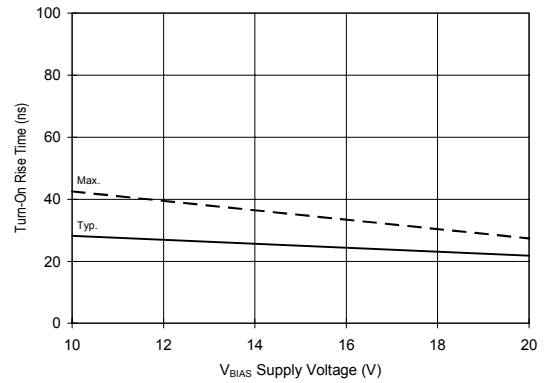


Figure 10B. Turn-On Rise Time vs. Voltage

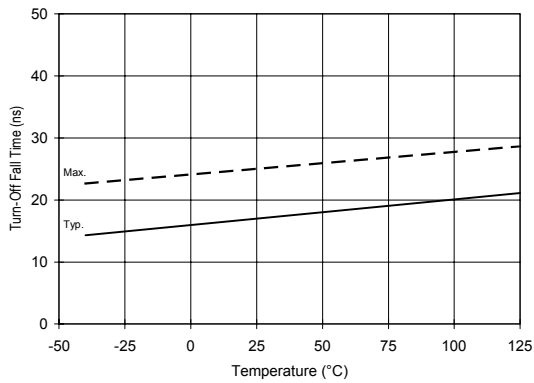


Figure 11A. Turn-Off Fall Time vs. Temperature

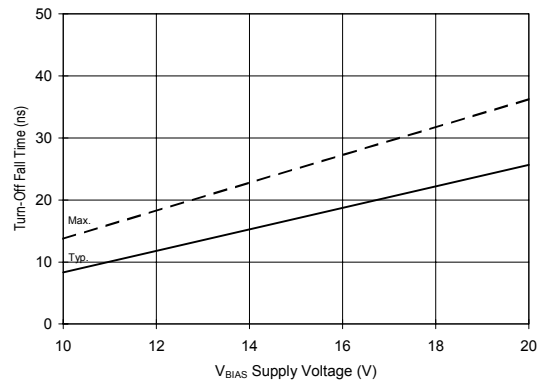


Figure 11B. Turn-Off Fall Time vs. Voltage

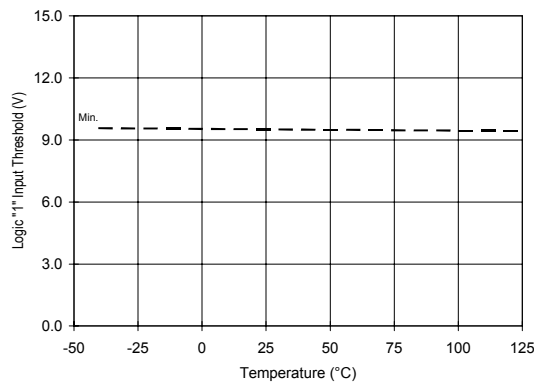


Figure 12A. Logic "1" Input Threshold vs. Temperature

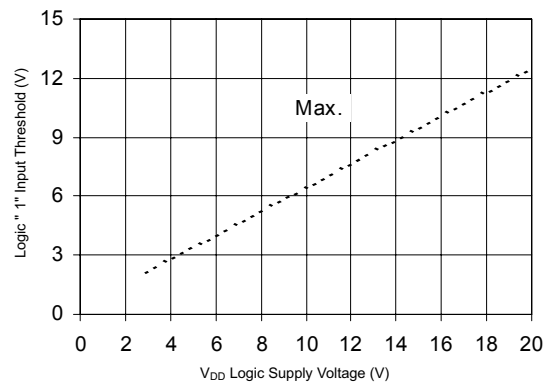


Figure 12B. Logic "1" Input Threshold vs. Voltage

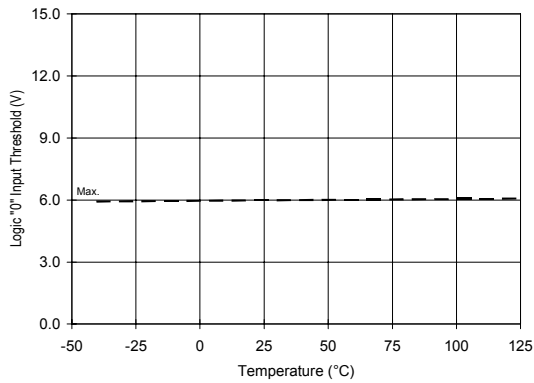


Figure 13A. Logic "0" Input Threshold vs. Temperature

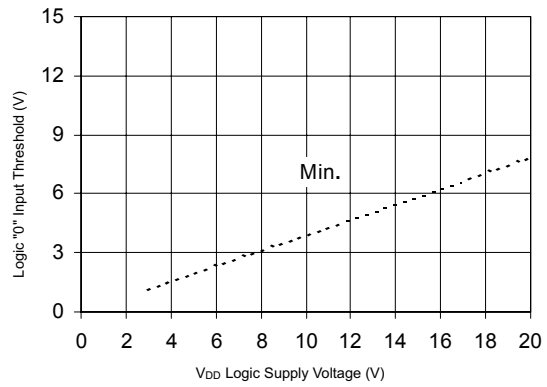


Figure 13B. Logic "0" Input Threshold vs. Voltage

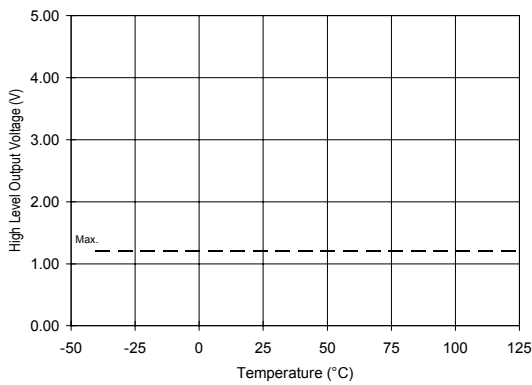


Figure 14A. High Level Output vs. Temperature

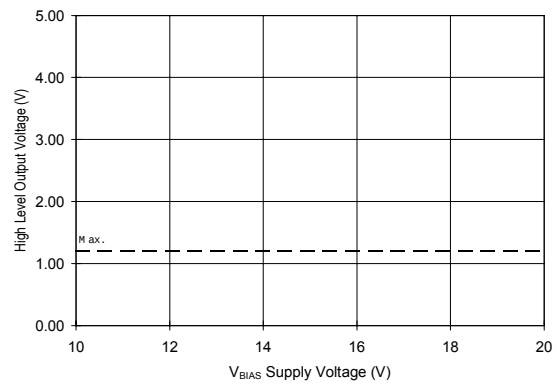


Figure 14B. High Level Output vs. Voltage

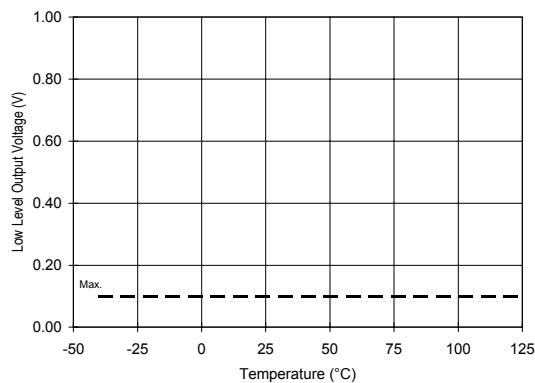


Figure 15A. Low Level Output vs. Temperature

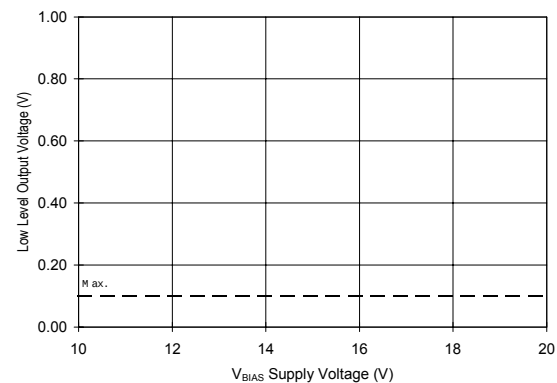


Figure 15B. Low Level Output vs. Voltage

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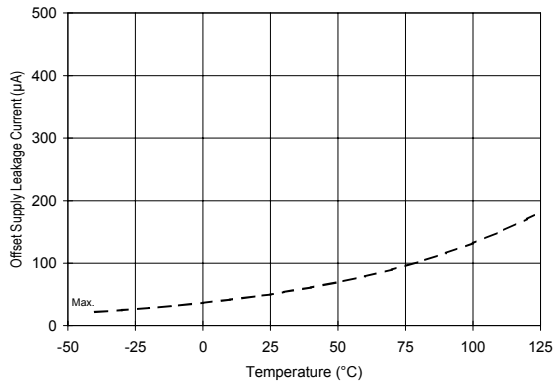


Figure 16A. Offset Supply Current vs. Temperature

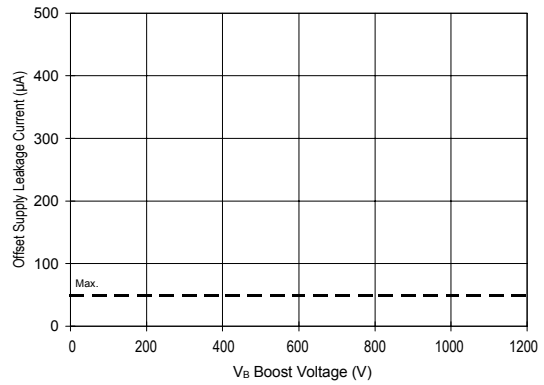


Figure 16B. Offset Supply Current vs. Voltage

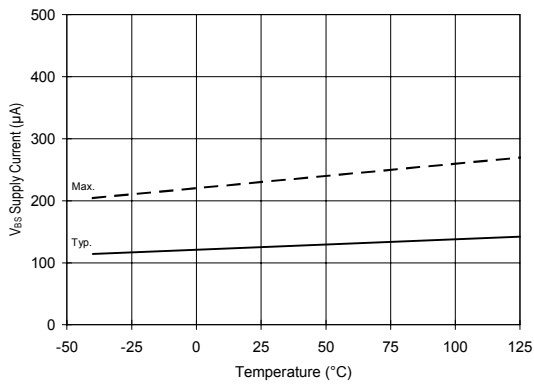


Figure 17A. V_{BS} Supply Current vs. Temperature

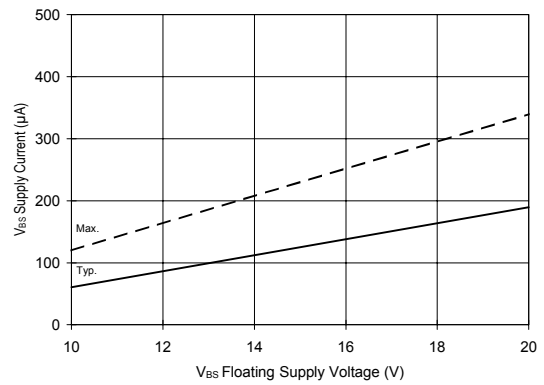


Figure 17B. V_{BS} Supply Current vs. Voltage

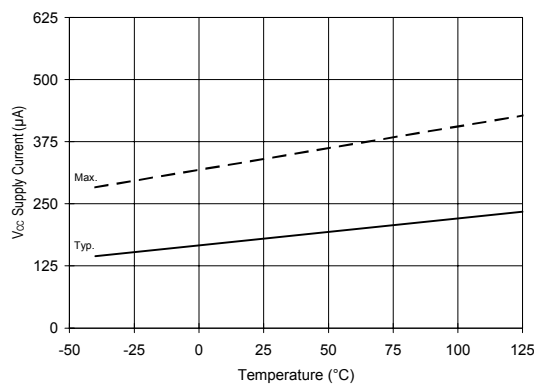


Figure 18A. V_{CC} Supply Current vs. Temperature

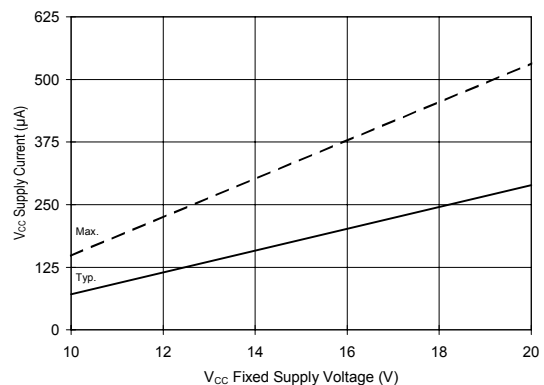


Figure 18B. V_{CC} Supply Current vs. Voltage

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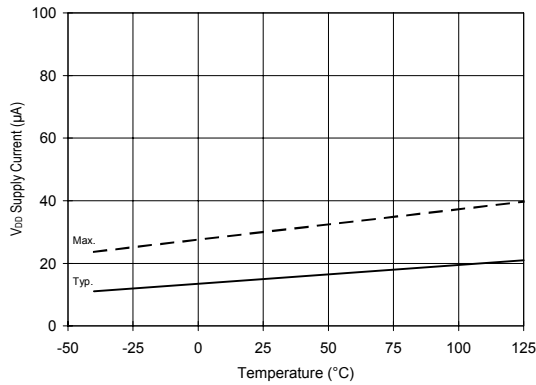


Figure 19A. V_{DD} Supply Current vs. Temperature

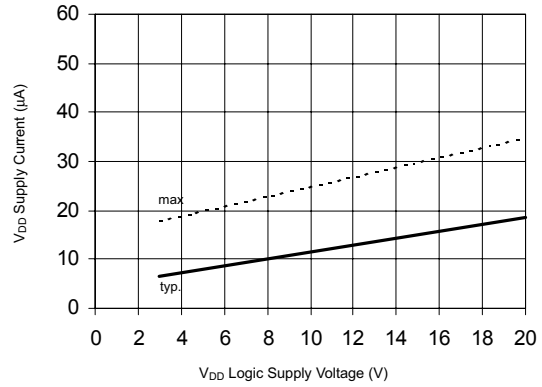


Figure 19B. V_{DD} Supply Current vs. V_{DD} Voltage

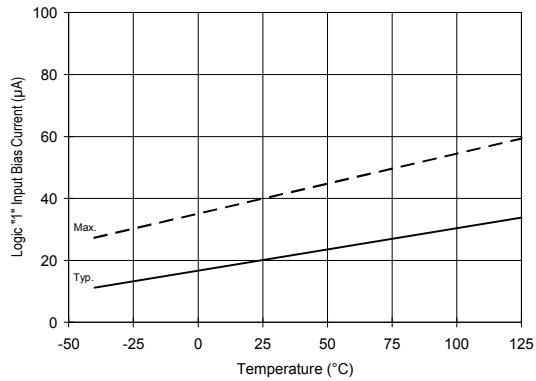


Figure 20A. Logic "1" Input Current vs. Temperature

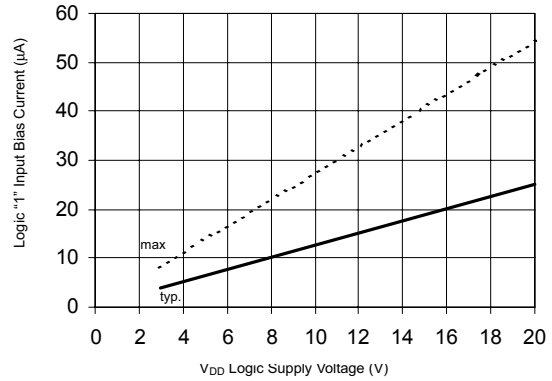


Figure 20B. Logic "1" Input Current vs. V_{DD} Voltage

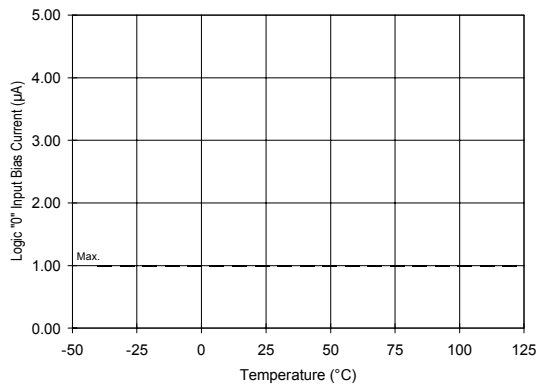


Figure 21A. Logic "0" Input Current vs. Temperature

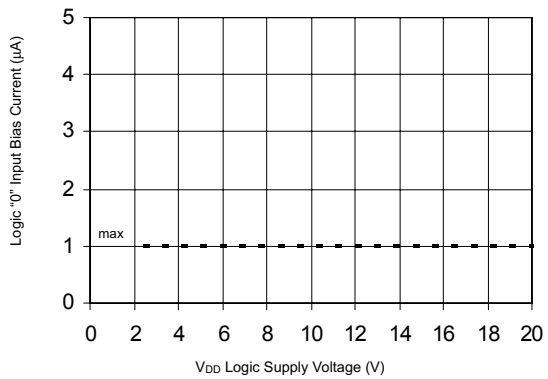


Figure 21B. Logic "0" Input Current vs. V_{DD} Voltage

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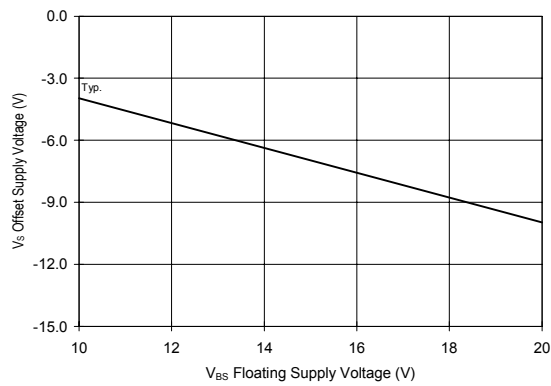


Figure 22. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

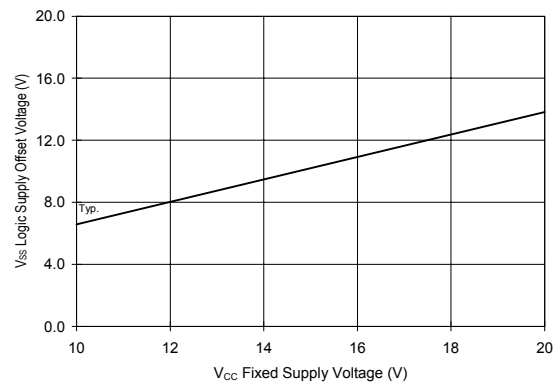


Figure 23. Maximum V_{SS} Positive Offset vs. V_{CC} Supply Voltage

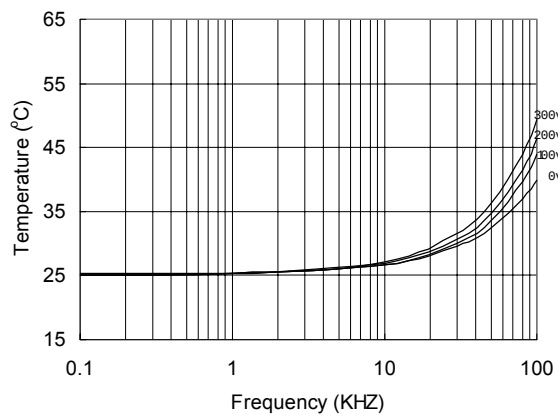


Figure 24. IR2213s vs. Frequency (IRFBC20)
 $R_{gate}=33\Omega$, $V_{CC}=15V$

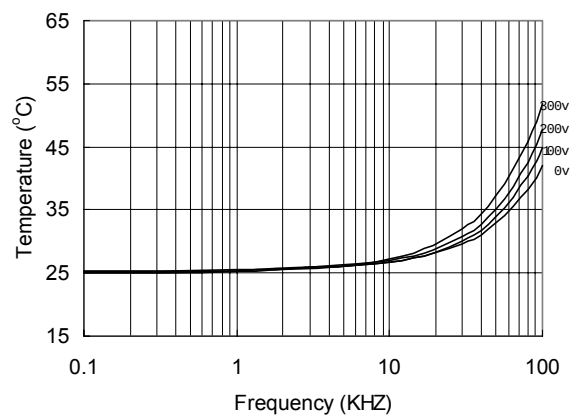


Figure 25. IR2213s vs. Frequency (IRFBC30)
 $R_{gate}=22\Omega$, $V_{CC}=15V$

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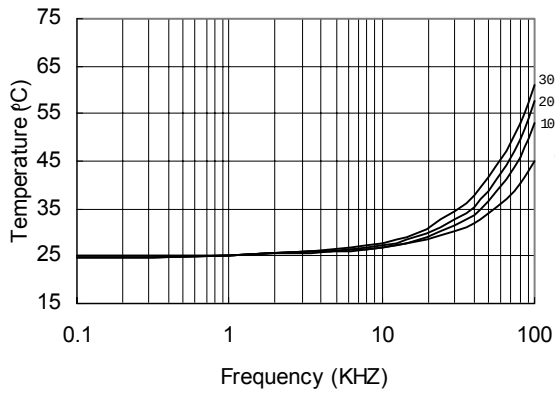


Figure 26. IR2213s vs. Frequency (IRFBC40)
 $R_{gate}=15\Omega$, $V_{CC}=15V$

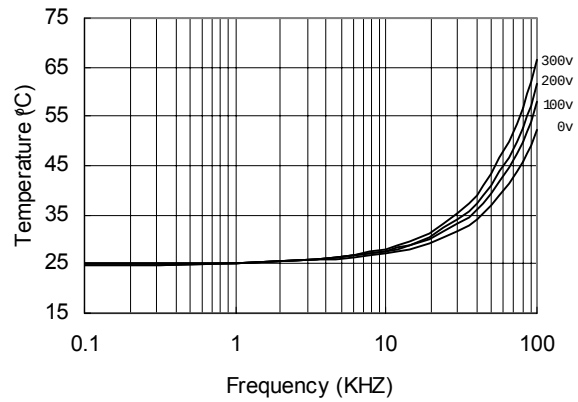


Figure 27. IR2213s vs. Frequency (IRFBC50)
 $R_{gate}=10\Omega$, $V_{CC}=15V$

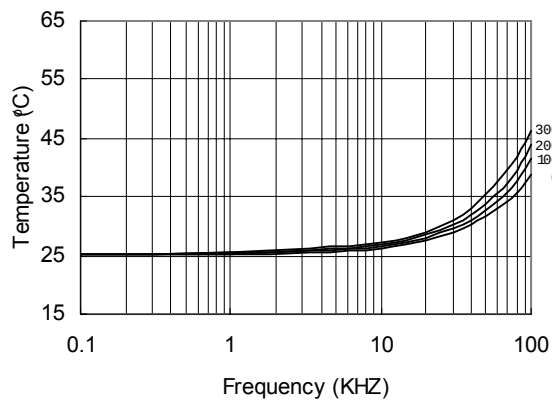


Figure 28. IR2213 vs. Frequency (IRFBC20)
 $R_{gate}=33\Omega$, $V_{CC}=15V$

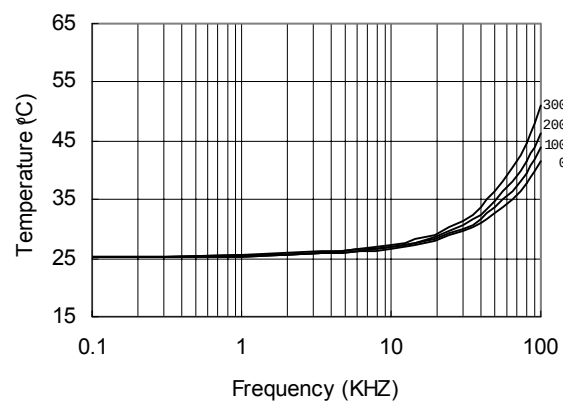


Figure 29. IR2213 vs. Frequency (IRFBC30)
 $R_{gate}=22\Omega$, $V_{CC}=15V$

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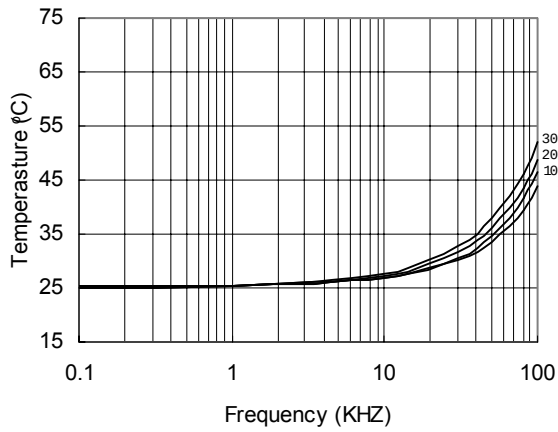


Figure 30. IR2213 vs. Frequency (IRFBC40)
 $R_{gate}=15\Omega$, $V_{CC}=15V$

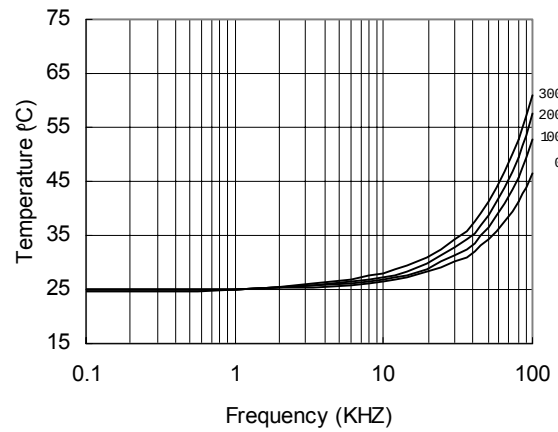


Figure 31. IR213 vs. Frequency (IRFBC50)
 $R_{gate}=10\Omega$, $V_{CC}=15V$

14-Lead PDIP

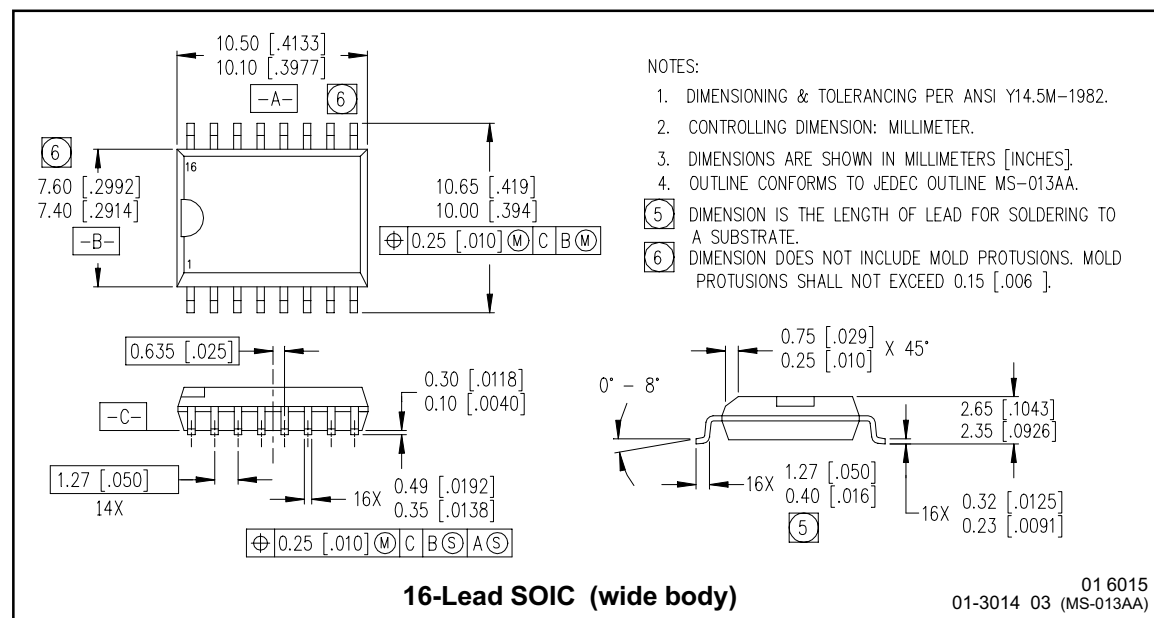
Dimensions (mm [inches]):

- Top View:
 - Overall Width: 20.19 [.795]
 - Lead Spacing: 18.42 [.725]
 - Lead Width: 1.77 [.070]
 - Lead Thickness: 1.15 [.045]
 - Lead Angle: 0° - 15°
 - Lead Length: 7.62 [.300]
 - Lead Spacing (Detail): 12X 2.54 [.100]
- Side View:
 - Overall Height: 5.33 [.210] MAX
 - Lead Height: 0.39 [.015] MIN
 - Lead Angle: 0° - 15°
 - Lead Length: 7.62 [.300]
 - Lead Spacing (Detail): 12X 2.54 [.100]
- Detail View:
 - Lead Width: 1.77 [.070]
 - Lead Thickness: 1.15 [.045]
 - Lead Angle: 0° - 15°
 - Lead Length: 7.62 [.300]
 - Lead Spacing (Detail): 12X 2.54 [.100]

Notes:

- DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AC.
- MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
- DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

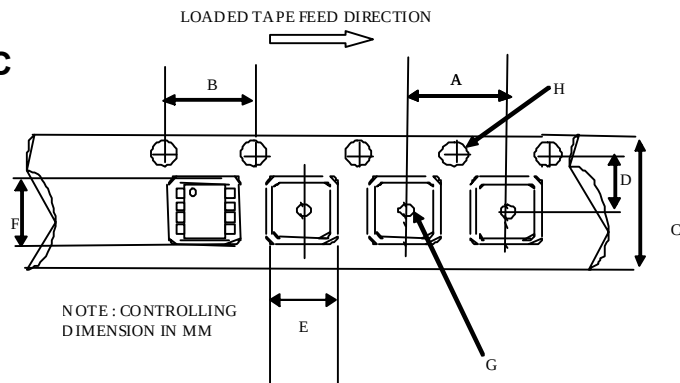
01-6010
01-3002 03 (MS-001AC)



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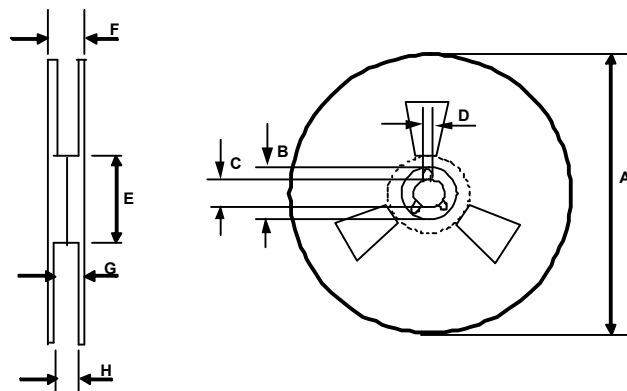
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Tape & Reel 16-Lead SOIC



CARRIER TAPE DIMENSION FOR 16SOICW

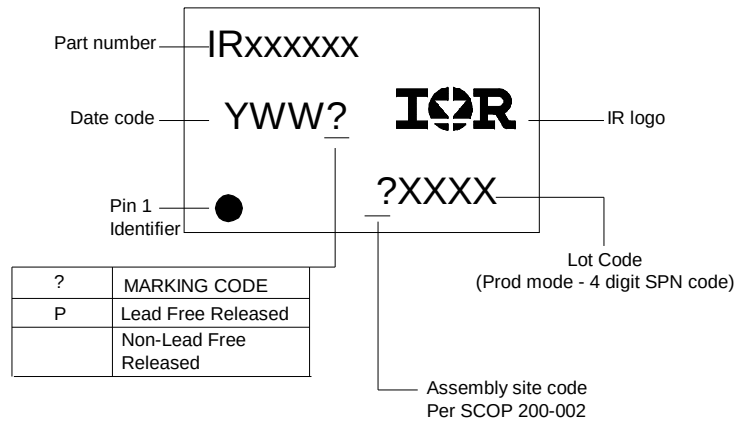
Code	Metric		Imperial	
	Min	Max	Min	Max
A	11.90	12.10	0.468	0.476
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	10.80	11.00	0.425	0.433
F	10.60	10.80	0.417	0.425
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 16SOICW

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)

14-Lead PDIP IR2213 order IR2213
16-Lead SOIC IR2213S order IR2213S
16-Lead SOIC Tape & Reel order IR2213STR

Leadfree Part

14-Lead PDIP IR2213 order IR2213PbF
16-Lead SOIC IR2213S order IR2213SPbF
16-Lead SOIC Tape & Reel order IR2213STRPbF