

IRF7490PbF

HEXFET® Power MOSFET

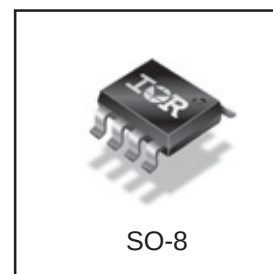
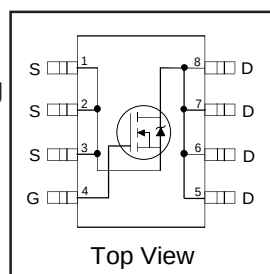
Applications

- High frequency DC-DC converters
- Lead-Free

V_{DS}	$R_{DS(on)}$ max	Q_g
100V	$39m\Omega @ V_{GS}=10V$	37nC

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	± 20	
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	5.4	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	4.3	
I_{DM}	Pulsed Drain Current ^①	43	
$P_D @ T_A = 25^\circ C$	Maximum Power Dissipation	2.5	W
$P_D @ T_A = 70^\circ C$	Maximum Power Dissipation	1.6	
	Linear Derating Factor	20	mW/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead	—	20	°C/W
$R_{\theta JA}$	Junction-to-Ambient ^④	—	50	

Notes ① through ④ are on page 9
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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to 25°C , $I_D = 1\text{mA}$ ③
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	33	39	m Ω	$V_{GS} = 10V, I_D = 3.2A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	8.0	—	—	S	$V_{DS} = 50V, I_D = 3.2A$
Q_g	Total Gate Charge	—	37	56	nC	$I_D = 3.2A$
Q_{gs}	Gate-to-Source Charge	—	8.0	—		$V_{DS} = 50V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	10	—		$V_{GS} = 10V,$
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	$V_{DD} = 100V$
t_r	Rise Time	—	4.2	—		$I_D = 3.2A$
$t_{d(off)}$	Turn-Off Delay Time	—	51	—		$R_G = 9.1\Omega$
t_f	Fall Time	—	11	—		$V_{GS} = 10V$ ③
C_{iss}	Input Capacitance	—	1720	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	220	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	25	—		$f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	1650	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	130	—		$V_{GS} = 0V, V_{DS} = 80V, f = 1.0\text{MHz}$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	250	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V$ ⑤

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	91	mJ
I_{AR}	Avalanche Current①	—	3.2	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	2.3	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	43		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 3.2A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	67	100	ns	$T_J = 25^\circ\text{C}, I_F = 3.2A$
Q_{rr}	Reverse Recovery Charge	—	220	330	nC	$di/dt = 100A/\mu s$ ③

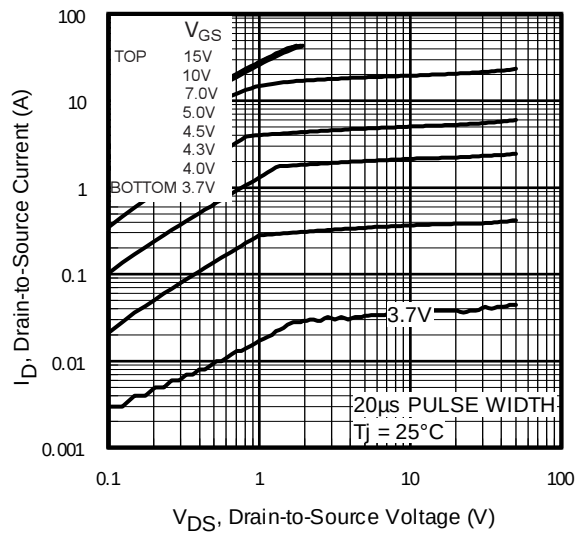


Fig 1. Typical Output Characteristics

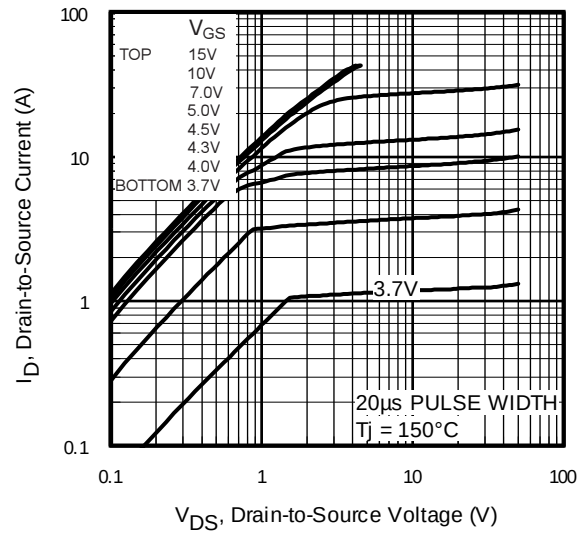


Fig 2. Typical Output Characteristics

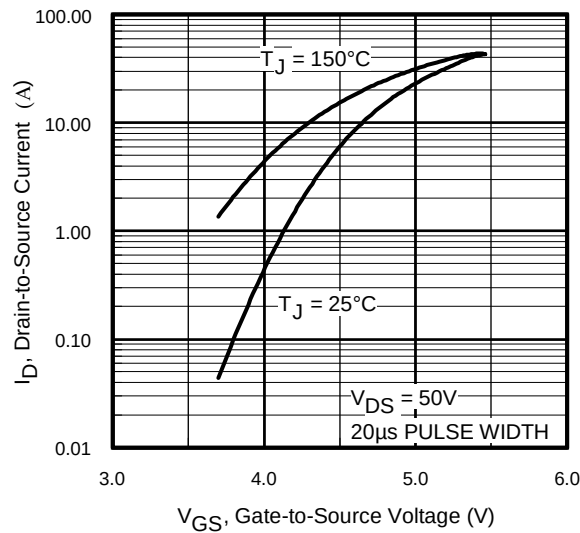


Fig 3. Typical Transfer Characteristics

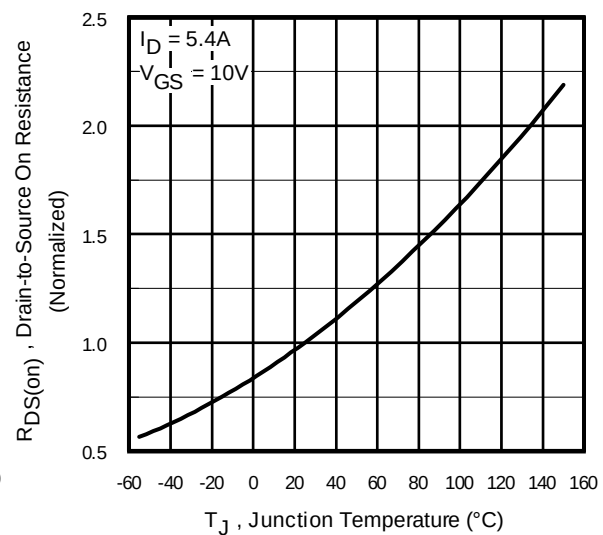
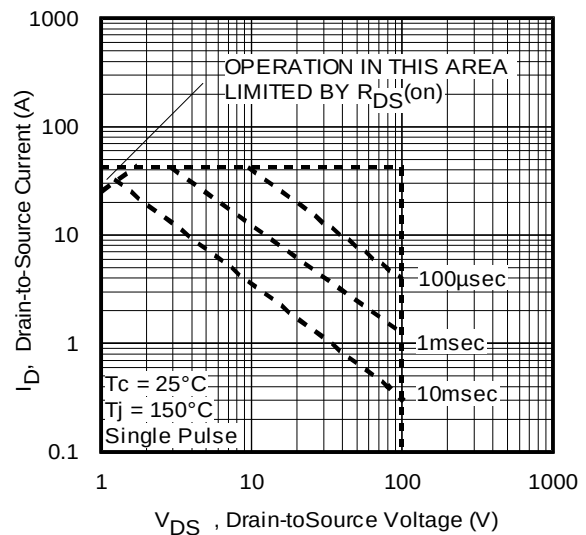
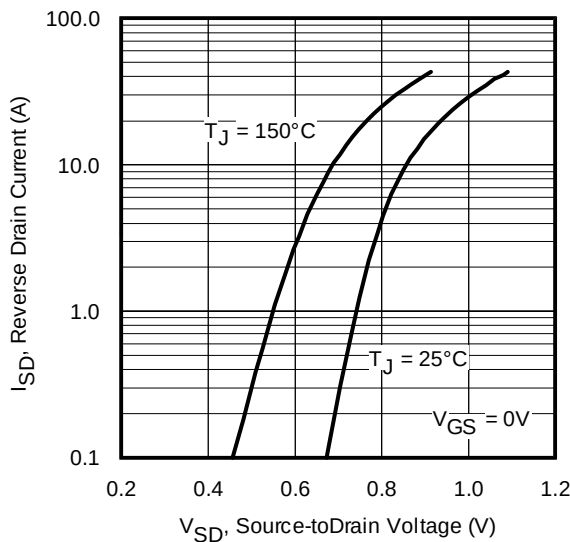
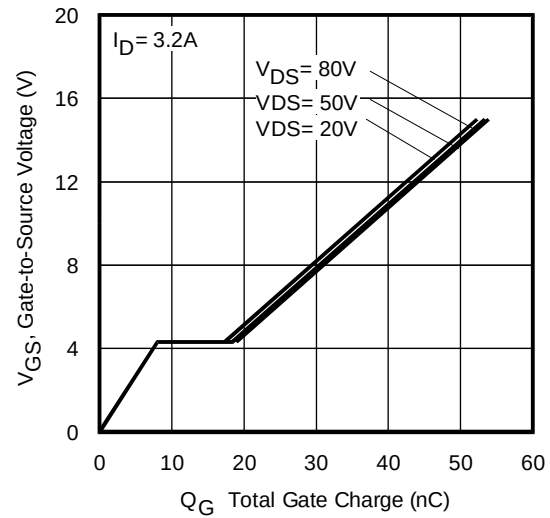
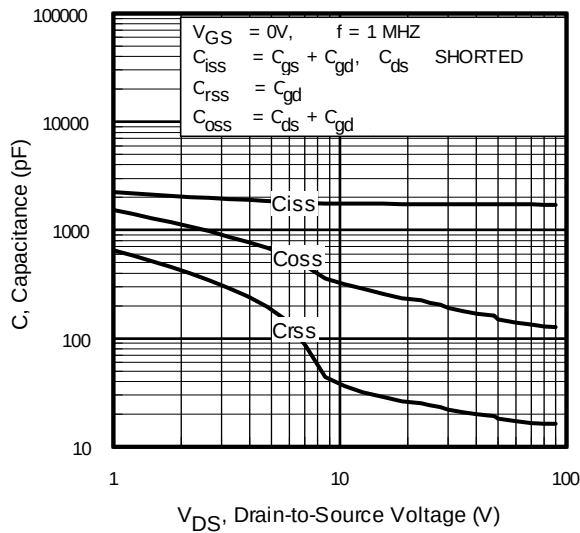


Fig 4. Normalized On-Resistance
Vs. Temperature



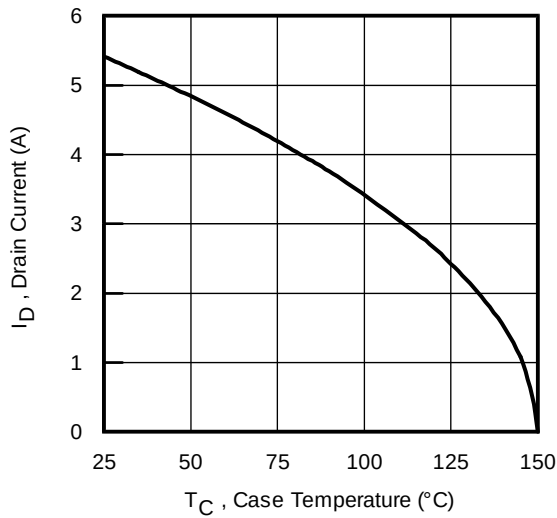


Fig 9. Maximum Drain Current Vs. Ambient Temperature

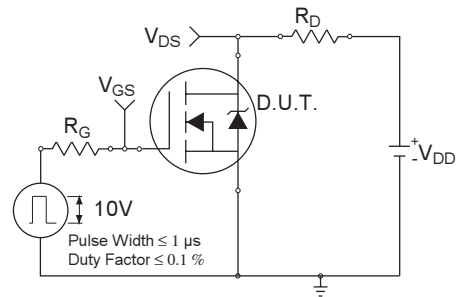


Fig 10a. Switching Time Test Circuit

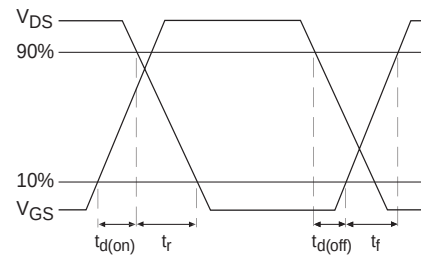


Fig 10b. Switching Time Waveforms

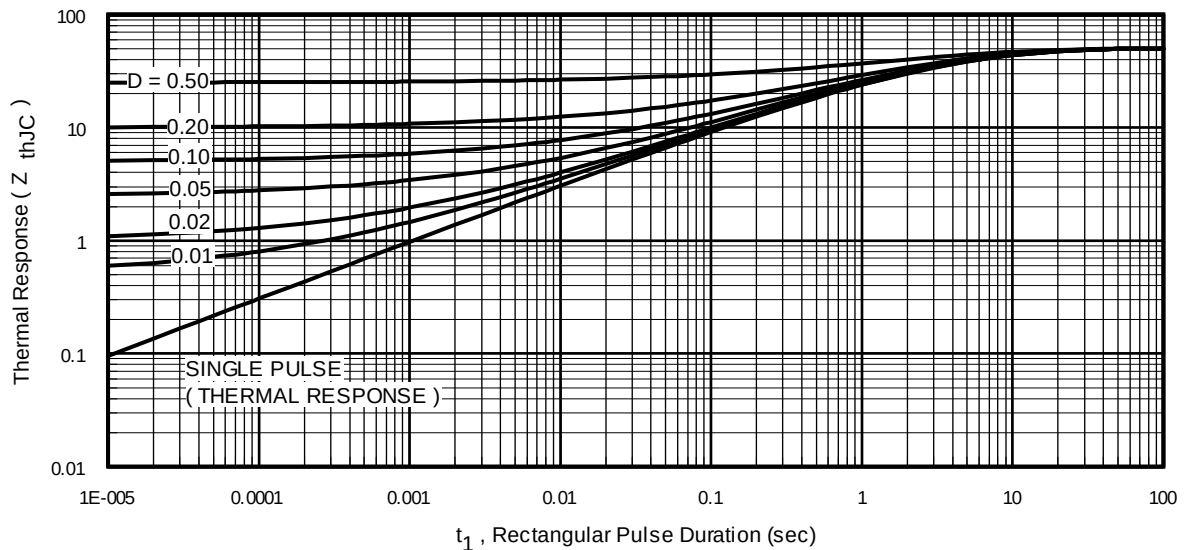


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

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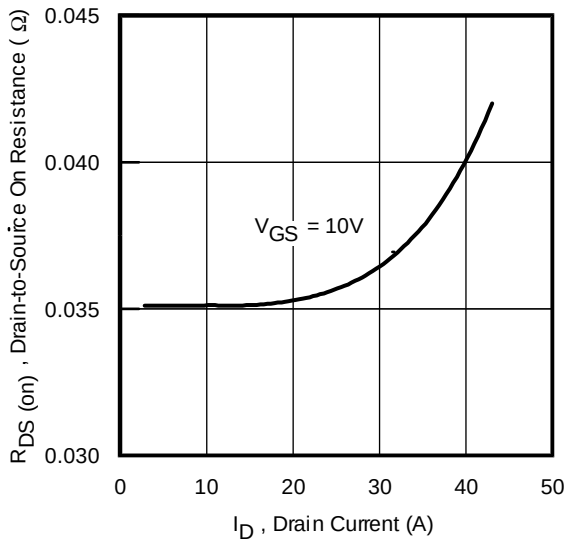


Fig 12. On-Resistance Vs. Drain Current

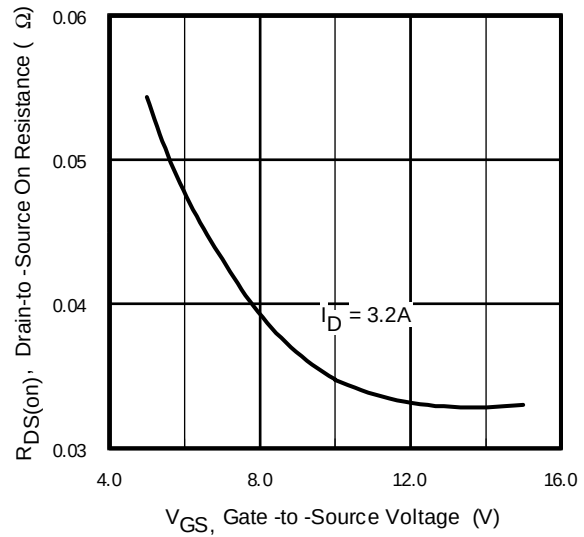


Fig 13. On-Resistance Vs. Gate Voltage

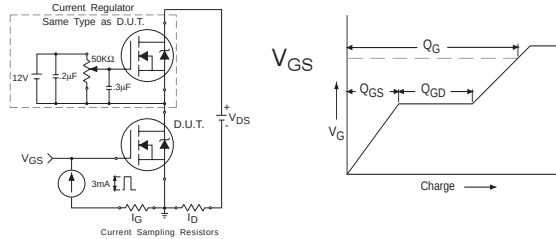


Fig 14a&b. Basic Gate Charge Test Circuit and Waveform

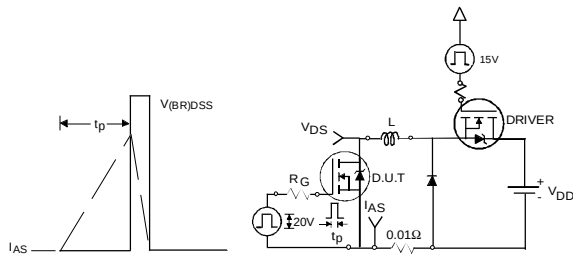


Fig 15a&b. Unclamped Inductive Test circuit and Waveforms

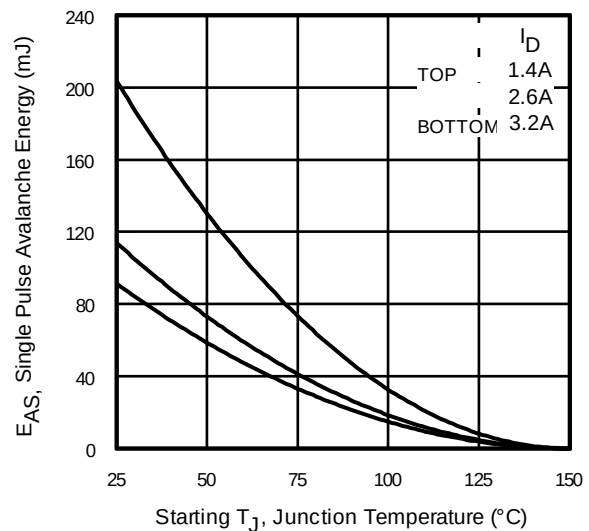


Fig 15c. Maximum Avalanche Energy Vs. Drain Current

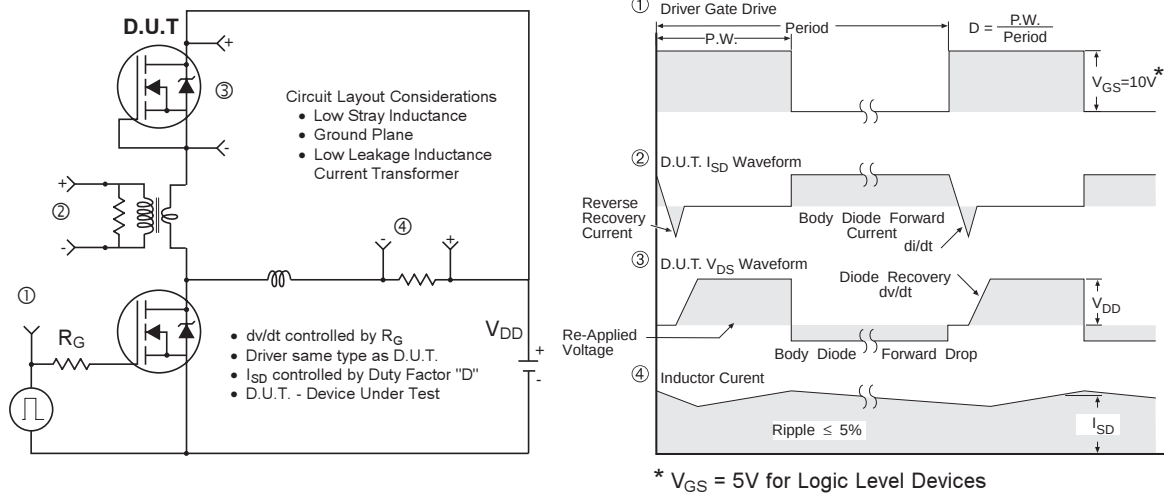


Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

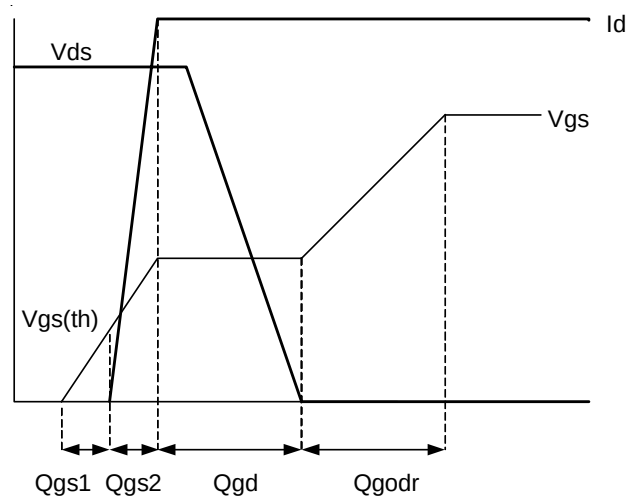
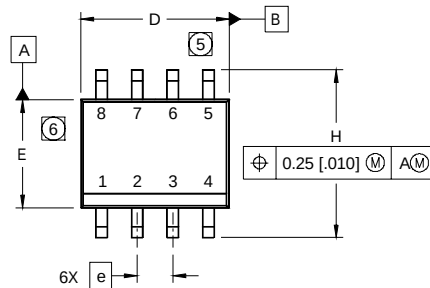


Fig 17. Gate Charge Waveform

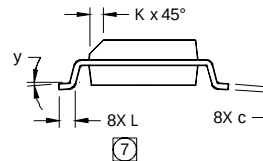
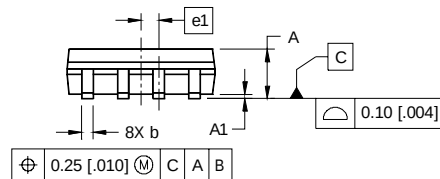
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SO-8 Package Outline



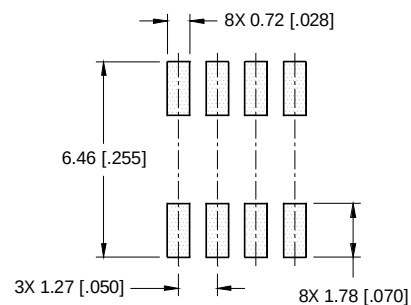
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



NOTES:

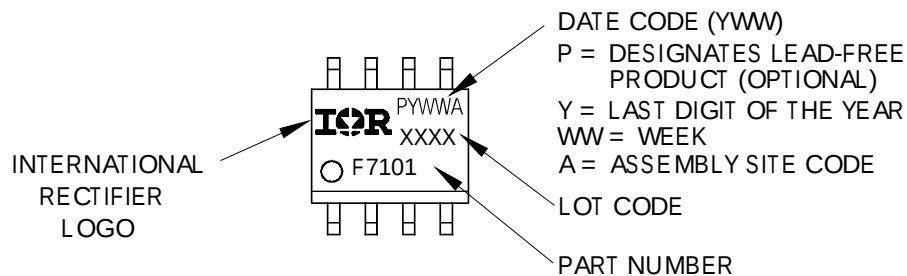
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
- ⑤ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
- ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
- ⑦ DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT

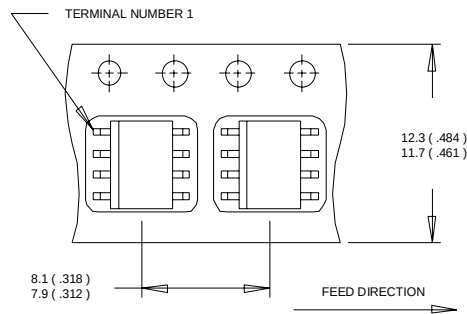


SO-8 Part Marking

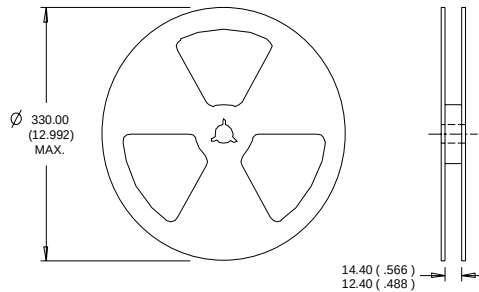
EXAMPLE: THIS IS AN IRF7101 (MOSFET)



SO-8 Tape and Reel



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
 2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 17\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 3.2\text{A}$.
- ③ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ When mounted on 1 inch square copper board
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualifications Standards can be found on IR's Web site.