

IRFB42N20DPbF

HEXFET® Power MOSFET

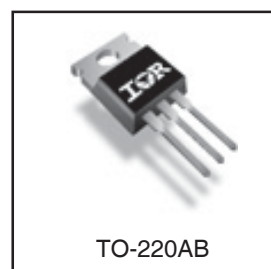
Applications

- High frequency DC-DC converters
- Motor Control
- Uninterruptible Power Supplies
- Lead-Free

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current

V_{DSS}	$R_{DS(on)}$ max	I_D
200V	0.055 Ω	44A



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	44	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	31	
I_{DM}	Pulsed Drain Current ①	180	
P_D @ $T_A = 25^\circ\text{C}$	Power Dissipation	2.4	W
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	330	
	Linear Derating Factor	2.2	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	2.5	V/ns
T_J	Operating Junction and	-55 to + 175	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.45	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

Notes ① through ⑤ are on page 8

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.26	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.055	Ω	$V_{GS} = 10V, I_D = 26A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 160V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

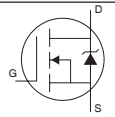
Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	21	—	—	S	$V_{DS} = 50V, I_D = 26A$
Q_g	Total Gate Charge	—	91	140	nC	$I_D = 26A$
Q_{gs}	Gate-to-Source Charge	—	24	36		$V_{DS} = 160V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	43	65		$V_{GS} = 10V,$
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	$V_{DD} = 100V$
t_r	Rise Time	—	69	—		$I_D = 26A$
$t_{d(off)}$	Turn-Off Delay Time	—	29	—		$R_G = 1.8\Omega$
t_f	Fall Time	—	32	—		$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	3430	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	530	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	100	—		$f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	5310	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	210	—		$V_{GS} = 0V, V_{DS} = 160V, f = 1.0\text{MHz}$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	400	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 160V$ ⑤

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	510	mJ
I_{AR}	Avalanche Current①	—	26	A
E_{AR}	Repetitive Avalanche Energy①	—	33	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	44	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	180		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 26A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	220	330	ns	$T_J = 25^\circ\text{C}, I_F = 26A$
Q_{rr}	Reverse Recovery Charge	—	1860	2790	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

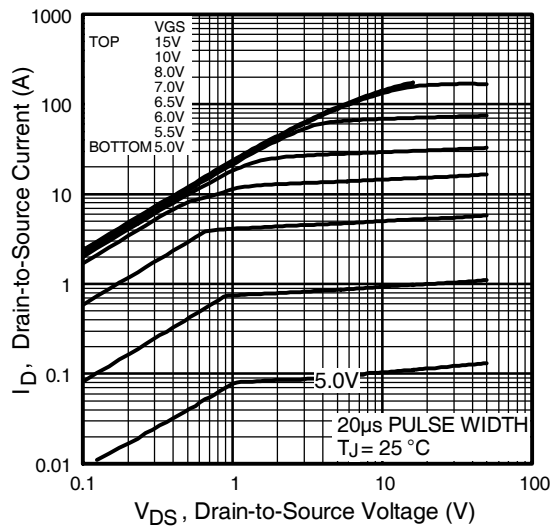


Fig 1. Typical Output Characteristics

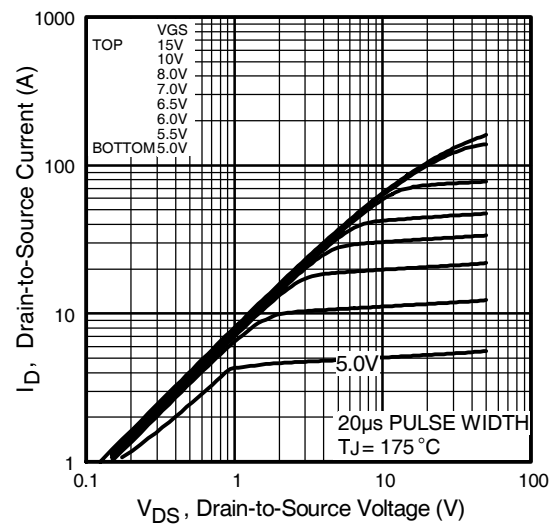


Fig 2. Typical Output Characteristics

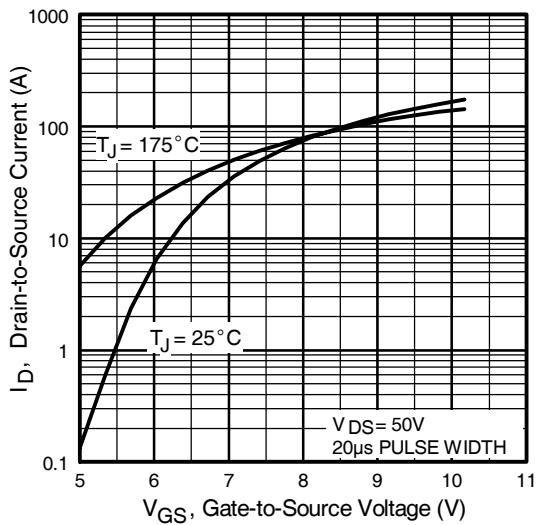


Fig 3. Typical Transfer Characteristics

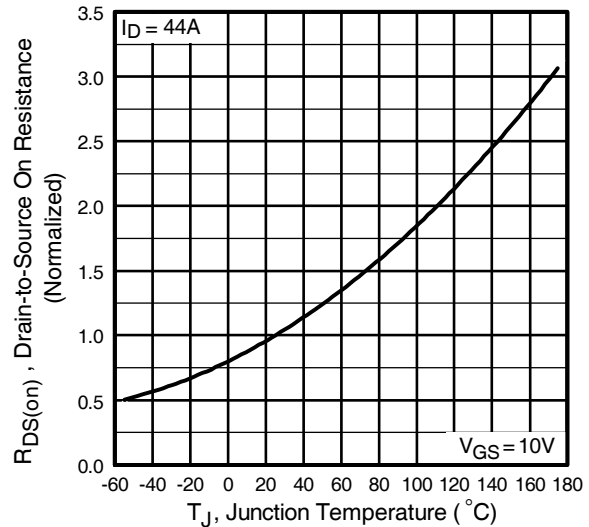


Fig 4. Normalized On-Resistance Vs. Temperature

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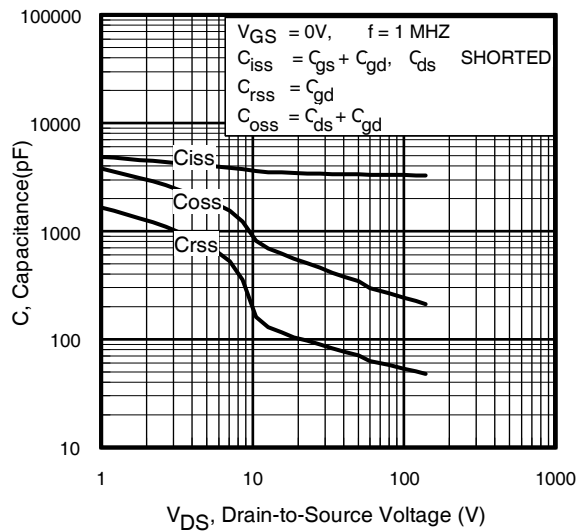


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

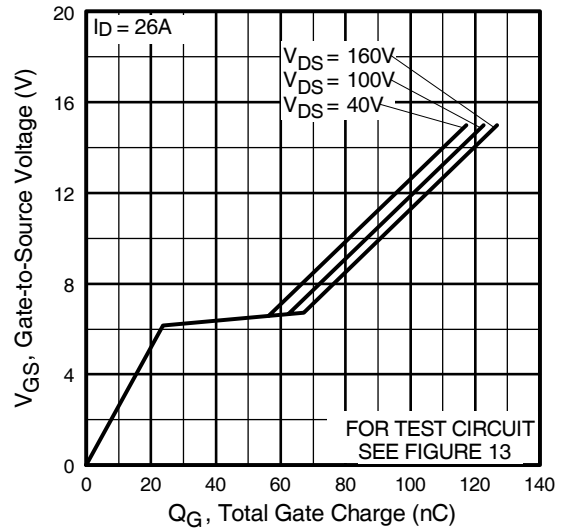


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

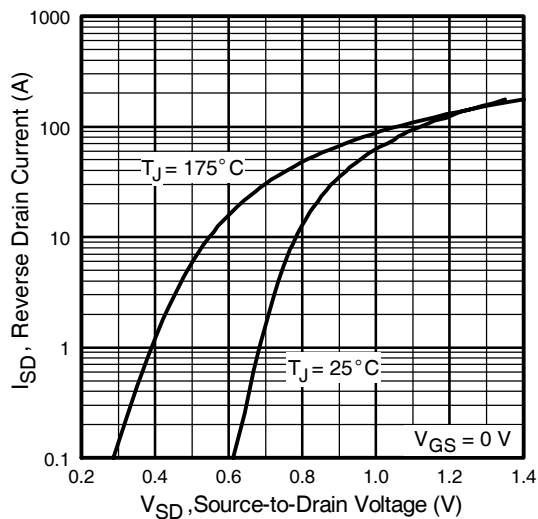


Fig 7. Typical Source-Drain Diode Forward Voltage

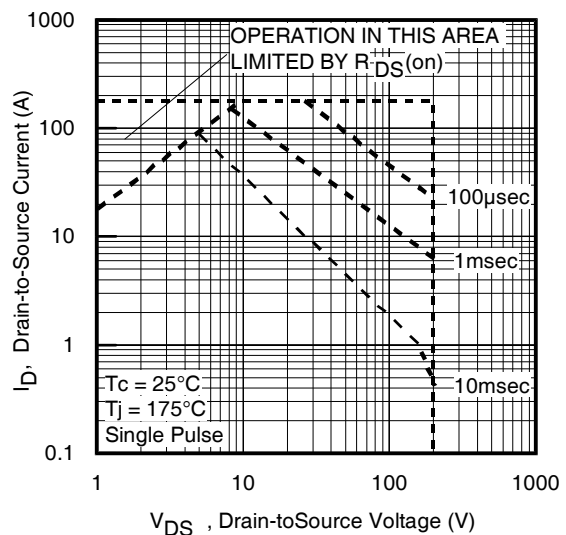


Fig 8. Maximum Safe Operating Area

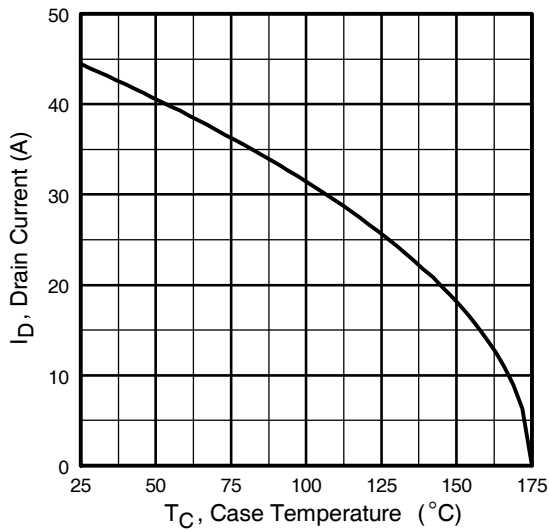


Fig 9. Maximum Drain Current Vs. Case Temperature

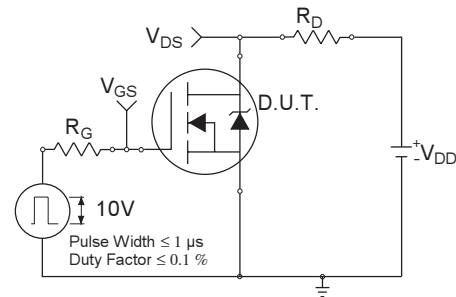


Fig 10a. Switching Time Test Circuit

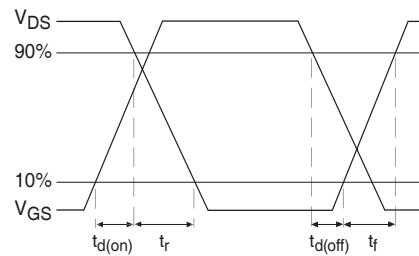


Fig 10b. Switching Time Waveforms

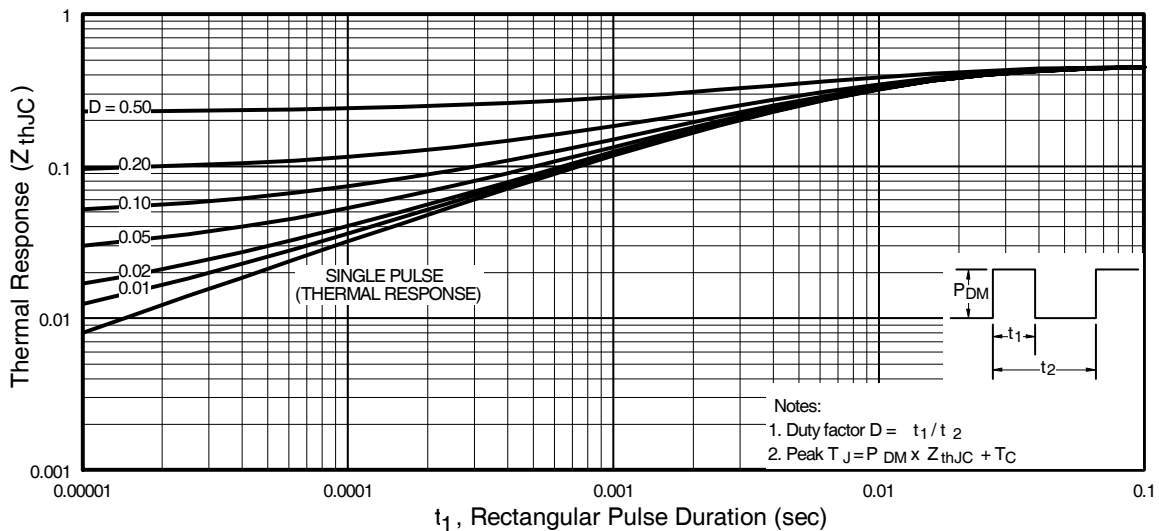


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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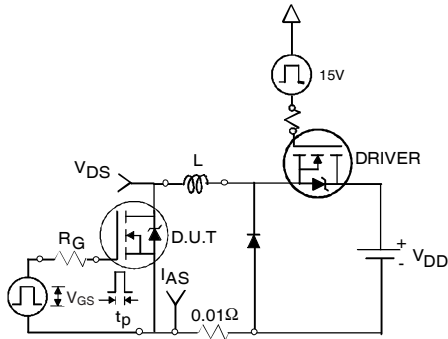


Fig 12a. Unclamped Inductive Test Circuit



Fig 12b. Unclamped Inductive Waveforms

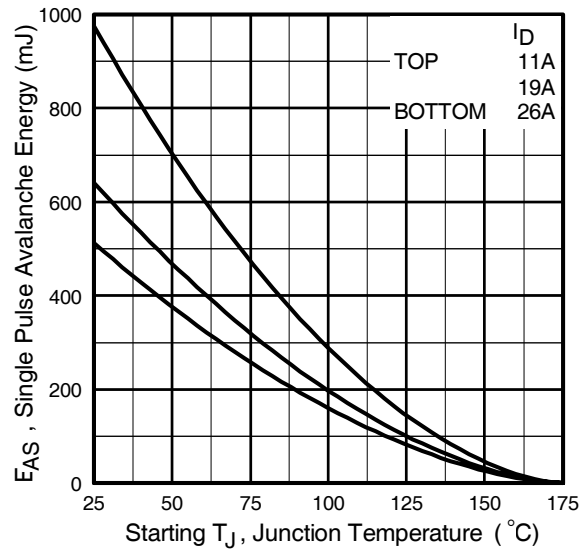


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

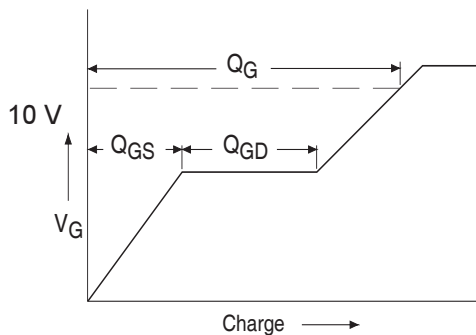


Fig 13a. Basic Gate Charge Waveform



Fig 13b. Gate Charge Test Circuit

The diagram shows a Class D amplifier circuit. At the bottom left, a square wave pulse generator (1) is connected to the gate of a driver MOSFET through a gate resistor R_G . The driver MOSFET's source is grounded, and its drain is connected to the source of a load MOSFET. The load MOSFET's gate is driven by a transformer-coupled driver (2). The load MOSFET's drain is connected to the D.U.T. (3) through an inductor. The D.U.T. is represented by a circle containing a diode-OR gate symbol. Its source is grounded, and its drain is connected to a load network (4) consisting of an inductor, a resistor, and a capacitor in parallel. The output of the load network is connected to a DC supply V_{DD} .

Circuit Layout Considerations

- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance

Current Transformer

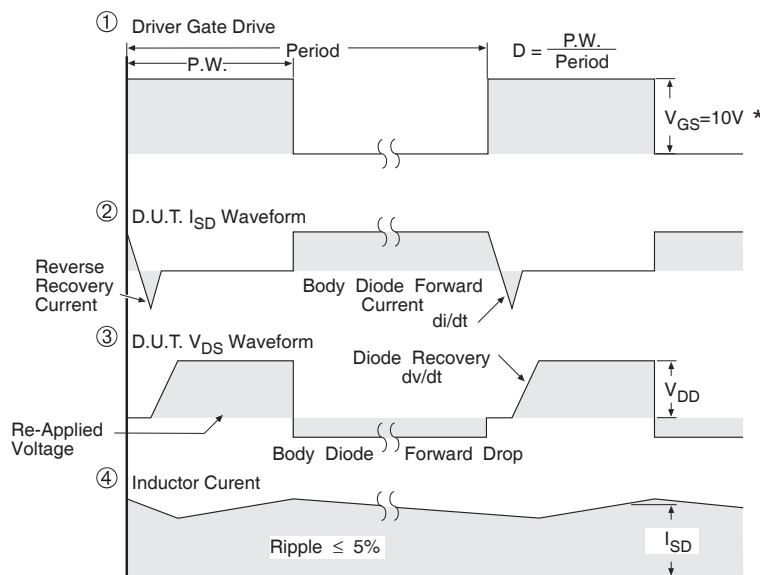
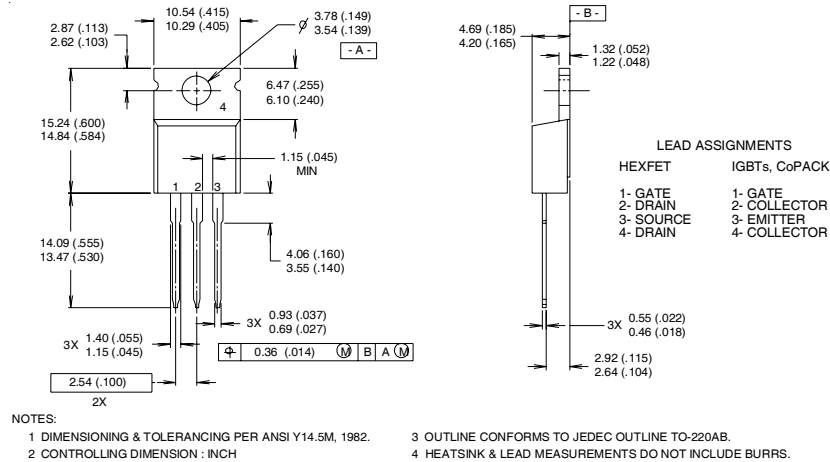


Fig 14. For N-Channel HEXFET® Power MOSFETs

IRFB42N20DPbF

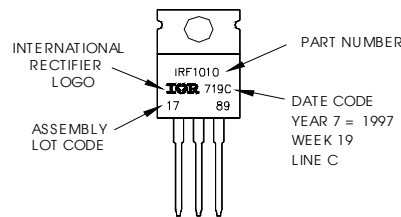
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TO-220AB Package Outline



TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"
Note: "P" in assembly line
position indicates "Lead-Free"



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 1.45\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 26\text{A}$, $V_{GS} = 10\text{V}$
- ③ $I_{SD} \leq 26\text{A}$, $di/dt \leq 110\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>