8-PIN SYNCHRONOUS PWM CONTROLLER

FEATURES

- Synchronous Controller in 8-Pin Package
- Operating with single 5V or 12V supply voltage
- Internal 200KHz Oscillator (400KHz for APU3037A)
- Soft-Start Function
- Fixed Frequency Voltage Mode
- 500mA Peak Output Drive Capability
- Protects the output when control FET is shorted
- RoHS Compliant & Halogen-Free Product

APPLICATIONS

- DDR memory source sink Vtt application
- Low cost on-board DC to DC such as 5V to 3.3V, 2.5V or 1.8V
- Graphic Card
- Hard Disk Drive

DESCRIPTION

The APU3037 controller IC is designed to provide a low cost synchronous Buck regulator for on-board DC to DC converter applications. With the migration of today's ASIC products requiring low supply voltages such as 1.8V and lower, together with currents in excess of 3A, traditional linear regulators are simply too lossy to be used when input supply is 5V or even in some cases with 3.3V input supply. The APU3037 together with dual N-channel MOSFETs such as AP60T03, provide a low cost solution for such applications. This device features an internal 200KHz oscillator (400KHz for "A" version), under-voltage lockout for both Vcc and Vc supplies, an external programmable soft-start function as well as output under-voltage detection that latches off the device when an output short is detected.

TYPICAL APPLICATION

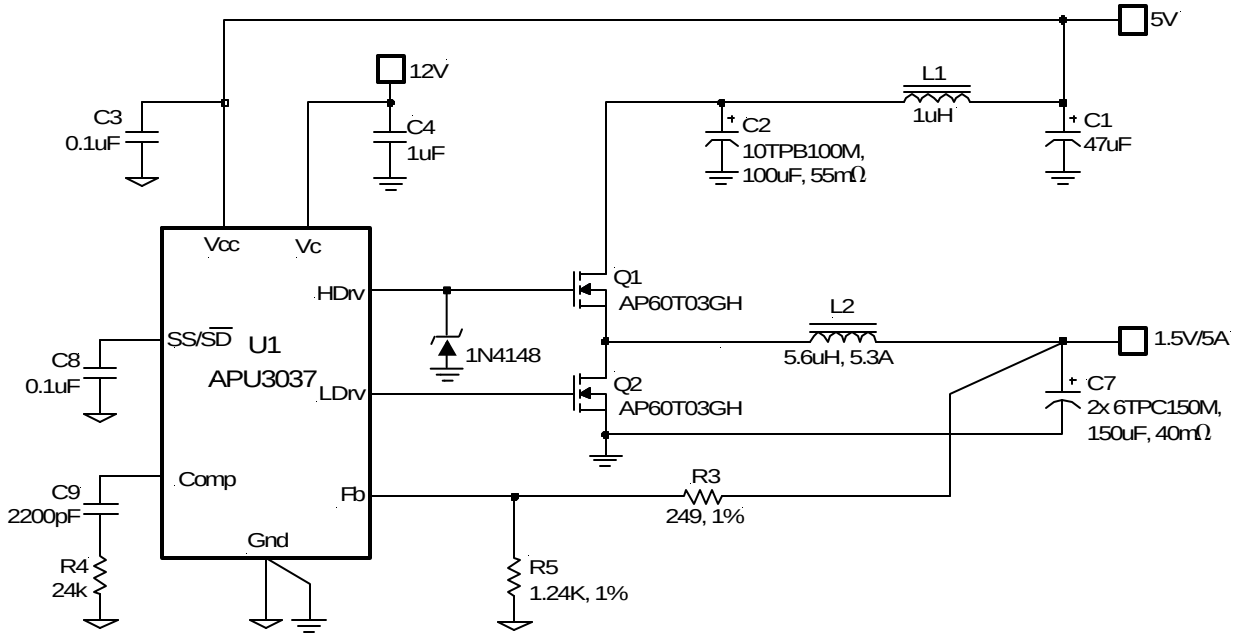


Figure 1 - Typical application of APU3037 or APU3037A.

PACKAGE ORDER INFORMATION

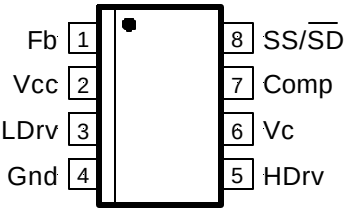
T_A (°C)	DEVICE	PACKAGE	FREQUENCY
0 To 70	APU3037O-HF	8-Pin Plastic TSSOP (O)	200KHz
0 To 70	APU3037M/MP-HF	8-Pin Plastic SOIC NB (M/MP)	200KHz
0 To 70	APU3037AO-HF	8-Pin Plastic TSSOP (O)	400KHz
0 To 70	APU3037AM/AMP-HF	8-Pin Plastic SOIC NB (M/MP)	400KHz

ABSOLUTE MAXIMUM RATINGS

Vcc Supply Voltage 25V
Vc Supply Voltage ..... 30V (not rated for inductive load)
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device.

PACKAGE INFORMATION

8-PIN PLASTIC TSSOP (O)	8-PIN PLASTIC SOIC (M/MP)
 θ_{JC}=42℃/W θ_{JA}=124℃/W	 θ_{JC}=45℃/W θ_{JA}=160°C/W without exposed pad (M) θ_{JC}=15℃/W θ_{JA}=80°C/W with exposed pad (MP)

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc=5V, Vc=12V and T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage						
Fb Voltage	V_{FB}	APU3037	1.225	1.250	1.275	
		APU3037A	0.784	0.800	0.816	V
Fb Voltage Line Regulation	L_{REG}	5<Vcc<12		0.2	0.35	%
UVLO						
UVLO Threshold - Vcc	UVLO Vcc	Supply Ramping Up	4.0	4.2	4.4	V
UVLO Hysteresis - Vcc				0.25		V
UVLO Threshold - Vc	UVLO Vc	Supply Ramping Up	3.1	3.3	3.5	V
UVLO Hysteresis - Vc				0.2		V
UVLO Threshold - Fb	UVLO Fb	Fb Ramping Down (APU3037)	0.4	0.6	0.8	V
		(APU3037A)	0.3	0.4	0.5	
UVLO Hysteresis - Fb				0.1		V
Supply Current						
Vcc Dynamic Supply Current	Dyn Icc	Freq=200KHz, C_L=1500pF	2	5	8	mA
Vc Dynamic Supply Current	Dyn Ic	Freq=200KHz, C_L=1500pF	2	7	10	mA
Vcc Static Supply Current	I_{CCQ}	SS=0V	1	3.3	6	mA
Vc Static Supply Current	I_{CQ}	SS=0V	0.5	1	4.5	mA
Soft-Start Section						
Charge Current	SS_{IB}	SS=0V	-10	-20	-30	μA

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Error Amp						
Fb Voltage Input Bias Current	I_{FB1}	SS=3V, Fb=1V		-0.1		μA
Fb Voltage Input Bias Current	I_{FB2}	SS=0V, Fb=1V		-64		μA
Transconductance	gm		450	600	750	μmho
Oscillator						
Frequency	Freq	APU3037	180	200	220	KHz
		APU3037A	360	400	440	
Ramp-Amplitude Voltage	V_{RAMP}		1.225	1.25	1.275	V
Output Drivers						
Rise Time	T_r	C_L=1500pF		50	100	ns
Fall Time	T_f	C_L=1500pF		50	100	ns
Dead Band Time	T_{DB}		50	150	250	ns
Max Duty Cycle	T_{ON}	Fb=1V, Freq=200KHz	85	90	95	%
Min Duty Cycle	T_{OFF}	Fb=1.5V	0	0		%

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Fb	This pin is connected directly to the output of the switching regulator via resistor divider to provide feedback to the Error amplifier.
2	Vcc	This pin provides biasing for the internal blocks of the IC as well as power for the low side driver. A minimum of 1μF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
3	LDrv	Output driver for the synchronous power MOSFET.
4	Gnd	This pin serves as the ground pin and must be connected directly to the ground plane. A high frequency capacitor (0.1 to 1μF) must be connected from V5 and V12 pins to this pin for noise free operation.
5	HDrv	Output driver for the high side power MOSFET. Connect a diode, such as BAT54 or 1N4148, from this pin to ground for the application when the inductor current goes negative (Source/ Sink), soft-start at no load and for the fast load transient from full load to no load.
6	Vc	This pin is connected to a voltage that must be at least 4V higher than the bus voltage of the switcher (assuming 5V threshold MOSFET) and powers the high side output driver. A minimum of 1μF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
7	Comp	Compensation pin of the error amplifier. An external resistor and capacitor network is typically connected from this pin to ground to provide loop compensation.
8	SS / $\overline{SD}$	This pin provides soft-start for the switching regulator. An internal current source charges an external capacitor that is connected from this pin to ground which ramps up the output of the switching regulator, preventing it from overshooting as well as limiting the input current. The converter can be shutdown by pulling this pin below 0.5V.

BLOCK DIAGRAM

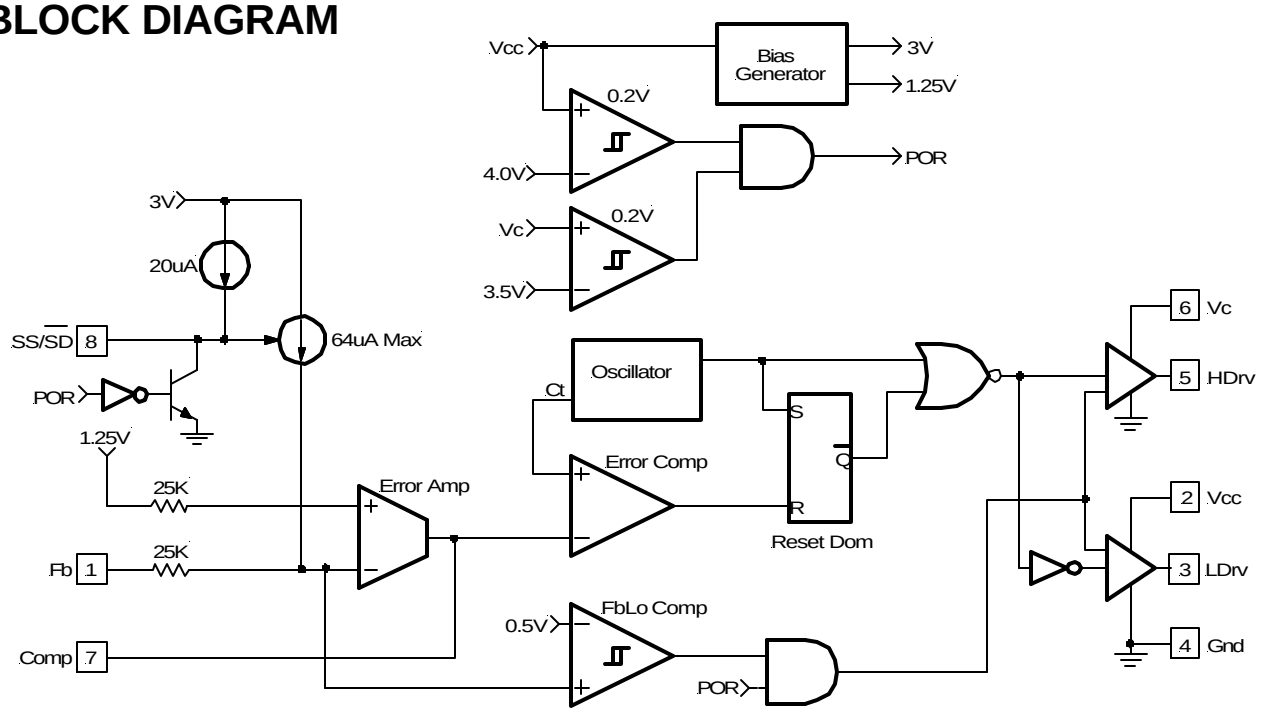


Figure 2 - Simplified block diagram of the APU3037.

THEORY OF OPERATION

Introduction

The APU3037 is a fixed frequency, voltage mode synchronous controller and consists of a precision reference voltage, an error amplifier, an internal oscillator, a PWM comparator, 0.5A peak gate driver, soft-start and shutdown circuits (see Block Diagram).

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier; this is the amplified error signal from the sensed output voltage and the reference voltage.

This voltage is compared to a fixed frequency linear sawtooth ramp and generates fixed frequency pulses of variable duty-cycle, which drives the two N-channel external MOSFETs.The timing of the IC is provided through an internal oscillator circuit which uses on-chip capacitor to set the oscillation frequency to 200 KHz (400 KHz for “A” version).

Soft-Start

The APU3037 has a programmable soft-start to control the output voltage rise and limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Vc and Vcc rise above their threshold (3.3V and 4.2V respectively) and generates the Power On Reset (POR) signal. Soft-start function operates by sourcing an internal current to charge an external capacitor to about 3V. Initially, the soft-start function clamps the E/A’s output of the PWM converter. As the charging voltage of the external capacitor ramps up, the PWM signals increase from zero to the point the feedback loop takes control.

Short-Circuit Protection

The outputs are protected against the short-circuit. The APU3037 protects the circuit for shorted output by sensing the output voltage (through the external resistor divider). The APU3037 shuts down the PWM signals, when the Fb voltage drops below 0.6V (0.4V for APU3037A).

The APU3037 also protects the output from over-voltaging when the control FET is shorted. This is done by turning on the sync FET with the maximum duty cycle.

Under-Voltage Lockout

The under-voltage lockout circuit assures that the MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if Vc and Vcc fall below 3.3V and 4.2V respectively. Normal operation resumes once Vc and Vcc rise above the set values.

APPLICATION INFORMATION

Design Example:

The following example is a typical application for APU3037, the schematic is Figure 18 on page 14.

V_{IN} = 5V
V_{OUT} = 3.3V
I_{OUT} = 4A
ΔV_{OUT} = 100mV
f_S = 200KHz

Output Voltage Programming

Output voltage is programmed by reference voltage and external voltage divider. The Fb pin is the inverting input of the error amplifier, which is internally referenced to 1.25V (0.8V for APU3037A). The divider is ratioed to provide 1.25V at the Fb pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_6}{R_5}\right) \qquad ---(1)$$

When an external resistor divider is connected to the output as shown in Figure 3.

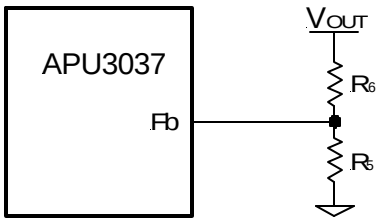


Figure 3 - Typical application of the APU3037 for programming the output voltage.

Equation (1) can be rewritten as:

$$R_6 = R_5 \times \left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

Choose R_5 = 1KΩ
This will result to R_6 = 1.65KΩ

If the high value feedback resistors are used, the input bias current of the Fb pin could cause a slight increase in output voltage. The output voltage set point can be more accurate by using precision resistor.

Soft-Start Programming

The soft-start timing can be programmed by selecting the soft start capacitance value. The start up time of the converter can be calculated by using:

$$t_{START} = 75 \times Css \quad (ms) \qquad ---(2)$$

Where:
C_{SS} is the soft-start capacitor (μF)

For a start-up time of 7.5ms, the soft-start capacitor will be 0.1μF. Choose a ceramic capacitor at 0.1μF.

Shutdown

The converter can be shutdown by pulling the soft-start pin below 0.5V. The control MOSFET turns off and the synchronous MOSFET turns on during shutdown.

Boost Supply Vc

To drive the high-side switch it is necessary to supply a gate voltage at least 4V greater than the bus voltage. This is achieved by using a charge pump configuration as shown in Figure 18. The capacitor is charged up to approximately twice the bus voltage. A capacitor in the range of 0.1μF to 1μF is generally adequate for most applications. In application, when a separate voltage source is available the boost circuit can be avoided as shown in Figure 1.

Input Capacitor Selection

The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The larger capacitor, the less ripple expected but consider should be taken for the higher surge current during the power-up. The APU3037 provides the soft-start function which controls and limits the current surge. The value of the input capacitor can be calculated by the following formula:

$$C_{IN} = \frac{I_{IN} \times \Delta t}{\Delta V} \qquad ---(3)$$

Where:
C_{IN} is the input capacitance (μF)
I_{IN} is the input current (A)
Δt is the turn on time of the high-side switch (μs)
ΔV is the allowable peak to peak voltage ripple (V)

Assuming the following:

$\Delta V = 1\%(V_{IN})$, Efficiency(η) = 90%

$$\Delta t = D \times \frac{1}{f_S} \rightarrow \Delta t = 3.3\mu s$$

$$I_{IN} = \frac{V_O \times I_O}{\eta \times V_{IN}} \rightarrow I_{IN} = 2.93A$$

By using equation (3), $C_{IN} = 193.3\mu F$
For higher efficiency, low ESR capacitor is recommended. Choose two 100μF capacitors.

The Sanyo TPB series PosCap capacitor 100μF, 10V with 55mΩ ESR is a good choice.

Output Capacitor Selection

The criteria to select the output capacitor is normally based on the value of the Effective Series Resistance (ESR). In general, the output capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements. The ESR of the output capacitor is calculated by the following relationship:

$$ESR \leq \frac{\Delta V_O}{\Delta I_O} \qquad ---(4)$$

Where:
ΔV_O = Output Voltage Ripple
ΔI_O = Output Current
ΔV_O=100mV and ΔI_O=4A
Results to ESR=25mΩ

The Sanyo TPC series, PosCap capacitor is a good choice. The 6TPC150M 150μF, 6.3V has an ESR 40mΩ. Selecting two of these capacitors in parallel, results to an ESR of ≅ 20mΩ which achieves our low ESR goal.

The capacitor value must be high enough to absorb the inductor's ripple current. The larger the value of capacitor, the lower will be the output ripple voltage.

Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. Low inductor value causes large ripple current, resulting in the smaller size, but poor efficiency and high output noise. Generally, the selection of inductor value can be reduced to desired maximum ripple current in the inductor (Δi). The optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{IN} - V_{OUT} = L \times \frac{\Delta i}{\Delta t} \; ; \; \Delta t = D \times \frac{1}{f_S} \; ; \; D = \frac{V_{OUT}}{V_{IN}}$$

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times \Delta i \times f_S} \qquad ---(5)$$

Where:
V_{IN} = Maximum Input Voltage
V_{OUT} = Output Voltage
Δi = Inductor Ripple Current
f_S = Switching Frequency
Δt = Turn On Time
D = Duty Cycle

If $\Delta i = 20\%(I_O)$, then the output inductor will be:

$L = 7\mu H$

The Toko D124C series provides a range of inductors in different values, low profile suitable for large currents, 10μH, 4.2A is a good choice for this application. This will result to a ripple approximately 14% of output current.

Power MOSFET Selection

The APU3037 uses two N-Channel MOSFETs. The selections criteria to meet power transfer requirements is based on maximum drain-source voltage (V_{DSS}), gate-source drive voltage (V_{GS}), maximum output current, On-resistance $R_{DS(ON)}$ and thermal management.

The MOSFET must have a maximum operating voltage (V_{DSS}) exceeding the maximum input voltage (V_{IN}).

The gate drive requirement is almost the same for both MOSFETs. Logic-level transistor can be used and caution should be taken with devices at very low V_{GS} to prevent undesired turn-on of the complementary MOSFET, which results a shoot-through current.

The total power dissipation for MOSFETs includes conduction and switching losses. For the Buck converter the average inductor current is equal to the DC load current. The conduction loss is defined as:

$$P_{COND} \text{ (Upper Switch)} = I^2_{LOAD} \times R_{DS(ON)} \times D \times \vartheta$$

$$P_{COND} \text{ (Lower Switch)} = I^2_{LOAD} \times R_{DS(ON)} \times (1 - D) \times \vartheta$$

ϑ = $R_{DS(ON)}$ Temperature Dependency

The $R_{DS(ON)}$ temperature dependency should be considered for the worst case operation. This is typically given in the MOSFET data sheet. Ensure that the conduction losses and switching losses do not exceed the package ratings or violate the overall thermal budget.

For this design, AP60T03GH is a good choice. The device provides low on-resistance in a TO-252 package.

The AP60T03GH has the following data:

V_{DSS} = 30V
I_D = 4.5A
$R_{DS(ON)}$ = 0.012Ω

The total conduction losses will be:

$P_{CON(TOTAL)}=P_{CON}$(Upper Switch)+P_{CON}(Lower Switch)

$P_{CON(TOTAL)} = I^2_{LOAD} \times R_{DS(ON)} \times \vartheta$

ϑ = 1.5 according to the AP60T03GH data sheet for 150°C junction temperature

$P_{CON(TOTAL)}$ = 0.288W

The switching loss is more difficult to calculate, even though the switching transition is well understood. The reason is the effect of the parasitic components and switching times during the switching procedures such as turn-on / turnoff delays and rise and fall times. With a linear approximation, the total switching loss can be expressed as:

$$P_{SW} = \frac{V_{DS(OFF)}}{2} \times \frac{t_r + t_f}{T} \times I_{LOAD} \quad \text{---(6)}$$

Where:
$V_{DS(OFF)}$ = Drain to Source Voltage at off time
t_r = Rise Time
t_f = Fall Time
T = Switching Period
I_{LOAD} = Load Current

The switching time waveform is shown in figure 4.

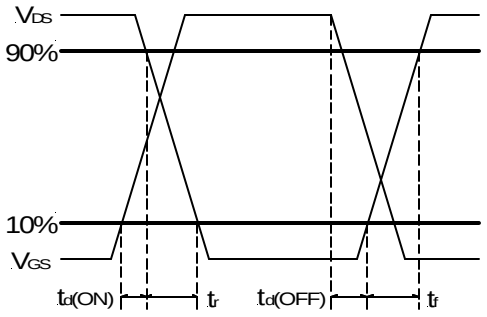


Figure 4 - Switching time waveforms.

From AP60T03GH data sheet we obtain:

t_r = 57.5ns
t_f = 6.4ns

These values are taken under a certain condition test. For more detail please refer to the AP60T03GH data sheet.

By using equation (6), we can calculate the switching losses.

P_{SW} = 0.127W

Feedback Compensation

The APU3037 is a voltage mode controller; the control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin (greater than 45°).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180° (see Figure 5). The Resonant frequency of the LC filter expressed as follows:

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \quad \text{---(7)}$$

Figure 5 shows gain and phase of the LC filter. Since we already have 180° phase shift just from the output filter, the system risks being unstable.

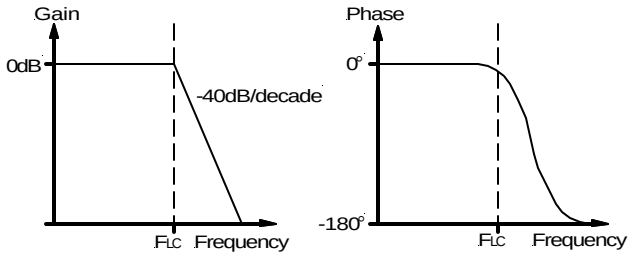


Figure 5 - Gain and phase of LC filter.

The APU3037's error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.

The E/A can be compensated with or without the use of local feedback. When operated without local feedback the transconductance properties of the E/A become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp pin to ground as shown in Figure 6.

Note that this method requires that the output capacitor should have enough ESR to satisfy stability requirements. In general the output capacitor's ESR generates a zero typically at 5KHz to 50KHz which is essential for an acceptable phase margin.

The ESR zero of the output capacitor expressed as follows:

$$F_{ESR} = \frac{1}{2\pi \times ESR \times Co} \quad ---(8)$$

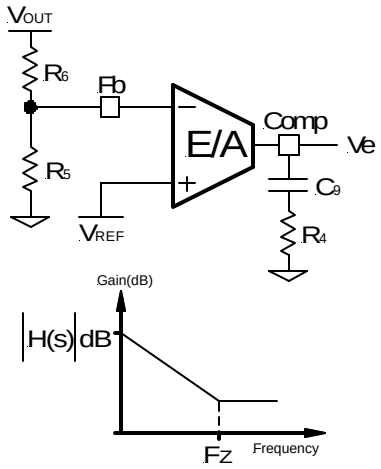


Figure 6 - Compensation network without local feedback and its asymptotic gain plot.

The transfer function (Ve / V_{OUT}) is given by:

$$H(s) = \left(g_m \times \frac{R_5}{R_6 + R_5}\right) \times \frac{1 + sR_4C_9}{sC_9} \quad ---(9)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s)| = g_m \times \frac{R_5}{R_6 \times R_5} \times R_4 \quad ---(10)$$

$$F_Z = \frac{1}{2\pi \times R_4 \times C_9} \quad ---(11)$$

The gain is determined by the voltage divider and E/A's transconductance gain.

First select the desired zero-crossover frequency (Fo):

$Fo > F_{ESR}$ and $F_O \leq (1/5 \sim 1/10) \times f_S$

Use the following equation to calculate R_4:

$$R_4 = \frac{V_{OSC}}{V_{IN}} \times \frac{Fo \times F_{ESR}}{F_{LC}^2} \times \frac{R_5 + R_6}{R_5} \times \frac{1}{g_m} \quad ---(12)$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
Fo = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
R_5 and R_6 = Resistor Dividers for Output Voltage Programming
g_m = Error Amplifier Transconductance

For:
V_{IN} = 5V
V_{OSC} = 1.25V
Fo = 30KHz
F_{ESR} = 26.52KHz
F_{LC} = 2.9KHz
R_5 = 1K
R_6 = 1.65K
g_m = 600μmho

This results to R_4=104.4KΩ. Choose R_4=105KΩ

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$F_Z \cong 75\% F_{LC}$

$$F_Z \cong 0.75 \times \frac{1}{2\pi\sqrt{L_O \times C_O}} \quad ---(13)$$

For:
Lo = 10μH
Co = 300μF
F_Z = 2.17KHz
R_4 = 86.6KΩ

Using equations (11) and (13) to calculate C_9, we get:

C_9 = 698pF
Choose C_9 = 680pF

One more capacitor is sometimes added in parallel with C_9 and R_4. This introduces one more pole which is mainly used to supress the switching noise. The additional pole is given by:

$$F_P = \frac{1}{2\pi \times R_4 \times \frac{C_9 \times C_{POLE}}{C_9 + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi \times R_4 \times f_S - \frac{1}{C_9}} \cong \frac{1}{\pi \times R_4 \times f_S}$$

for $F_P << \frac{f_S}{2}$

For a general solution for unconditionally stability for any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network. The typically used compensation network for voltage-mode controller is shown in Figure 7.

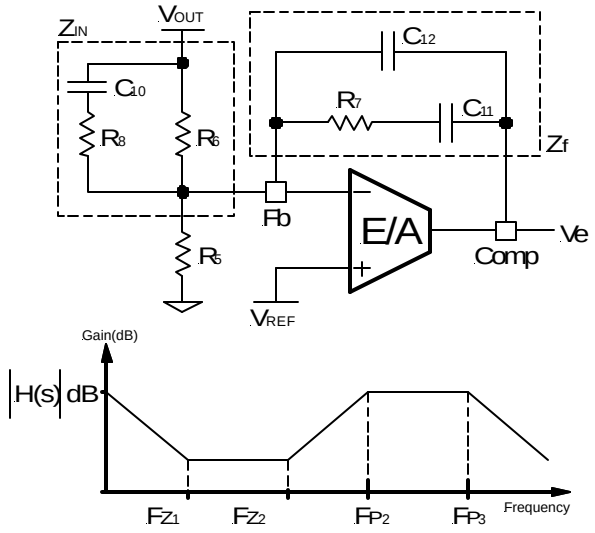


Figure 7 - Compensation network with local feedback and its asymptotic gain plot.

In such configuration, the transfer function is given by:

$$\frac{Ve}{V_{OUT}} = \frac{1 - g_m Z_f}{1 + g_m Z_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$$g_m Z_f >> 1 \quad \text{and} \quad g_m Z_{IN} >> 1 \qquad \text{---(14)}$$

By replacing Z_{IN} and Z_f according to Figure 7, the transformer function can be expressed as:

$$H(s) = \frac{1}{sR_6(C_{12}+C_{11})} \times \frac{(1+sR_7C_{11}) \times [1+sC_{10}(R_6+R_8)]}{\left[1+sR_7\left(\frac{C_{12} \times C_{11}}{C_{12}+C_{11}}\right)\right] \times (1+sR_8C_{10})}$$

As known, transconductance amplifier has high impedance (current source) output, therefore, consider should be taken when loading the E/A output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R_8 \times C_{10}}$$

$$F_{P3} = \frac{1}{2\pi \times R_7 \times \left(\frac{C_{12} \times C_{11}}{C_{12}+C_{11}}\right)} \cong \frac{1}{2\pi \times R_7 \times C_{12}}$$

$$F_{Z1} = \frac{1}{2\pi \times R_7 \times C_{11}}$$

$$F_{Z2} = \frac{1}{2\pi \times C_{10} \times (R_6 + R_8)} \cong \frac{1}{2\pi \times C_{10} \times R_6}$$

Cross Over Frequency:

$$F_O = R_7 \times C_{10} \times \frac{V_{IN}}{V_{OSC}} \times \frac{1}{2\pi \times Lo \times Co} \qquad \text{---(15)}$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
Lo = Output Inductor
Co = Total Output Capacitors

The stability requirement will be satisfied by placing the poles and zeros of the compensation network according to following design rules. The consideration has been taken to satisfy condition (14) regarding transconductance error amplifier.

1) Select the crossover frequency:
$F_O < F_{ESR}$ and $F_O \leq (1/10 \sim 1/6) \times f_S$

2) Select R_7, so that $R_7 >> \frac{2}{g_m}$

3) Place first zero before LC's resonant frequency pole.
$F_{Z1} \cong 75\% F_{LC}$

$$C_{11} = \frac{1}{2\pi \times F_{Z1} \times R_7}$$

4) Place third pole at the half of the switching frequency.

$$F_{P3} = \frac{f_S}{2}$$

$$C_{12} = \frac{1}{2\pi \times R_7 \times F_{P3}}$$

$C_{12} > 50pF$
If not, change R_7 selection.

5) Place R_7 in (15) and calculate C_{10}:

$$C_{10} \leq \frac{2\pi \times Lo \times Fo \times Co}{R_7} \times \frac{V_{OSC}}{V_{IN}}$$

6) Place second pole at the ESR zero.
$F_{P2} = F_{ESR}$

$$R_8 = \frac{1}{2\pi \times C_{10} \times F_{P2}}$$

Check if $R_8 > \frac{1}{gm}$

If R_8 is too small, increase R_7 and start from step 2.

7) Place second zero around the resonant frequency.
$F_{Z2} = F_{LC}$

$$R_6 = \frac{1}{2\pi \times C_{10} \times F_{Z2}} - R_8$$

8) Use equation (1) to calculate R_5.

$$R_5 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_6$$

These design rules will give a crossover frequency approximately one-tenth of the switching frequency. The higher the band width, the potentially faster the load transient speed. The gain margin will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than 45° for overall stability.

IC Quiescent Power Dissipation

Power dissipation for IC controller is a function of applied voltage, gate driver loads and switching frequency. The IC's maximum power dissipation occurs when the IC operating with single 12V supply voltage (Vcc=12V and Vc≅24V) at 400KHz switching frequency and maximum gate loads.

Figures 9 and 10 show voltage vs. current, when the gate drivers loaded with 470pF, 1150pF and 1540pF capacitors. The IC's power dissipation results to an excessive temperature rise. This should be considered when using APU3037A for such application.

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components, make all the connection in the top layer with wide, copper filled areas. The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET, to reduce the ESR replace the single input capacitor with two parallel units. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC. In multilayer PCB use one layer as power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

Figure 8 shows a suggested layout for the critical components, based on the schematic on page 14.

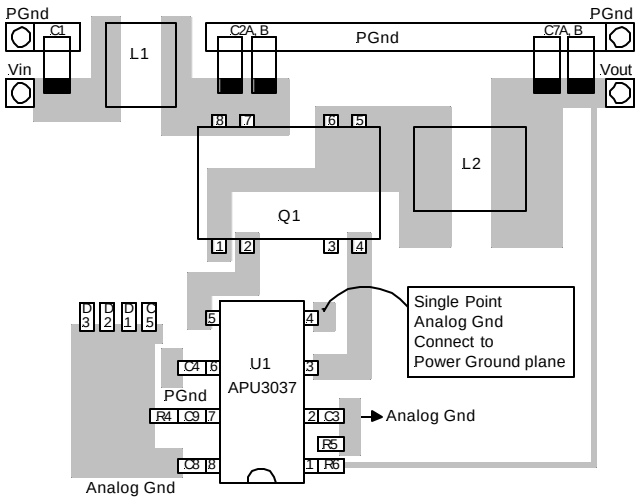


Figure 8 - Suggested layout.
(Topside shown only)

TYPICAL PERFORMANCE CHARACTERISTICS

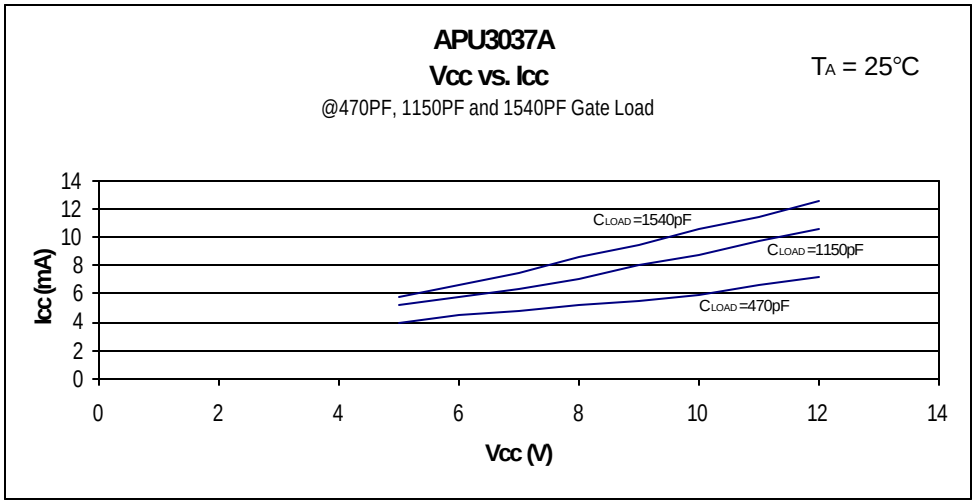


Figure 9 - Vcc vs. Icc

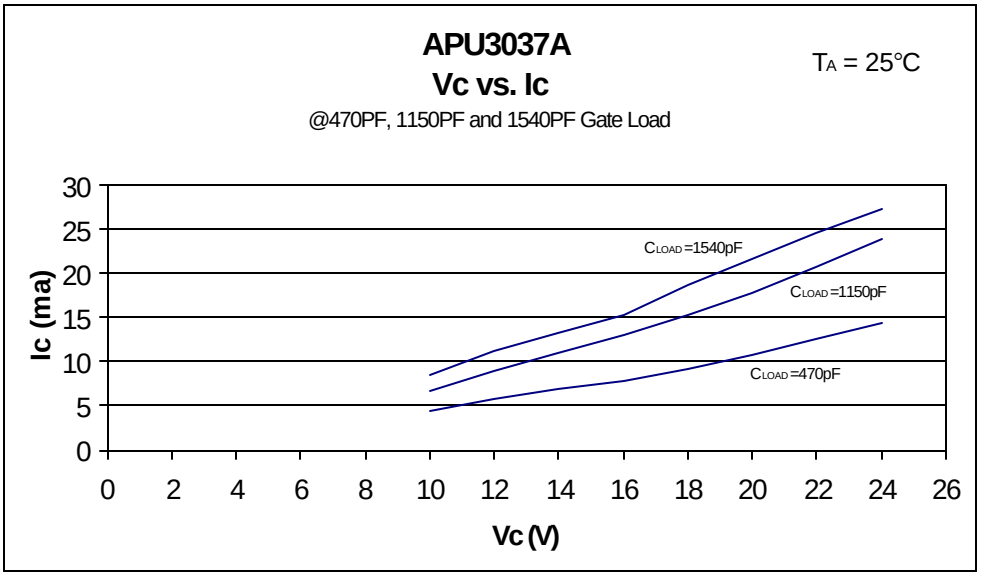


Figure 10 - Vc vs. Ic

TYPICAL PERFORMANCE CHARACTERISTICS

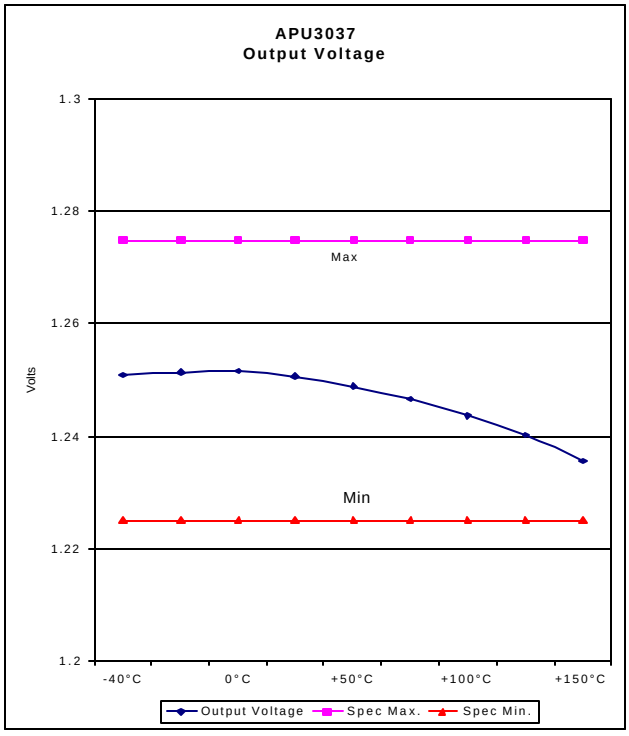


Figure 11 - Output Voltage

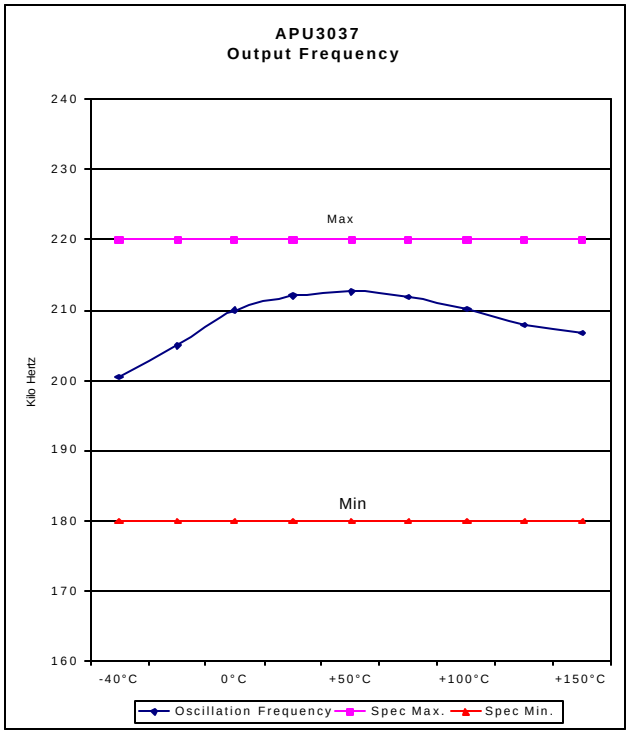


Figure 12 - Output Frequency

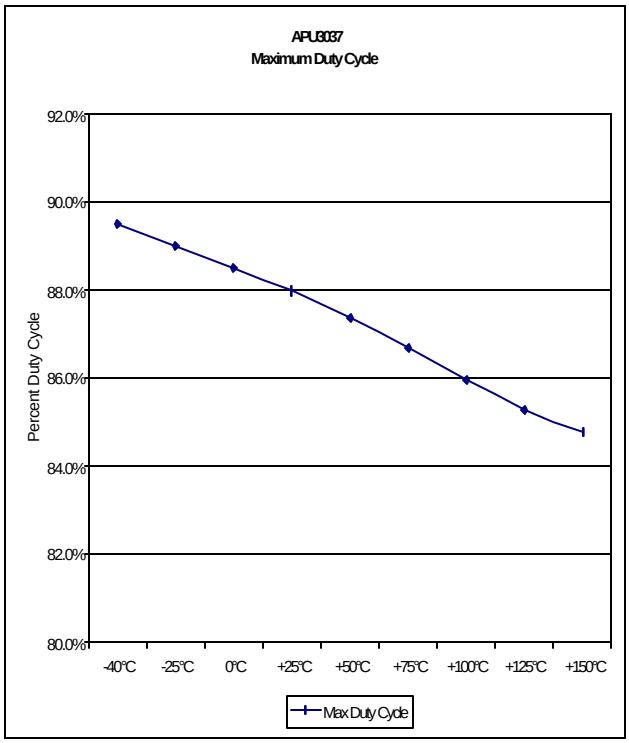


Figure 13 - Maximum Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS

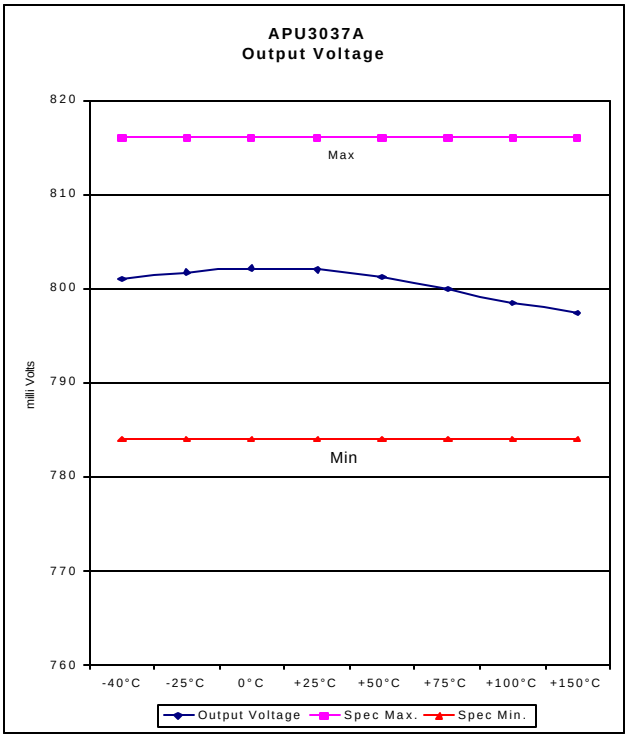


Figure 14 - Output Voltage

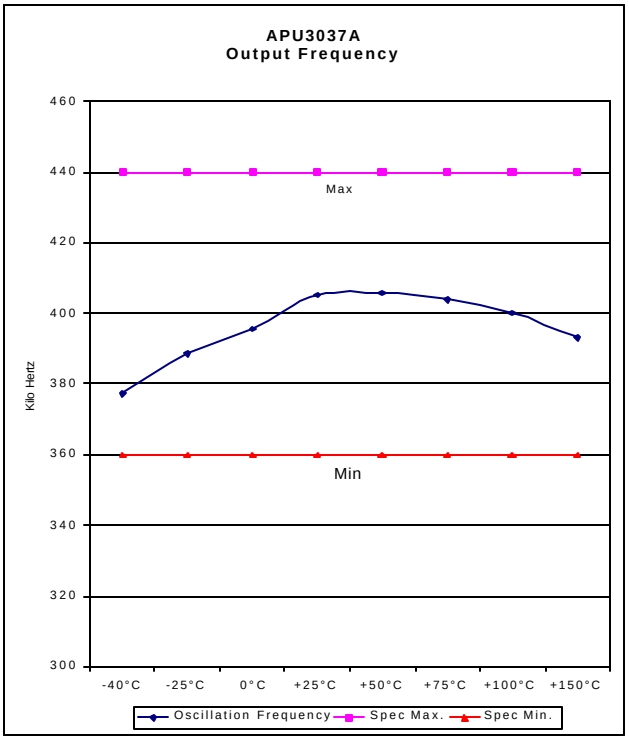


Figure 15 - Output Frequency

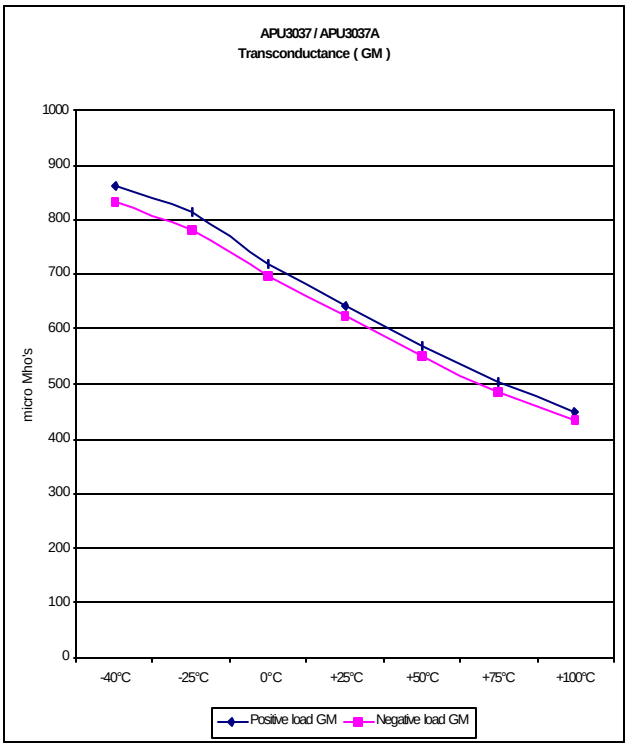


Figure 16 - Transconductance

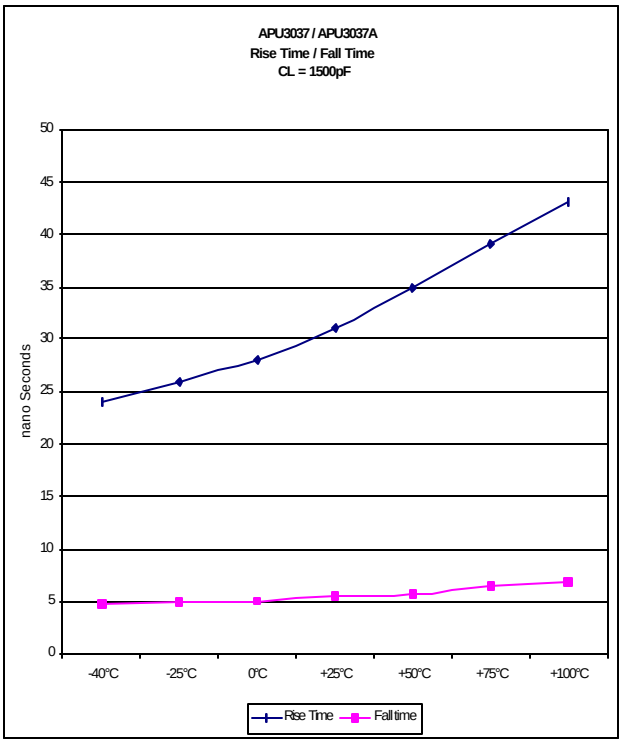


Figure 17 - Rise Time and Fall Time

TYPICAL APPLICATION

Single Supply 5V Input

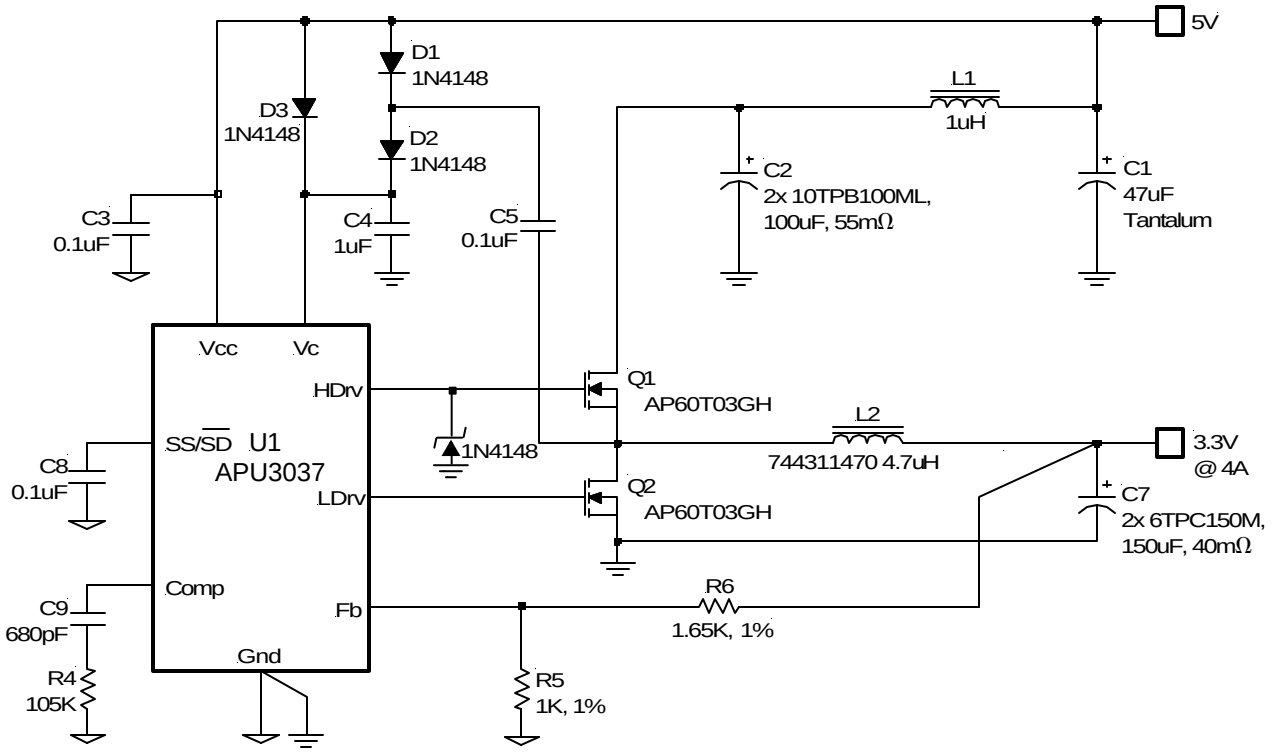


Figure 18 - Typical application of APU3037 in an on-board DC-DC converter using a single 5V supply.

TYPICAL APPLICATION

Dual Supply, 5V Bus and 12V Bias Input

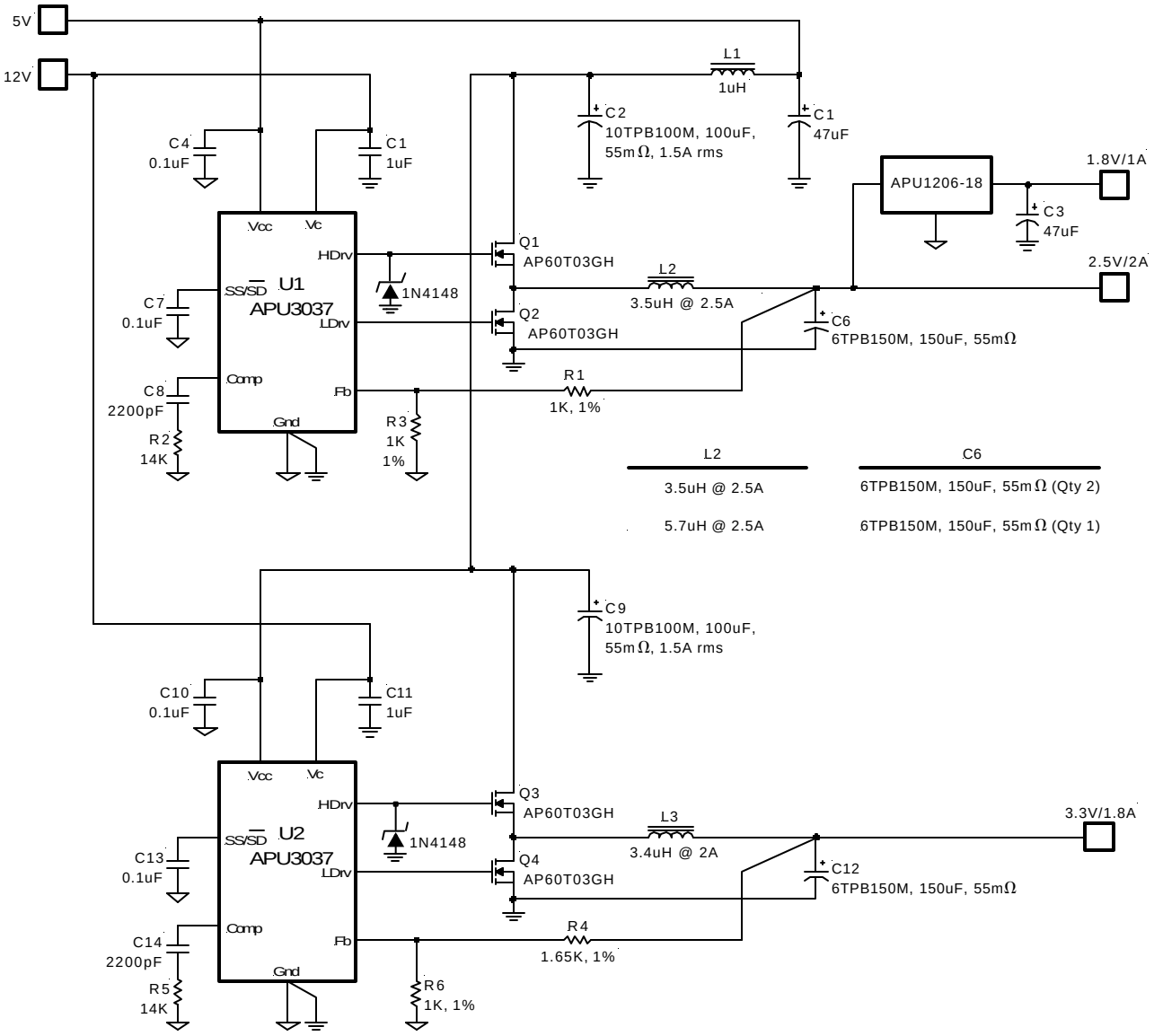


Figure 19 - Typical application of APU3037 or APU3037A in an on-board DC-DC converter providing the Core, GTL+, and Clock supplies for the Pentium II microprocessor.

TYPICAL APPLICATION

1.8V to 7.5V / 0.5A Boost Converter

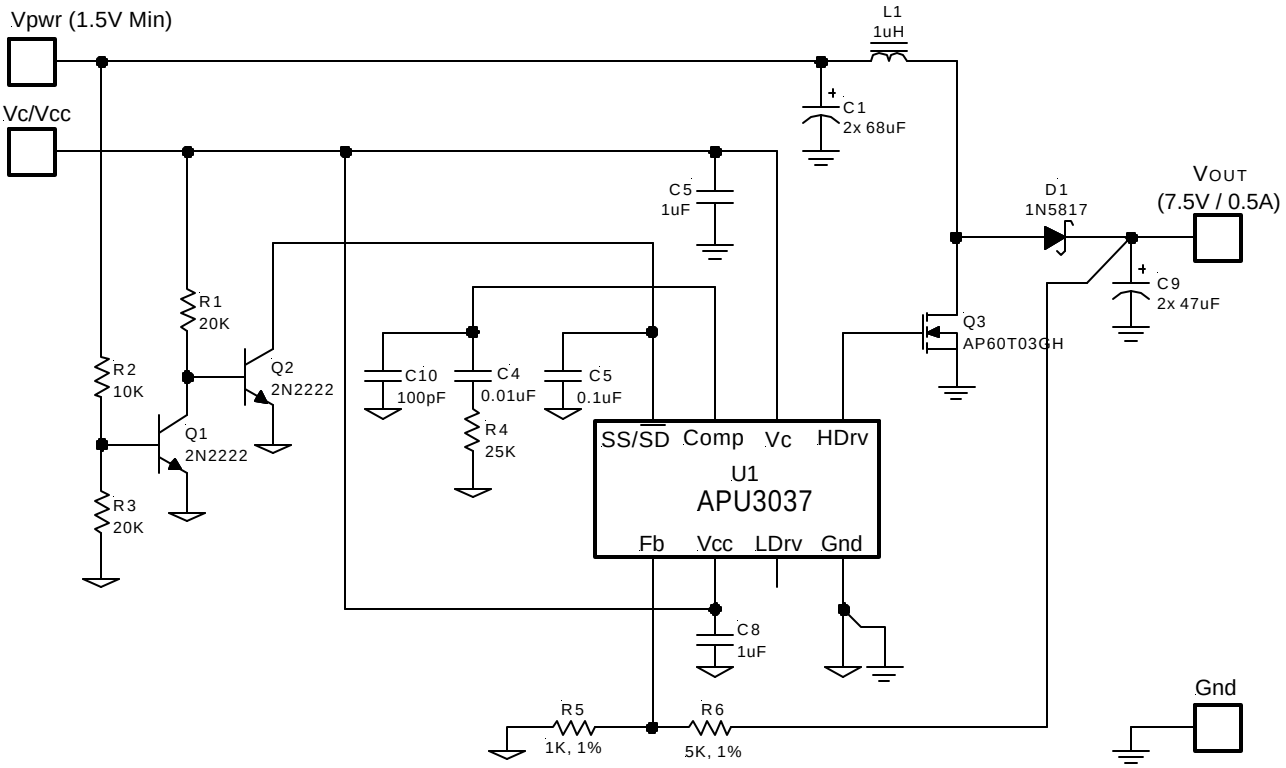


Figure 20 - Typical application of APU3037 as a boost converter.

DEMO-BOARD APPLICATION

5V or 12V to 3.3V @ 10A

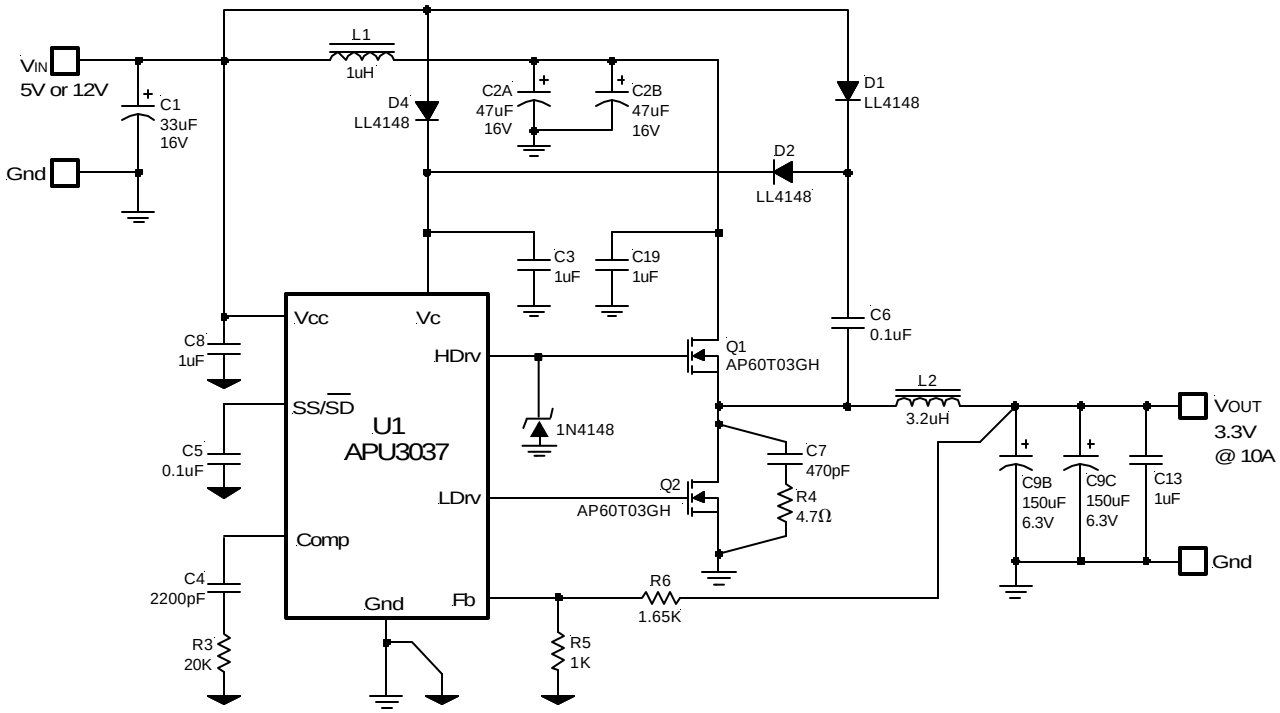


Figure 21 - Demo-board application of APU3037.

Application Parts List

Ref Desig	Description	Value	Qty	Part#	Manuf
Q1	MOSFET	30V, 12mΩ, 45A	1	AP60T03GH	APEC
Q2	MOSFET	30V, 12mΩ, 45A	1	AP60T03GH	APEC
U1	Controller	Synchronous PWM	1	APU3037	APEC
D1, D2, D4	Diode	Fast Switching	3	LL4148	
L1	Inductor	1μH, 10A	1	7445601	WE
L2	Inductor	3.2μH, 12A	1	7443550320	WE
C1	Capacitor, Tantalum	33μF, 16V	1	ECS-T1CD336R	
C2A, C2B	Capacitor, Poscap	47μF, 16V, 70mΩ	2	16TPB47M	
C9B, C9C	Capacitor, Poscap	150μF, 6.3V, 40mΩ	2	6TPC150M	
C5, C6	Capacitor, Ceramic	0.1μF, Y5V, 25V	2	ECJ-2VF1E104Z	
C3	Capacitor, Ceramic	1μF, X7R, 25V	1	ECJ-3YB1E105K	
C4	Capacitor, Ceramic	2200pF, X7R, 50V	1	ECJ-2VB1H222K	
C7	Capacitor, Ceramic	470pF, X7R	1	ECJ-2VB2D471K	
C8, C13, C19	Capacitor, Ceramic	1μF, Y5V, 16V	3	ECJ-2VF1C105Z	
R3	Resistor	20K, 5%	1		
R4	Resistor	4.7Ω, 5%	1		
R5	Resistor	1K, 1%	1		
R6	Resistor	1.65K, 1%	1		

DEMO-BOARD WAVEFORMS

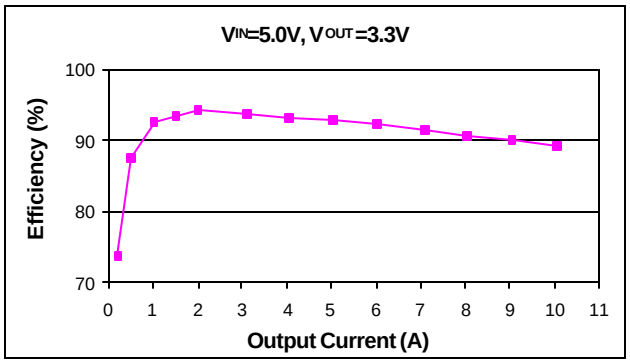


Figure 22 - Efficiency for APU3037 Evaluation Board.

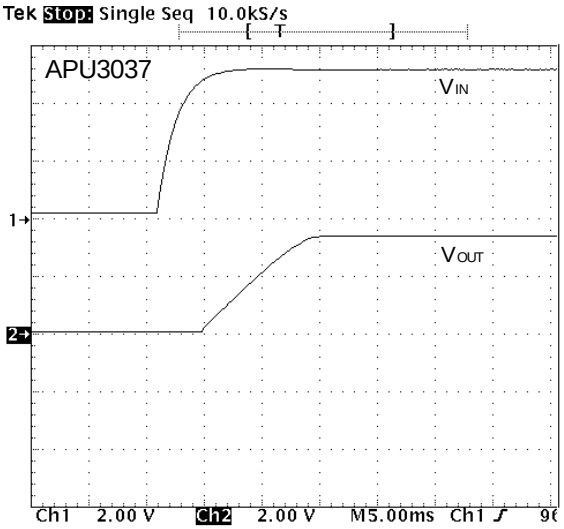


Figure 23 - Start-up time @ I_{OUT}=5A.

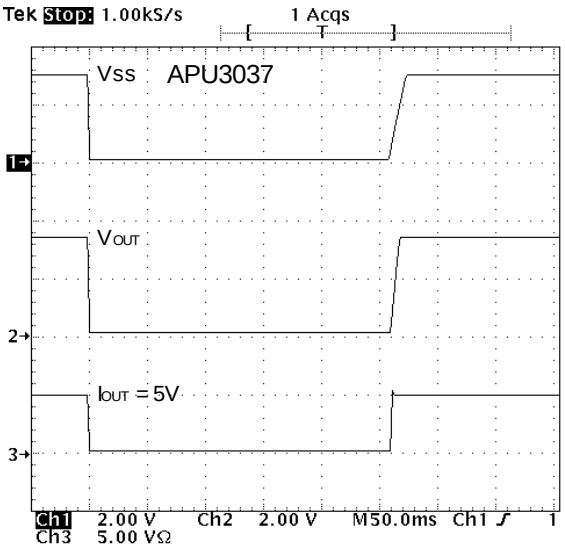


Figure 24 - Shutdown the output by pulling down the soft-start.

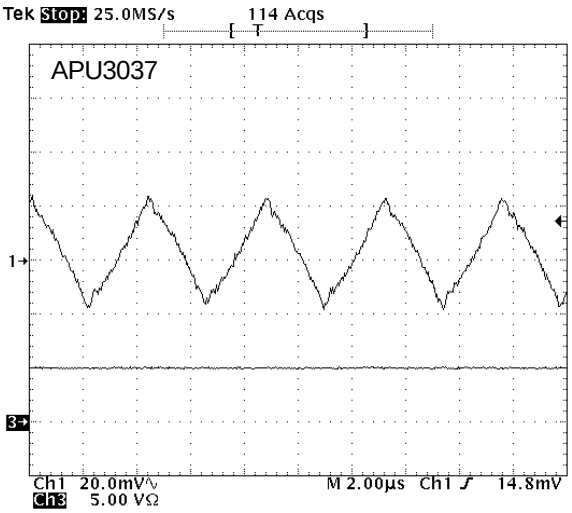


Figure 25 - 3.3V output voltage ripple @ I_{OUT}=5A.

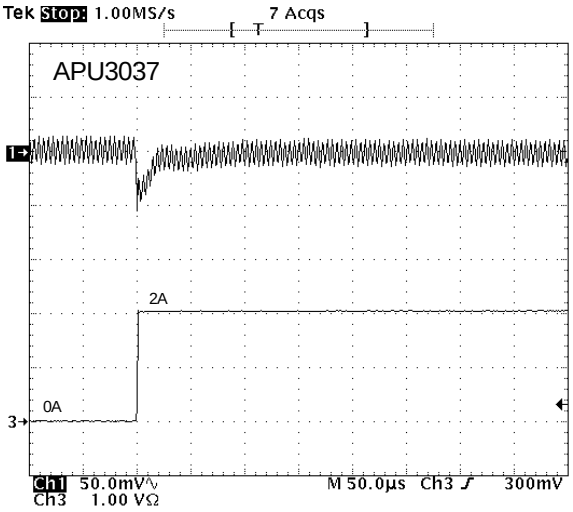


Figure 26 - Transient response @ I_{OUT} = 0 to 2A.

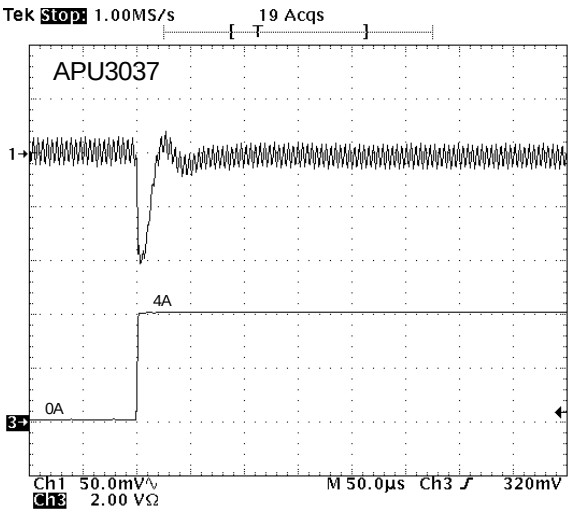
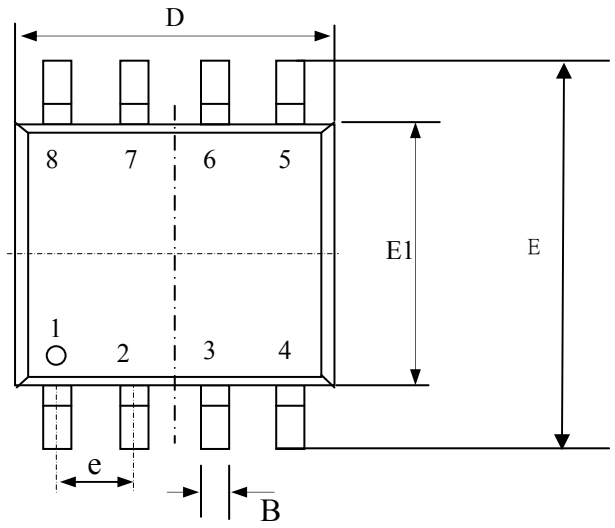
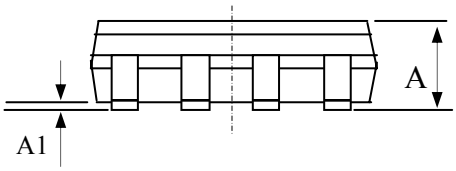


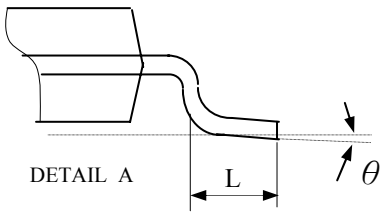
Figure 27 - Transient response @ I_{OUT} = 0 to 4A.

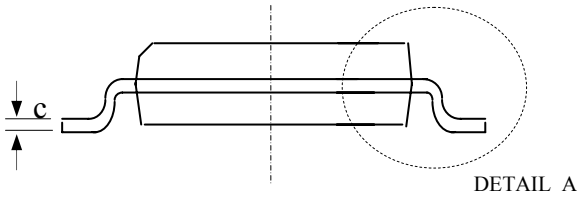
Package Outline : SO-8



	Millimeters		
SYMBOLS	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
B	0.33	0.41	0.51
C	0.19	0.22	0.25
D	4.80	4.90	5.00
E1	3.80	3.90	4.00
E	5.80	6.15	6.50
L	0.38	0.71	1.27
θ	0	4.00	8.00
e	1.27 TYP		



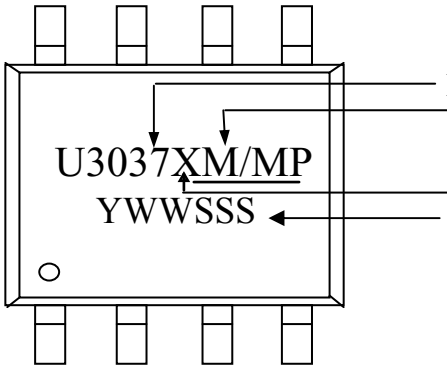




1.All Dimension Are In Millimeters.

2.Dimension Does Not Include Mold Protrusions.

Part Marking Information & Packing : SO-8



Part Number

Package Code

Frequency

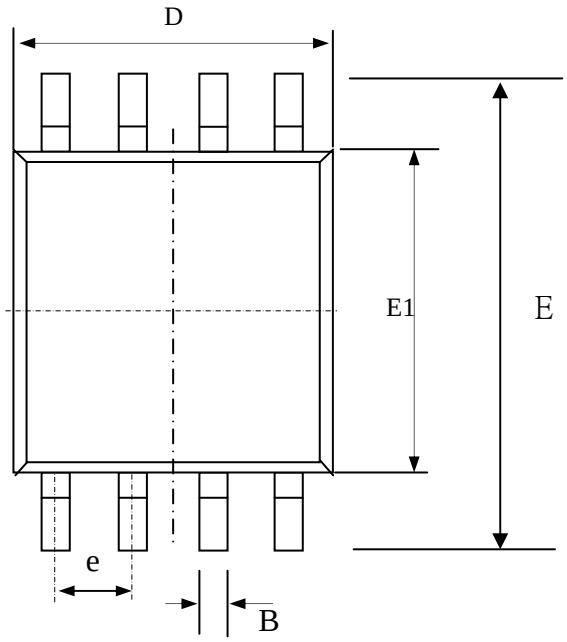
Date Code (YWWSSS)

Y：Last Digit Of The Year

WW：Week

SSS：Sequence

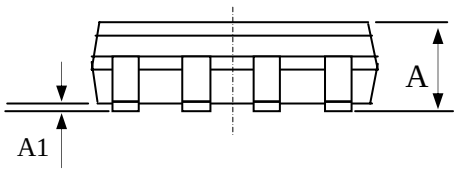
Package Outline : TSSOP-8

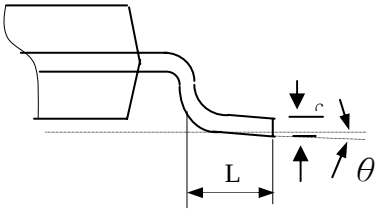


	Millimeters		
SYMBOLS	MIN	NOM	MAX
A	---	---	1.20
A1	0.05	---	0.15
B	0.19	---	0.30
C	---	0.127	----
D	2.90	3.00	3.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
e	0.65 REF.		
θ	0°	----	8°

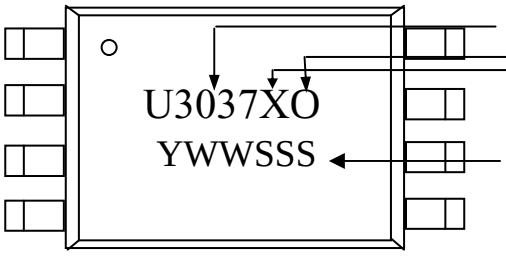
1.All Dimensions Are in Millimeters.

2.Dimension Does Not Include Mold Protrusions.





Part Marking Information & Packing : TSSOP-8



Part Number

Frequency

Package Code

Date Code (YWWSSS)

Y：Last Digit Of The Year

WW：Week

SSS：Sequence