

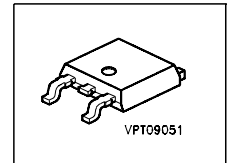
Cool MOS™ Power Transistor

Feature

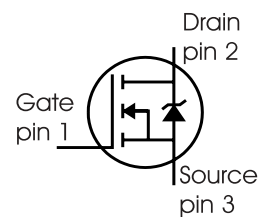
- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche rated
- Extreme dv/dt rated
- Ultra low effective capacitances
- Improved transconductance

$V_{DS} @ T_{jmax}$	560	V
$R_{DS(on)}$	3	Ω
I_D	1.8	A

P-TO252-3-1



Type	Package	Ordering Code	Marking
SPD02N50C3	P-TO252-3-1	Q67040-S4570	02N50C3



Maximum Ratings

Parameter	Symbol	Value	Unit
Continuous drain current $T_C = 25\text{ }^\circ\text{C}$ $T_C = 100\text{ }^\circ\text{C}$	I_D	1.8 1.1	A
Pulsed drain current, t_p limited by T_{jmax}	$I_{D\text{ puls}}$	5.4	
Avalanche energy, single pulse $I_D = 1.35\text{ A}$, $V_{DD} = 50\text{ V}$	E_{AS}	50	mJ
Avalanche energy, repetitive t_{AR} limited by T_{jmax} ¹ $I_D = 1.8\text{ A}$, $V_{DD} = 50\text{ V}$	E_{AR}	0.07	
Avalanche current, repetitive t_{AR} limited by T_{jmax}	I_{AR}	1.8	A
Gate source voltage	V_{GS}	± 20	V
Gate source voltage AC ($f > 1\text{ Hz}$)	V_{GS}	± 30	
Power dissipation, $T_C = 25\text{ }^\circ\text{C}$	P_{tot}	25	W
Operating and storage temperature	T_j, T_{stg}	-55... +150	$^\circ\text{C}$

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain Source voltage slope $V_{DS} = 400 \text{ V}$, $I_D = 1.8 \text{ A}$, $T_j = 125 \text{ }^\circ\text{C}$	dv/dt	50	V/ns

Thermal Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	-	-	5	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	75	
SMD version, device on PCB: @ min. footprint @ 6 cm ² cooling area ²⁾	R_{thJA}	-	-	75 50	
Soldering temperature, 1.6 mm (0.063 in.) from case for 10s	T_{sold}	-	-	260	$^\circ\text{C}$

Electrical Characteristics, at $T_j=25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{V}$, $I_D=0.25\text{mA}$	500	-	-	V
Drain-Source avalanche breakdown voltage	$V_{(BR)DS}$	$V_{GS}=0\text{V}$, $I_D=1.8\text{A}$	-	600	-	
Gate threshold voltage	$V_{GS(th)}$	$I_D=80\mu\text{A}$, $V_{GS}=V_{DS}$	2.1	3	3.9	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=500\text{V}$, $V_{GS}=0\text{V}$, $T_j=25^\circ\text{C}$, $T_j=150^\circ\text{C}$	- -	0.1 -	1 100	μA
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{V}$, $V_{DS}=0\text{V}$	-	-	100	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}$, $I_D=1.1\text{A}$, $T_j=25^\circ\text{C}$, $T_j=150^\circ\text{C}$	- -	2.7 7.3	3 -	Ω
Gate input resistance	R_G	$f=1\text{MHz}$, open Drain	-	12	-	

Electrical Characteristics , at $T_j = 25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Transconductance	g_{fs}	$V_{DS} \geq 2 \cdot I_D \cdot R_{DS(on)max}$, $I_D = 1.1A$	-	1.8	-	S
Input capacitance	C_{iss}	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1MHz$	-	190	-	pF
Output capacitance	C_{oss}		-	80	-	
Reverse transfer capacitance	C_{rss}		-	2	-	
Effective output capacitance, ³⁾ energy related	$C_{o(er)}$	$V_{GS} = 0V$, $V_{DS} = 0V$ to $400V$	-	9	-	pF
Effective output capacitance, ⁴⁾ time related	$C_{o(tr)}$		-	17	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 350V$, $V_{GS} = 0/10V$, $I_D = 1.8A$, $R_G = 25\Omega$	-	10	-	ns
Rise time	t_r		-	5	-	
Turn-off delay time	$t_{d(off)}$		-	70	-	
Fall time	t_f		-	15	-	

Gate Charge Characteristics

Gate to source charge	Q_{gs}	$V_{DD} = 400V$, $I_D = 1.8A$	-	1.5	-	nC
Gate to drain charge	Q_{gd}		-	4.5	-	
Gate charge total	Q_g	$V_{DD} = 400V$, $I_D = 1.8A$, $V_{GS} = 0$ to $10V$	-	9	-	
Gate plateau voltage	$V_{(plateau)}$	$V_{DD} = 400V$, $I_D = 1.8A$	-	5	-	V

¹ Repetitive avalanche causes additional power losses that can be calculated as $P_{AV} = E_{AR} \cdot f$.

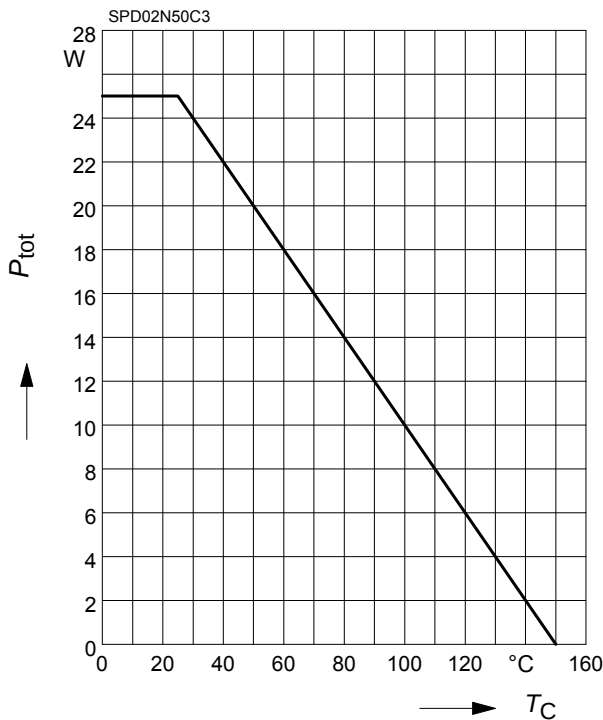
² Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical without blown air.

³ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⁴ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

1 Power dissipation

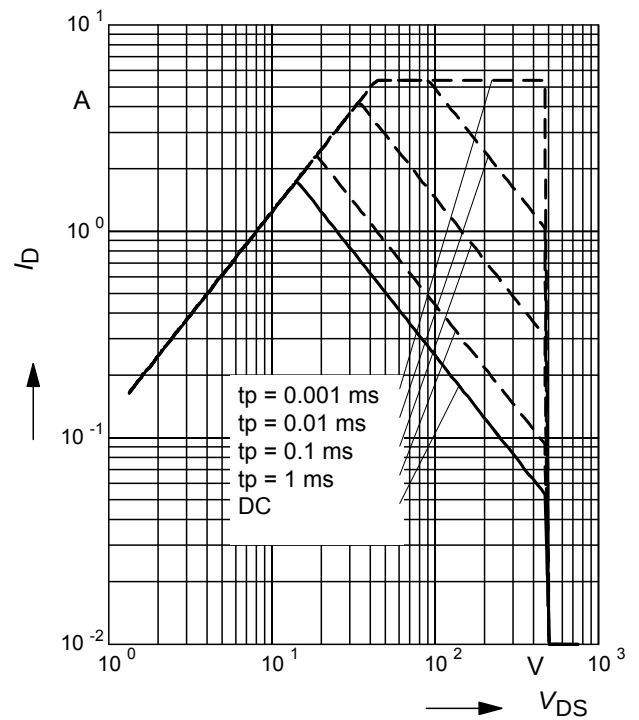
$$P_{\text{tot}} = f(T_C)$$



2 Safe operating area

$$I_D = f(V_{DS})$$

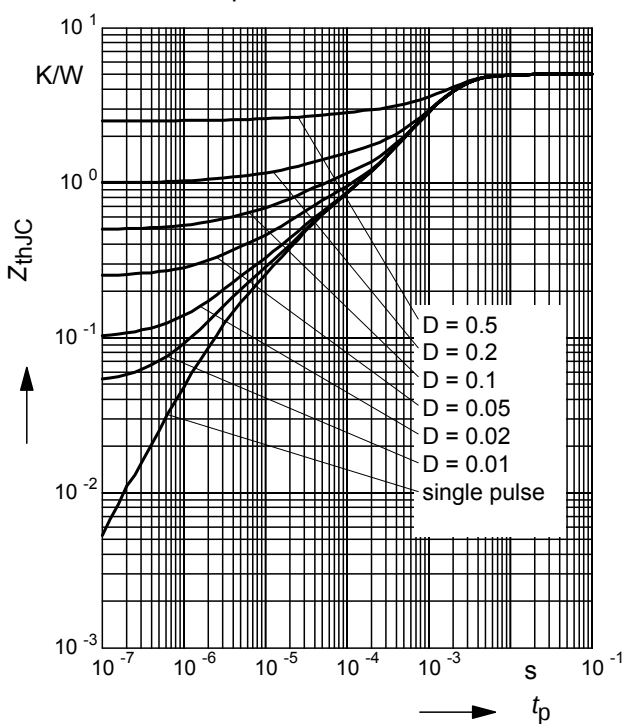
parameter : $D = 0$, $T_C = 25^\circ\text{C}$



3 Transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

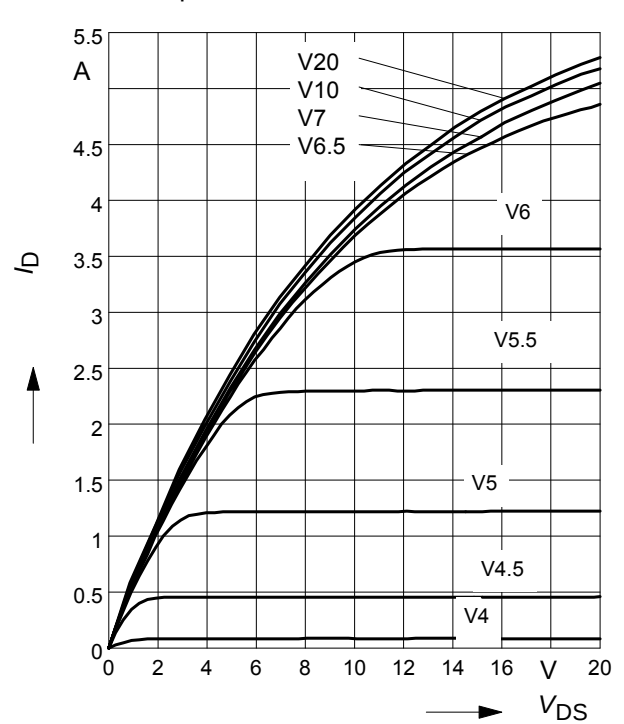
parameter: $D = t_p/T$



4 Typ. output characteristic

$$I_D = f(V_{DS}); T_J = 25^\circ\text{C}$$

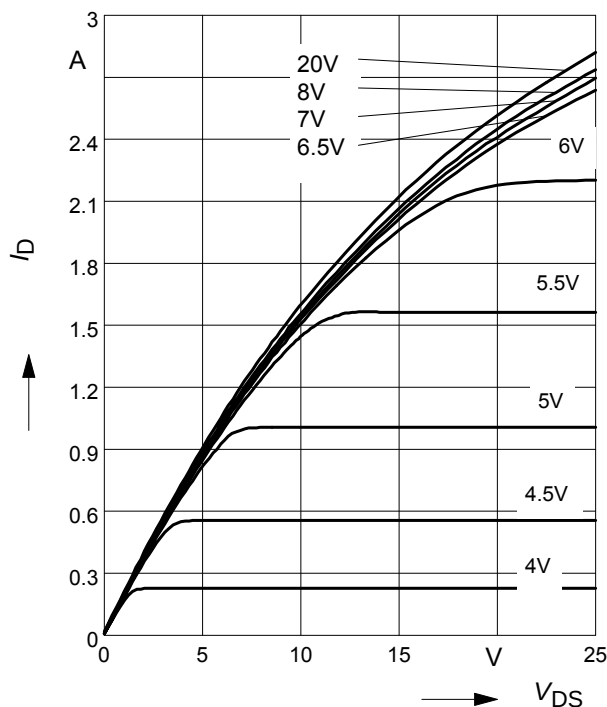
parameter: $t_p = 10 \mu\text{s}$, V_{GS}



5 Typ. output characteristic

$$I_D = f(V_{DS}); T_j = 150^\circ\text{C}$$

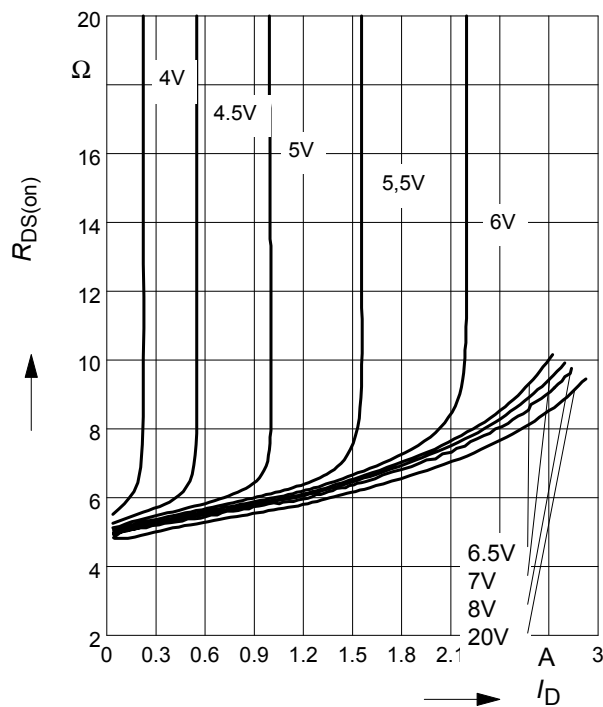
parameter: $t_p = 10 \mu\text{s}$, V_{GS}



6 Typ. drain-source on resistance

$$R_{DS(on)} = f(I_D)$$

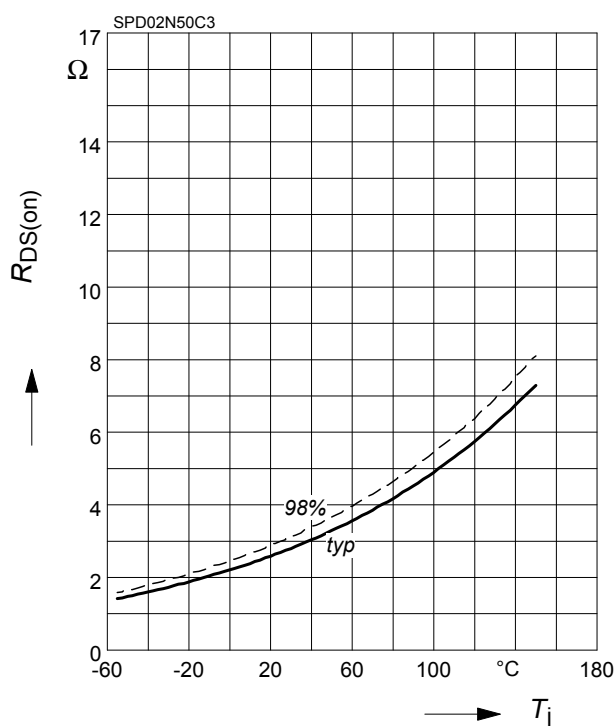
parameter: $T_j = 150^\circ\text{C}$, V_{GS}



7 Drain-source on-state resistance

$$R_{DS(on)} = f(T_j)$$

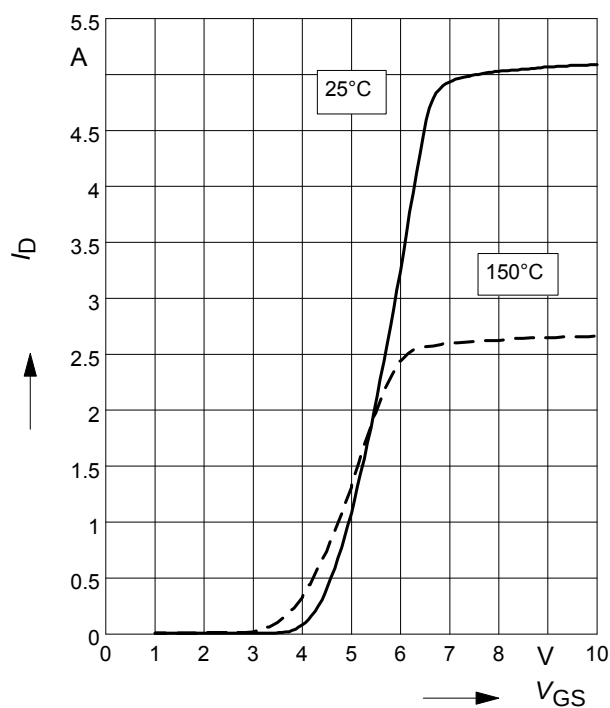
parameter: $I_D = 1.1 \text{ A}$, $V_{GS} = 10 \text{ V}$



8 Typ. transfer characteristics

$$I_D = f(V_{GS}); V_{DS} \geq 2 \times I_D \times R_{DS(on)\text{max}}$$

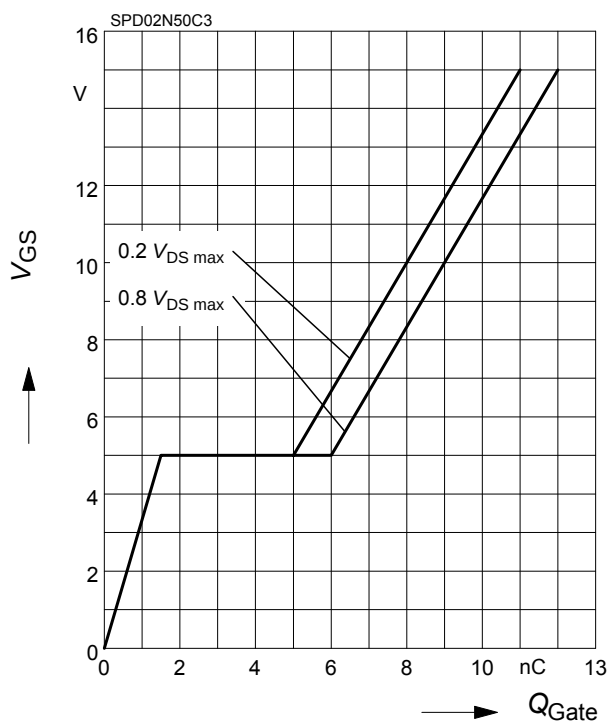
parameter: $t_p = 10 \mu\text{s}$



9 Typ. gate charge

$$V_{GS} = f(Q_{Gate})$$

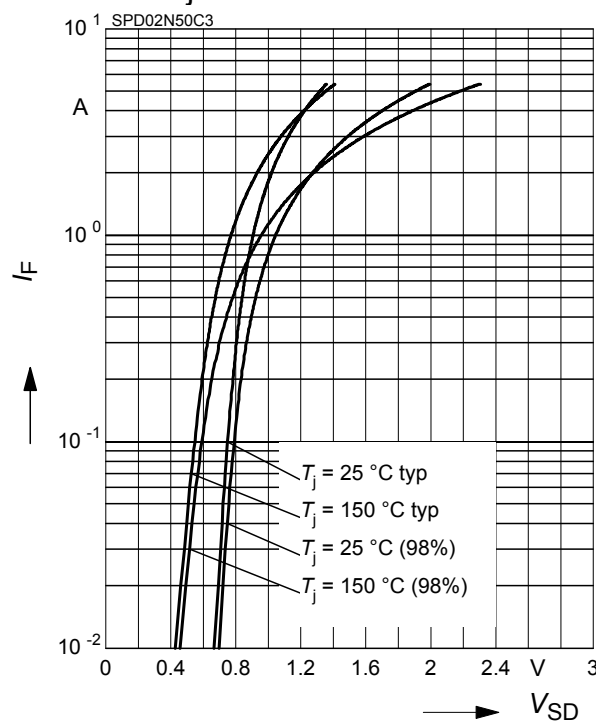
parameter: $I_D = 1.8 \text{ A}$ pulsed



10 Forward characteristics of body diode

$$I_F = f(V_{SD})$$

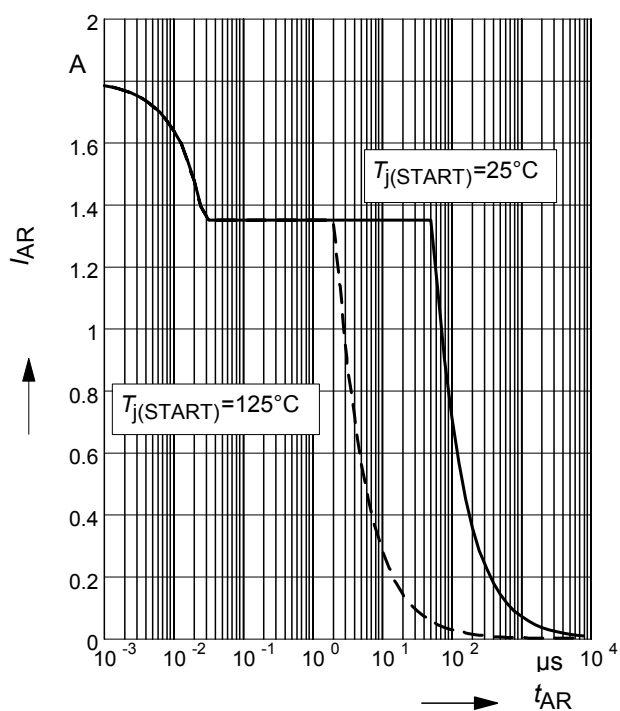
parameter: T_j , $t_p = 10 \mu\text{s}$



11 Avalanche SOA

$$I_{AR} = f(t_{AR})$$

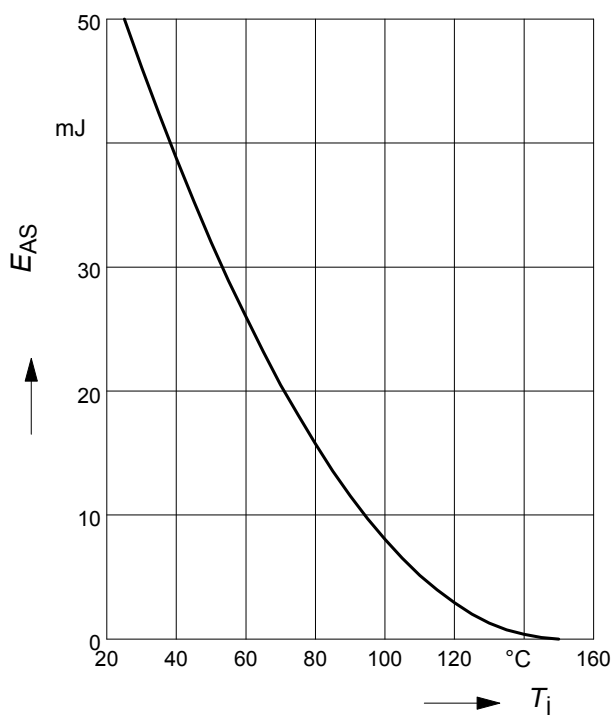
par.: $T_j \leq 150 \text{ °C}$



12 Avalanche energy

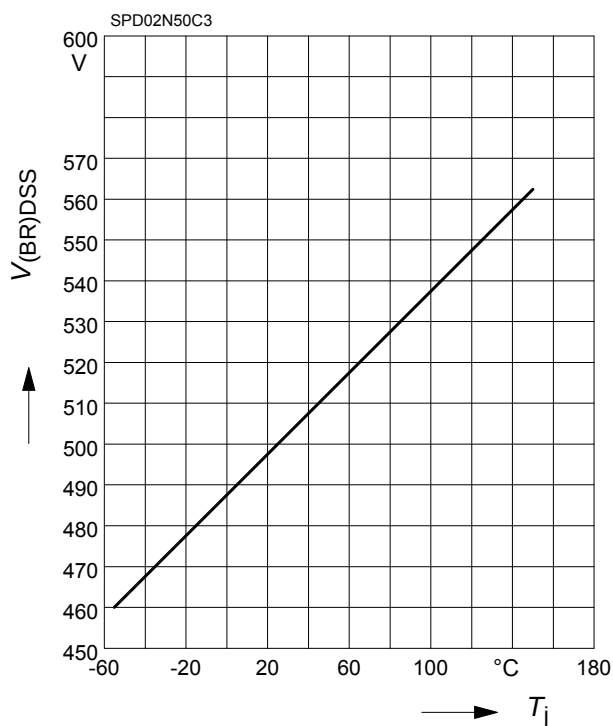
$$E_{AS} = f(T_j)$$

par.: $I_D = 1.35 \text{ A}$, $V_{DD} = 50 \text{ V}$



13 Drain-source breakdown voltage

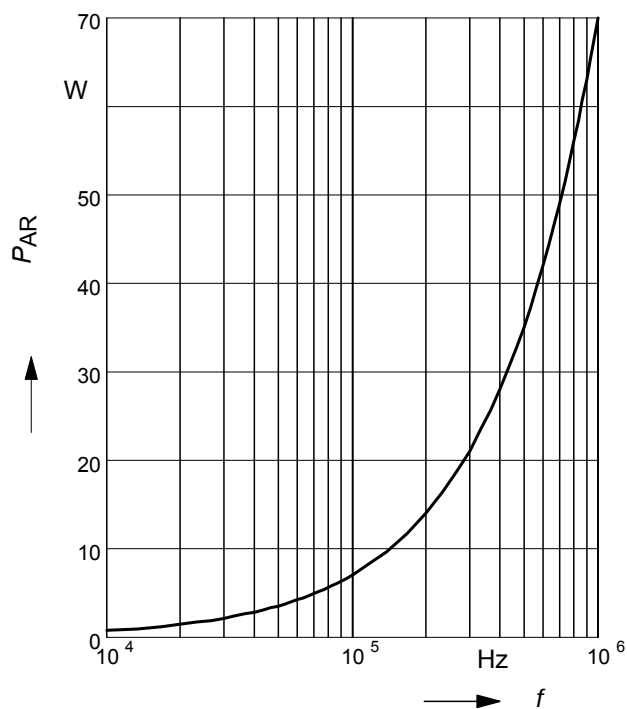
$$V_{(BR)DSS} = f(T_j)$$



14 Avalanche power losses

$$P_{AR} = f(f)$$

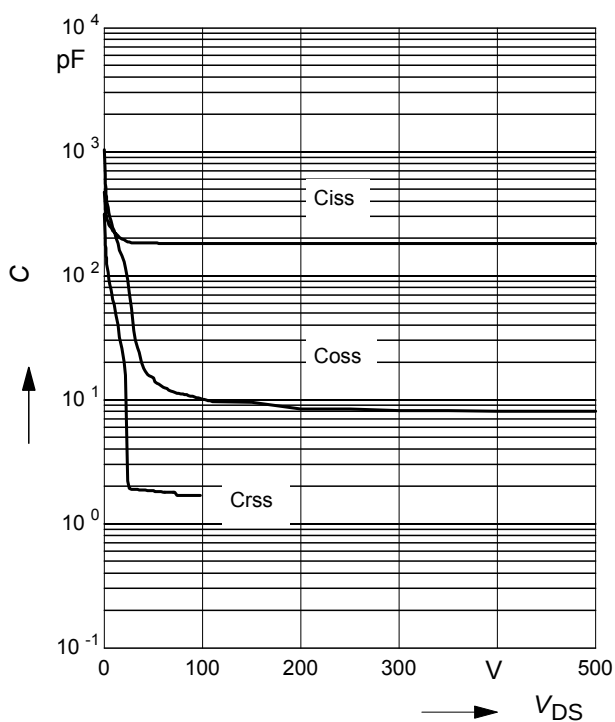
parameter: $E_{AR}=0.07\text{mJ}$



15 Typ. capacitances

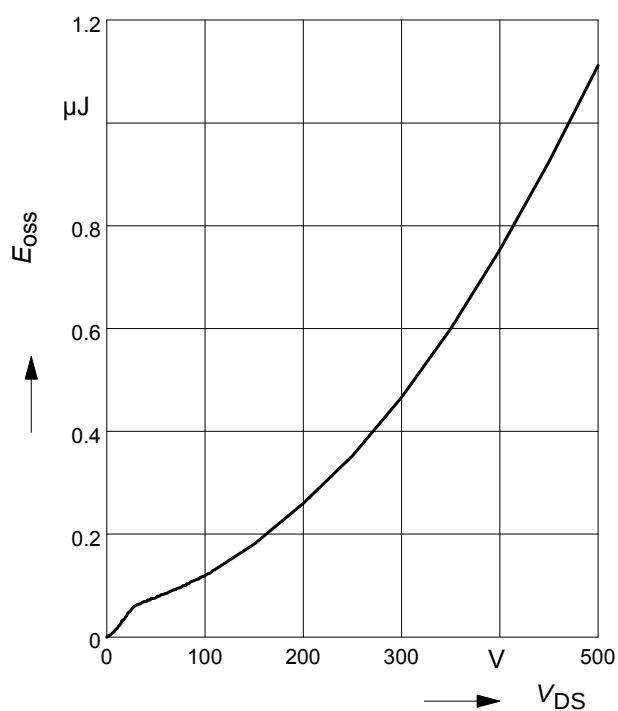
$$C = f(V_{DS})$$

parameter: $V_{GS}=0\text{V}$, $f=1\text{ MHz}$

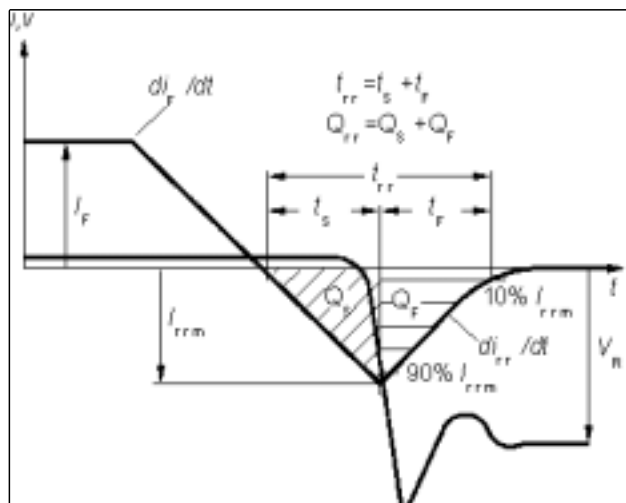


16 Typ. C_{OSS} stored energy

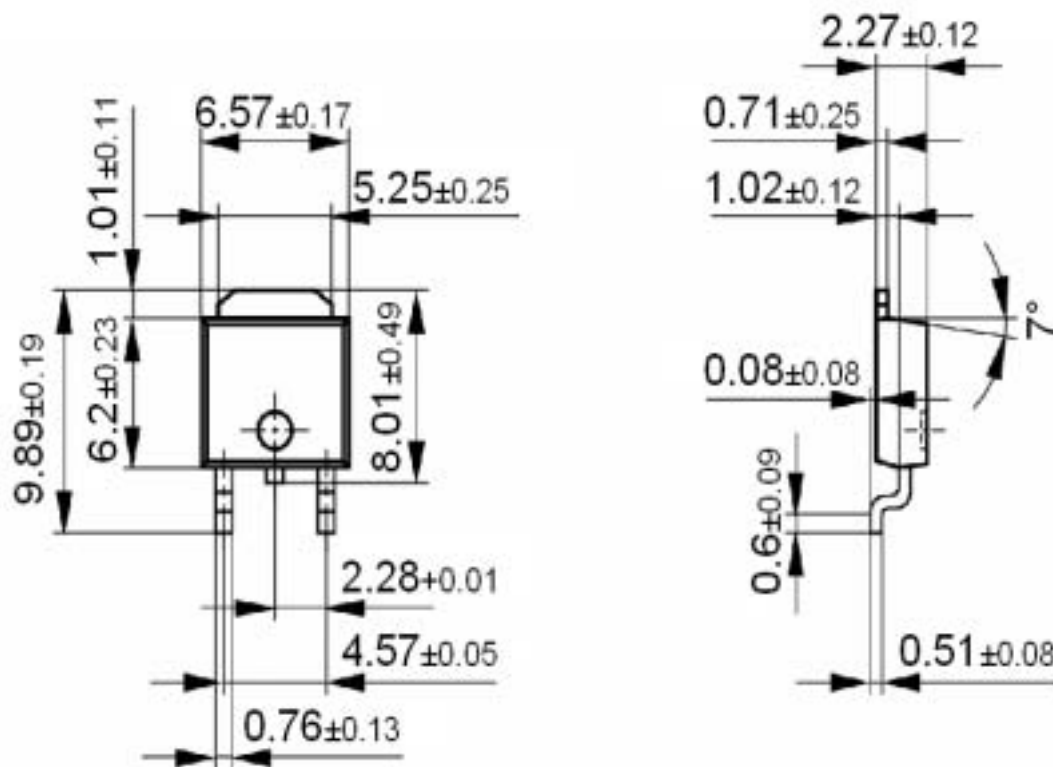
$$E_{OSS}=f(V_{DS})$$



Definition of diodes switching characteristics



P-TO-252-3-1 (D-PAK)



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