

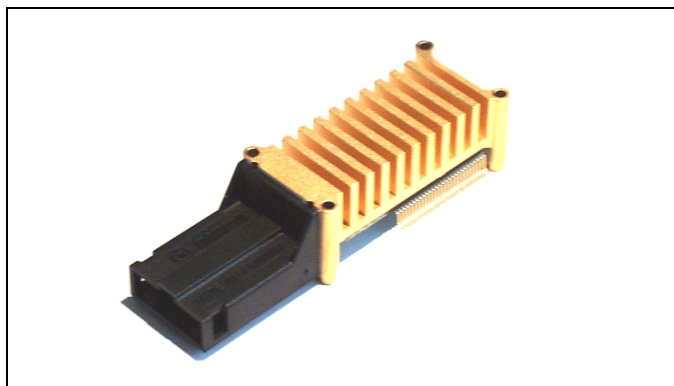
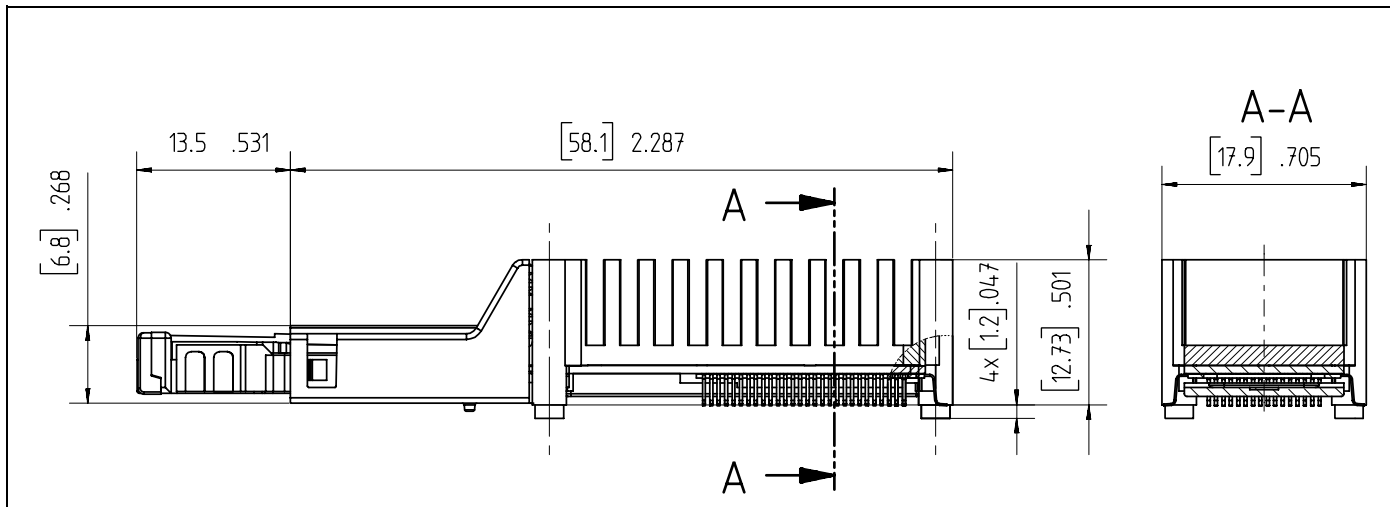


# V23814-U1306-M130

Parallel Optical Link: PAROLI® Tx AC, 1.6 Gbit/s

# V23815-U1306-M130

Parallel Optical Link: PAROLI® Rx AC, 1.6 Gbit/s



## FEATURES

- Power supply 3.3 V
- Low voltage differential signal electrical interface (LVDS)
- 12 electrical data channels
- Asynchronous, AC-coupled optical link
- 12 optical data channels
- Transmission data rate of up to 1600 Mbit/s per channel, total link data rate up to 19 Gbit/s
- 850 nm VCSEL array technology
- PIN diode array technology
- 62.5 μm graded index multimode fiber ribbon
- MT based optical port
- SMD technology
- Class 1 FDA and IEC Class 1 laser safety compliant

## APPLICATIONS

- Telecommunication**
  - Switching equipment
  - Access network
- Data Communication**
  - Interframe (rack-to-rack)
  - Intraframe (board-to-board)
  - On board (optical backplane)
  - Interface to SCI and HIPPI 6400 standards

## Absolute Maximum Ratings

Stress beyond the values stated below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

Supply Voltage ( $V_{CC}-V_{EE}$ ).....	-0.3 V to 4.5 V
Data/Control Input Levels ( $V_{IN}$ ) <sup>(1)</sup> .....	-0.5 V to $V_{CC}+0.5$ V
LVDS Input Differential Voltage ( $ V_{ID} $ ) <sup>(2)</sup> .....	2.0 V
Operating Case Temperature ( $T_{CASE}$ ) <sup>(3)</sup> .....	0°C to 80°C
Storage Ambient Temperature ( $T_{STG}$ ).....	-20°C to 100°C
Operating Moisture .....	20% to 85%
Storage Moisture.....	20% to 85%
Soldering Conditions Temp/Time ( $T_{SOLD}$ , $t_{SOLD}$ ) <sup>(4)</sup> .....	260°C/10s
ESD Resistance (all pins to $V_{EE}$ , human body model) <sup>(5)</sup> .....	1 kV

## Notes

1. At LVDS and LVC MOS inputs.
2.  $|V_{ID}| = |(\text{input voltage of non-inverted input} - \text{input voltage of inverted input})|$ .
3. Measured at case temperature reference point (see dimensional drawing).
4. Hot bar or hot air soldering.
5. To avoid electrostatic damage, handling cautions similar to those used for MOS devices must be observed.

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## DESCRIPTION

PAROLI is a parallel optical link for high-speed data transmission. A complete PAROLI system consists of a transmitter module, a 12-channel fiber optic cable, and a receiver module.

### Transmitter V23814-U1306-M130

The transmitter module converts parallel electrical input signals via a laser driver and a Vertical Cavity Surface Emitting Laser (VCSEL) diode array into parallel optical output signals. All input data signals are Low Voltage Differential Signals (LVDS). The data rate is up to 1600 Mbit/s for each channel. The transmitter module's min. data rate  $DR_{min}$  depends on the disparity  $D$  and on the duty cycle of the electrical input data. If the duty cycle exceeds 57%, the channel will be shut down with a minimum response time of 1  $\mu$ s. (See "Laser safety design considerations" on this page). If the input duty cycle does not exceed 57%, the channel will be switched off if the input data's maximal run length of '1' bits exceeds the response time of 1  $\mu$ s. In the worst case the input data's maximal running length of '1' bits equals its disparity  $D$ . From this we derive the following expression for  $DR_{min}$ , the minimum data rate:

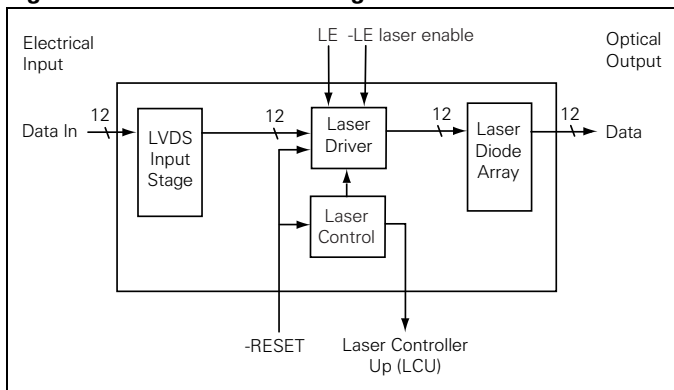
$$DR_{min} = D \text{ [Mbit/s]}$$

#### Notes

1. The running disparity of a data stream is the difference of the number of ones and zeroes of that data stream. The disparity  $D$  is the maximum value of the running disparity for all possible starting points (with running disparity set to zero at the starting point) in the data stream.
2. The run length is the maximal number of consecutive ones or zeroes in a data stream. The run length is  $\leq$  the disparity  $D$ .
3. Important:  
 $DR_{min}$  rate of the PAROLI link is higher than the value of  $DR_{min}$  of the transmitter module, as  $DR_{min}$  of the receiver module is higher. (See "Receiver V23815-U1306-M130" on page 6.)

A logic low level at  $\text{-RESET}$  switches all laser outputs off. During power-up  $\text{-RESET}$  must be used as a power-on reset which disables the laser driver and laser control until the power supply has reached a 3 V level. The Laser Controller Up (LCU) output is low if a laser fault is detected or  $\text{-RESET}$  is forced to low. All Onondaga signals have LVCMOS levels. Transmission delay of the PAROLI system is  $\leq 1$  ns for the transmitter,  $\leq 1$  ns for the receiver and approximately 5 ns per meter for the fiber optic cable.

Figure 1. Transmitter block diagram



## LASER SAFETY

The transmitter of the AC coupled Parallel Optical Link (PAROLI) is an FDA Class 1 laser product. It complies with FDA regulations 21 CFR 1040.10 and 1040.11. The transmitter is also an IEC Class 1 laser product as defined by IEC 60825-1 Amend. 2. To avoid possible exposure to hazardous levels of invisible laser radiation, do not exceed maximum ratings.

The PAROLI module must be operated under the specified operating conditions (supply voltage between 3.0 V and 3.6 V, case temperature between 0°C and 80°C) under any circumstances to ensure laser safety.

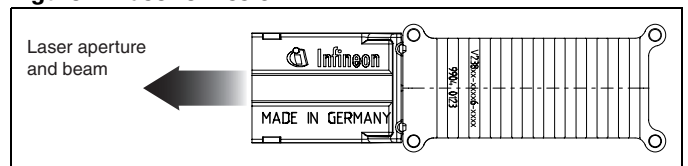
### Caution

#### Class 1 Laser Product

#### Note

Any modification of the module will be considered an act of "manufacturing," and will require, under law, recertification of the product under FDA (21 CFR 1040.10 (i)).

Figure 2. Laser emission



### Laser safety design considerations

To ensure laser safety for all input data patterns each channel is controlled internally and will be switched off if the laser safety limits are exceeded.

A channel alerter switches the respective data channel output off if the input duty cycle permanently exceeds 57%. The alerter will not disable the channel below an input duty cycle of 57% under all circumstances.

The minimum alerter response time is 1  $\mu$ s with a constant high input, i.e. in the input pattern the time interval of excessive high input (e.g. '1's in excess of a 57% duty cycle, consecutive or non-consecutive) must not exceed 1  $\mu$ s, otherwise the respective channel will be switched off. The alerter switches the respective channel from off to on without the need of resetting the module if the input duty cycle is no longer violated.

All of the channel alerters operate independently, i.e. an alert within a channel does not affect the other channels. To decrease the power consumption of the module unused channel inputs can be tied to high input level. In this way a portion of the supply current in this channel is triggered to shut down by the corresponding alerter.

## TECHNICAL DATA

The electro-optical characteristics described in the following tables are valid only for use under the recommended operating conditions.

### Recommended Operating Conditions

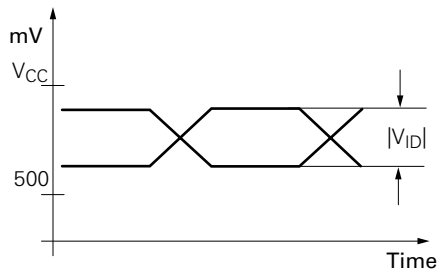
Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	$V_{CC}$	3.0	3.6	V
Noise on Power Supply <sup>(1)</sup>	$N_{PS1}$		50	mV
Noise on Power Supply <sup>(2)</sup>	$N_{PS2}$		100	
LVDS Input Voltage Range <sup>(6, 7)</sup>	$V_{LVDSI}$	500	$V_{CC}$	
LVDS Input Differential Voltage <sup>(3, 7)</sup>	$ V_{ID} $	100	1000	
LVDS Input Skew <sup>(4)</sup>	$t_{SPN}$		$0.5 \times t_R, t_F$	ps
LVDS Input Rise/Fall Time <sup>(5)</sup>	$t_R, t_F$	100	300	
LVC MOS Input High Voltage	$V_{LVC MOSIH}$	2.0	$V_{CC}$	V
LVC MOS Input Low Voltage	$V_{LVC MOSIL}$	$V_{EE}$	0.8	
LVC MOS Input Rise/Fall Time <sup>(8)</sup>	$t_R, t_F$		20	ns

### Notes

Voltages refer to  $V_{EE}=0$  V.

- Noise frequency is 1 kHz to 10 MHz. Voltage is peak-to-peak value.
- Noise frequency is > 10 MHz. Voltage is peak-to-peak value.
- $|V_{ID}|=|(\text{input voltage of non-inverted input minus input voltage of inverted input})|$ .
- Skew between positive and negative inputs measured at 50% level.
- 20%–80% level.
- This implies that the input stage can be AC coupled.
- Level diagram:

Figure 3. Input level diagram



- Measured between 0.8 V and 2.0 V.

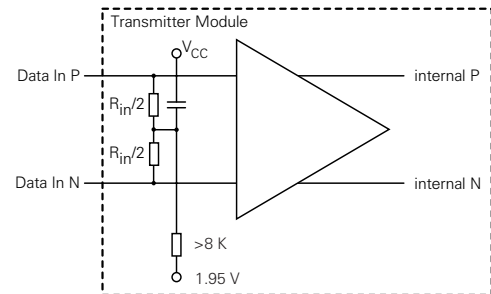
## Transmitter Electro-Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Current	$I_{CC}$		350	450	mA
Power Consumption	P		1.2	1.6	W
Data Rate per Channel	DR	(1)		1600	MBit/s
LVC MOS Output Voltage Low	$V_{LVC MOSOL}$			0.4	V
LVC MOS Output Voltage High	$V_{LVC MOSOH}$	2.5			V
LVC MOS Input Current High/Low	$I_{LVC MOSI}$	-500		500	$\mu$ A
LVC MOS Output Current High <sup>(2)</sup>	$I_{LVC MOSOH}$			0.5	mA
LVC MOS Output Current Low <sup>(3)</sup>	$I_{LVC MOSOL}$			4.0	mA
LVDS Differential Input Impedance <sup>(4)</sup>	$R_{IN}$	80		120	$\Omega$
LVDS Input Differential Current	$ I_I $			5.0	mA

### Notes

- $DR_{min} = D$  [Mbit/s], with  $D$ : disparity of the input pattern. (See “Transmitter V23814-U1306-M130” on page 2.)
- Source current.
- Sink current.
- LVDS input stage.

Figure 4. LVDS input stage



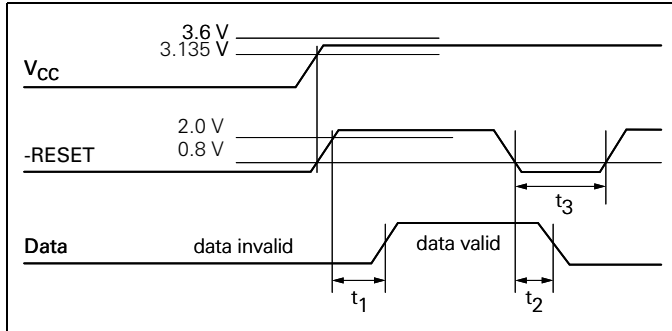
Parameter	Symbol	Min.	Max.	Units
Optical Rise Time <sup>(1)</sup>	$t_R$		400	ps
Optical Fall Time <sup>(1)</sup>	$t_F$			
Random Jitter ( $14\sigma$ ) <sup>(2)</sup>	$J_R$		0.23	UI
Deterministic Jitter	$J_D$		0.20	
Channel-to-channel skew <sup>(3)</sup>	$t_{CSK}$		75	ps
Launched Average Power	$P_{AVG}$	-11.0	-5.0	dBm
Launched Power Shutdown	$P_{SD}$		-30.0	
Center Wavelength	$\lambda_C$	840	860	nm
Spectral Width (FWHM)	$\Delta\lambda$		2	
Spectral Width (rms)	$\Delta\lambda$		0.85	
Relative Intensity Noise	RIN		-116	dB/Hz
Extinction Ratio (dynamic)	ER	6.0		dB

**Notes**

Optical parameters valid for each channel.

1. 20%–80% level, measured using a GBE (Gigabit Ethernet) filter.
2. Measured with 01010... (square) optical output pattern and in module thermal steady state status. Without cooling this steady state status is reached after approximately 10 minutes.
3. With input channel-to-channel skew 0 ps and a maximum LVDS channel-to-channel average deviation and swing deviation of 5%.

**Figure 5. Timing diagram**

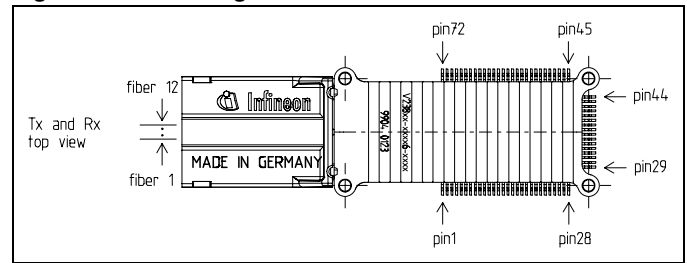


Parameter	Symbol	Min.	Max.	Units
-RESET on Delay Time	t <sub>1</sub>		100	ms
-RESET off Delay Time	t <sub>2</sub>		50	μs
-RESET Low Duration <sup>(1)</sup>	t <sub>3</sub>	10		μs

**Note**

1. Only when not used as power on reset. At any failure recovery, -RESET must be brought to low level for at least t<sub>3</sub>.

**Figure 6. Numbering conventions transmitter**



The numbering conventions for the Tx and Rx modules are the same.

**Transmitter Pin Description**

Pin#	Pin Name	Level/Logic	Description
1	V <sub>CC</sub>		Power supply voltage of laser driver
2	t.b.l.o.		to be left open
3			
4			
5			
6	LCU	LVC MOS Out	Laser Controller Up High=normal operation Low=laser fault or -RESET low
7	V <sub>EE</sub>		Ground
8	V <sub>EE</sub>		Ground
9	t.b.l.o.		to be left open
10	t.b.l.o.		to be left open
11	V <sub>EE</sub>		Ground
12	V <sub>EE</sub>		Ground
13	DI01N	LVDS In	Data Input #1, inverted
14	DI01P	LVDS In	Data Input #1, non- inverted
15	V <sub>EE</sub>		Ground
16	V <sub>EE</sub>		Ground
17	DI02N	LVDS In	Data Input #2, inverted
18	DI02P	LVDS In	Data Input #2, non- inverted
19	V <sub>EE</sub>		Ground
20	V <sub>EE</sub>		Ground
21	DI03N	LVDS In	Data Input #3, inverted
22	DI03P	LVDS In	Data Input #3, non- inverted
23	V <sub>EE</sub>		Ground
24	V <sub>EE</sub>		Ground
25	t.b.l.o.		to be left open
26	DI04N	LVDS In	Data Input #4, inverted
27	DI04P	LVDS In	Data Input #4, non- inverted
28	V <sub>EE</sub>		Ground
29	DI05N	LVDS In	Data Input #5, inverted
30	DI05P	LVDS In	Data Input #5, non- inverted
31	V <sub>EE</sub>		Ground
32	V <sub>EE</sub>		Ground
33	DI06N	LVDS In	Data Input #6, inverted
34	DI06P	LVDS In	Data Input #6, non- inverted

Pin#	Pin Name	Level/Logic	Description
35	V <sub>EE</sub>		Ground
36	V <sub>EE</sub>		Ground
37	DI07N	LVDS In	Data Input #7, inverted
38	DI07P	LVDS In	Data Input #7, non- inverted
39	V <sub>EE</sub>		Ground
40	V <sub>EE</sub>		Ground
41	DI08N	LVDS In	Data Input #8, inverted
42	DI08P	LVDS In	Data Input #8, non- inverted
43	V <sub>EE</sub>		Ground
44	V <sub>EE</sub>		Ground
45	V <sub>EE</sub>		Ground
46	DI09N	LVDS In	Data Input #9, inverted
47	DI09P	LVDS In	Data Input #9, non- inverted
48	t.b.l.o.		to be left open
49	V <sub>EE</sub>		Ground
50	V <sub>EE</sub>		Ground
51	DI10N	LVDS In	Data Input #10, inverted
52	DI10P	LVDS In	Data Input #10, non- inverted
53	V <sub>EE</sub>		Ground
54	V <sub>EE</sub>		Ground
55	DI11N	LVDS In	Data Input #11, inverted
56	DI11P	LVDS In	Data Input #11, non- inverted
57	V <sub>EE</sub>		Ground
58	V <sub>EE</sub>		Ground
59	DI12N	LVDS In	Data Input #12, inverted
60	DI12P	LVDS In	Data Input #12, non- inverted
61	V <sub>EE</sub>		Ground
62	V <sub>EE</sub>		Ground
63	t.b.l.o.		to be left open
64	-RESET	LVC MOS In	High=laser diode array is active Low=switches laser diode array off This input has an internal pull-down resistor to ensure laser safety switch off in case of unconnected -RESET input
65	V <sub>EE</sub>		Ground
66	V <sub>EE</sub>		Ground
67	LE	LVC MOS In	Laser ENABLE. High active. High=laser array is on if -LE is also active. Low=laser array is off. This input has an internal pull-up, therefore can be left open.
68	-LE		Laser ENABLE. Low active. Low=laser array is on if LE is also active. This input has an internal pull-down, therefore can be left open.

Pin#	Pin Name	Level/Logic	Description
69	t.b.l.o.		to be left open
70	t.b.l.o.		to be left open
71	t.b.l.o.		to be left open
72	V <sub>CC</sub>		Power supply voltage of laser driver

## DESCRIPTION

### Receiver V23815-U1306-M130

The PAROLI receiver module converts parallel optical input signals into parallel electrical output signals. The optical signals received are converted into voltage signals by PIN diodes, transimpedance amplifiers, and gain amplifiers. All output data signals are Low Voltage Differential Signals (LVDS).

The data rate is up to 1600 Mbit/s for each channel. The receiver module's min. data rate  $DR_{min}$  depends on the disparity  $D$  of the optical input data (coming from a transmitter module). It is given by the following expression:

$$DR_{min} = 8 \cdot D \text{ [Mbit/s]}$$

#### Notes

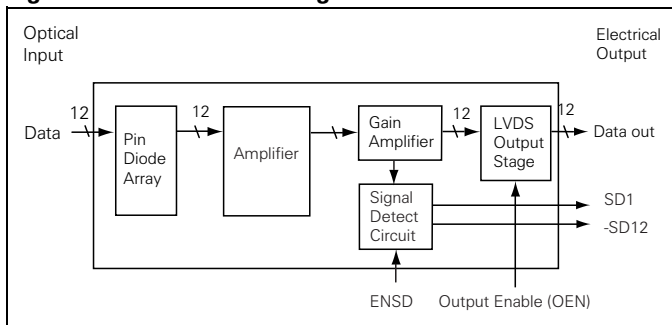
1. The running disparity of a data stream is the difference of the number of ones and zeroes of that data stream. The disparity  $D$  is the maximum value of the running disparity for all possible starting points (with running disparity set to zero at the starting point) in the data stream.

Additional Signal Detect outputs (SD1 active high / SD12 active low) show whether an optical AC input signal is present at data input 1 and/or 12. The signal detect circuit can be disabled with a logic low at ENSD. The disabled signal detect circuit will permanently generate an active level at Signal Detect outputs, even if there is insufficient signal input. This could be used for test purposes.

A logic low at LVDS Output Enable (OEN) sets all data outputs to logic low. SD outputs will not be effected.

All non data signals have LVCMOS levels. Transmission delay of the PAROLI system is at a maximum 1 ns for the transmitter, 1 ns for the receiver and approximately 5 ns per meter for the fiber optic cable.

**Figure 7. Receiver block diagram**



## TECHNICAL DATA

### Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	$V_{CC}$	3.0	3.6	V
Noise on Power Supply <sup>(1)</sup>	$N_{PS1}$		50	mV
Noise on Power Supply <sup>(2)</sup>	$N_{PS2}$		100	
Differential LVDS Termination Impedance	$R_t$	80	120	$\Omega$
LVCMOS Input High Voltage	$V_{LVCMOSIH}$	2.0	$V_{CC}$	V
LVCMOS Input Low Voltage	$V_{LVCMOSIL}$	$V_{EE}$	0.8	
LVCMOS Input Rise/Fall Time <sup>(3)</sup>	$t_R, t_F$		20	ns
Optical Input Rise/Fall Time <sup>(4)</sup>	$t_R, t_F$		400	ps
Input Extinction Ratio	ER	5.0		dB
Input Center Wavelength	$\lambda_C$	820	860	nm

#### Notes

Voltages refer to  $V_{EE}=0$  V.

1. Noise frequency is 1 kHz to 10 MHz. Voltage is peak-to-peak value.
2. Noise frequency is > 10 MHz. Voltage is peak-to-peak value.
3. Measured between 0.8 V and 2.0 V.
4. 20%–80% level.

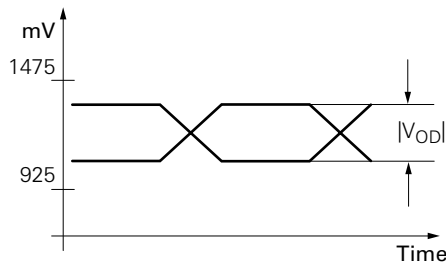
### Receiver Electro-Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Current	$I_{CC}$		250	350	mA
Power Consumption	P		0.8	1.3	W
LVDS Output Low Voltage <sup>(1,4)</sup>	$V_{LVDSOL}$	925			mV
LVDS Output High Voltage <sup>(1,4)</sup>	$V_{LVDSOH}$			1475	
LVDS Output Differential Voltage <sup>(1, 2, 4)</sup>	$ V_{OD} $	250		400	
LVDS Output Offset Voltage <sup>(1, 3, 4)</sup>	$V_{OS}$	1125		1275	
LVDS Rise/Fall Time <sup>(5)</sup>	$t_R, t_F$			400	ps
LVCMOS Output Voltage Low	$I_{LVCMOSOL}$			400	mV
LVCMOS Output Voltage High	$I_{LVCMOSOH}$	2500			
LVCMOS Input Current High/Low	$I_{LVCMOSI}$	-500		500	$\mu$ A
LVCMOS Output <sup>(8)</sup> Current High	$I_{LVCMOSOH}$			0.5	mA
LVCMOS Output <sup>(9)</sup> Current Low	$I_{LVCMOSOL}$			4.0	
Random Jitter <sup>(6, 7)</sup> ( $14\sigma$ )	$J_R$			0.31	UI
Deterministic Jitter <sup>(6)</sup>	$J_D$			0.08	
Channel-to-channel skew <sup>(10)</sup>	$t_{CSK}$			75	ps

Notes

1. Level Diagram

Figure 8. Output level diagram



2.  $|V_{ODI}|$ =(output voltage of non-inverted output minus output voltage of inverted output).
3.  $V_{OS} = 1/2$  (output voltage of inverted output + output voltage of non-inverted output).
4. LVDS output must be terminated differentially with  $R_t$ .
5. Measured between 20% and 80% level with a maximum capacitive load of 5 pF.
6. With no optical input jitter.
7. At sensitivity limit of -18.0 dBm at infinite ER.
8. Source current
9. Sink current
10. With input channel-to-channel skew 0 ps.

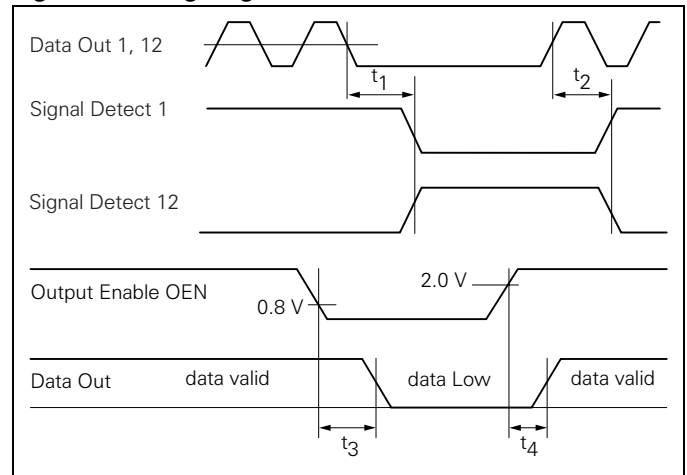
Parameter	Symbol	Min.	Max.	Units
Data Rate Per Channel	DR	(1)	1600	Mbit/s
Sensitivity (Average Power) <sup>(2)</sup>	P <sub>IN</sub>		-18.0	dBm
Saturation (Average Power) <sup>(2)</sup>	P <sub>SAT</sub>	-5.0		
Signal Detect Assert Level <sup>(3)</sup>	P <sub>SDA</sub>		-19.0	
Signal Detect Deassert Level <sup>(3)</sup>	P <sub>SDD</sub>	-28.0		
Signal Detect Hysteresis <sup>(3)</sup>	P <sub>SDA</sub> -P <sub>SDD</sub>	1.0	4.0	dB
Return Loss of Receiver	ARL	12		

Notes

Optical parameters valid for each channel.

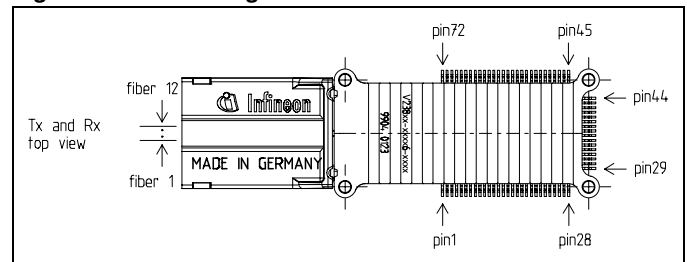
1.  $DR_{min} = 8 \cdot D$  [Mbit/s], with  $D$ : disparity of the input pattern. (See "Receiver V23815-U1306-M130" on page 6.)
2.  $D \leq 100$ , BER= $10^{-12}$ , Extinction ratio=infinite.
3. Extinction ratio=infinite,  
 P<sub>SDA</sub>: Average optical power when SD switches from inactive to active.  
 P<sub>SDD</sub>: Average optical power when SD switches from active to inactive.

Figure 9. Timing diagrams



Parameter	Symbol	Max.	Units
Signal Detect Deassert Time	t <sub>1</sub>	10	μs
Signal Detect Assert Time	t <sub>2</sub>		
LVDS Output Enable off Delay Time	t <sub>3</sub>	20	ns
LVDS Output Enable on Delay Time	t <sub>4</sub>		

Figure 10. Numbering conventions receiver



Receiver Pin Description

Pin#	Pin Name	Level/Logic	Description
1	V <sub>EE</sub>		Ground
2	V <sub>CC</sub>		Power supply voltage of pre-amplifier and analog circuitry
3	V <sub>CCO</sub>		Power supply voltage of output stages
4	t.b.l.o.		to be left open
5	OEN	LVC MOS In	Output Enable High=normal operation Low=sets all Data Outputs to low This input has an internal pull-up resistor which pulls to high level when this input is left open
6	SD1	LVC MOS Out	Signal Detect on fiber #1. High=signal of sufficient AC power is present on fiber #1 Low=signal on fiber #1 is insufficient.

Pin#	Pin Name	Level/Logic	Description
7	V <sub>CCO</sub>		Power supply voltage of output stages
8	V <sub>EE</sub>		Ground
9	t.b.l.o.		to be left open
10	V <sub>EE</sub>		Ground
11	V <sub>EE</sub>		Ground
12	V <sub>EE</sub>		Ground
13	DO01P	LVDS Out	Data Output #1, non-inverted
14	DO01N	LVDS Out	Data Output #1, inverted
15	V <sub>EE</sub>		Ground
16	V <sub>EE</sub>		Ground
17	DO02P	LVDS Out	Data Output #2, non-inverted
18	DO02N	LVDS Out	Data Output #2, inverted
19	V <sub>EE</sub>		Ground
20	V <sub>EE</sub>		Ground
21	DO03P	LVDS Out	Data Output #3, non-inverted
22	DO03N	LVDS Out	Data Output #3, inverted
23	V <sub>EE</sub>		Ground
24	V <sub>EE</sub>		Ground
25	t.b.l.o.		to be left open
26	DO04P	LVDS Out	Data Output #4, non-inverted
27	DO04N	LVDS Out	Data Output #4, inverted
28	V <sub>EE</sub>		Ground
29	DO05P	LVDS Out	Data Output #5, non-inverted
30	DO05N	LVDS Out	Data Output #5, inverted
31	V <sub>EE</sub>		Ground
32	V <sub>EE</sub>		Ground
33	DO06P	LVDS Out	Data Output #6, non-inverted
34	DO06N	LVDS Out	Data Output #6, inverted
35	V <sub>EE</sub>		Ground
36	V <sub>EE</sub>		Ground
37	DO07P	LVDS Out	Data Output #7, non-inverted
38	DO07N	LVDS Out	Data Output #7, inverted
39	V <sub>EE</sub>		Ground
40	V <sub>EE</sub>		Ground
41	DO08P	LVDS Out	Data Output #8, non-inverted
42	DO08N	LVDS Out	Data Output #8, inverted
43	V <sub>EE</sub>		Ground
44	V <sub>EE</sub>		Ground
45	V <sub>EE</sub>		Ground
46	DO09P	LVDS Out	Data Output #9, non-inverted
47	DO09N	LVDS Out	Data Output #9, inverted
48	t.b.l.o.		to be left open
49	V <sub>EE</sub>		Ground
50	V <sub>EE</sub>		Ground
51	DO10P	LVDS Out	Data Output #10, non-inverted
52	DO10N	LVDS Out	Data Output #10, inverted

Pin#	Pin Name	Level/Logic	Description
53	V <sub>EE</sub>		Ground
54	V <sub>EE</sub>		Ground
55	DO11P	LVDS Out	Data Output #11, non-inverted
56	DO11N	LVDS Out	Data Output #11, inverted
57	V <sub>EE</sub>		Ground
58	V <sub>EE</sub>		Ground
59	DO12P	LVDS Out	Data Output #12, non-inverted
60	DO12N	LVDS Out	Data Output #12, inverted
61	V <sub>EE</sub>		Ground
62	V <sub>EE</sub>		Ground
63	V <sub>EE</sub>		Ground
64	t.b.l.o.		to be left open
65	V <sub>EE</sub>		Ground
66	V <sub>CCO</sub>		Power supply voltage of output stages
67	-SD12	LVC MOS Out low active	Signal Detect on fiber #12 Low=signal of sufficient AC power is present on fiber #12 High=signal on fiber #12 is insufficient.
68	ENSD	LVC MOS In	Enable Signal Detect High=SD1 and SD12 function enabled Low=SD1 and SD12 are set to permanent active. This input has an internal pull-up resistor which pulls to high level when this input is left open
69	t.b.l.o.		to be left open
70	V <sub>CC</sub>		Power supply voltage of pre-amplifier and analog circuitry
71	V <sub>CC</sub>		Power supply voltage of pre-amplifier and analog circuitry
72	V <sub>EE</sub>		Ground



## Optical Port

- Designed for the Simplex MT Connector (SMC)
- Port outside dimensions: 15.4 mm x 6.8 mm (width x height)
- MT compatible (IEC 61754-5) fiber spacing (250  $\mu\text{m}$ ) and alignment pin spacing (4600  $\mu\text{m}$ )
- Alignment pins fixed in module port
- Integrated mechanical keying
- Process plug (SMC dimensions) included with every module
- Cleaning of port and connector interfaces necessary prior to mating

## Features of the Simplex MT Connector (SMC)

(as part of optional PAROLI fiber optic cables)

- Uses standardized MT ferrule (IEC 61754-5)
- MT compatible fiber spacing (250  $\mu\text{m}$ ) and alignment pin spacing (4600  $\mu\text{m}$ )
- Snap-in mechanism
- Ferrule bearing spring loaded
- Integrated mechanical keying

## Assembly

On the next pages are some figures to assist the customer in designing his printed circuit board (PCB). Figure 11 shows the mechanical dimensions of the PAROLI transmitter and receiver modules and Figures 12 to 14 give the dimensions of the holes and solder pads on a customer PCB that are necessary to mount the modules on this PCB. Keeping the tolerances for the PCB given in Figures 12 to 14 is required to properly attach the PAROLI transmitter and receiver module to the PCB.

Attachment to the customer PCB should be done with four M2 screws torqued to 0.25 Nm + 0.05 Nm (see Figure 11, cross section B-B). The screw length  $a$  should be 3 to 4 mm plus the thickness  $b$  of the customer PCB.

Special care must be taken to remove residues from the soldering and washing process which can impact the mechanical function. Avoid the use of aggressive organic solvents like ketones, ethers, etc. Consult the supplier of the PAROLI modules and the supplier of the solder paste and flux for recommended cleaning solvents.

The following common cleaning solvents will not affect the module: deionized water, ethanol, and isopropyl alcohol. Air-drying is recommended to a maximum temperature of 150°C. Do not use ultrasonics.

During soldering, heat must be applied to the leads only, to ensure that the case temperature never exceeds 150°C. The module must be mounted with a hot-air or hot-bar soldering process using a SnPb solder type, e.g. Sn62Pb36Ag2, in accordance with ISO 9435.

**Figure 11. Drawing of the PAROLI transmitter and receiver module**

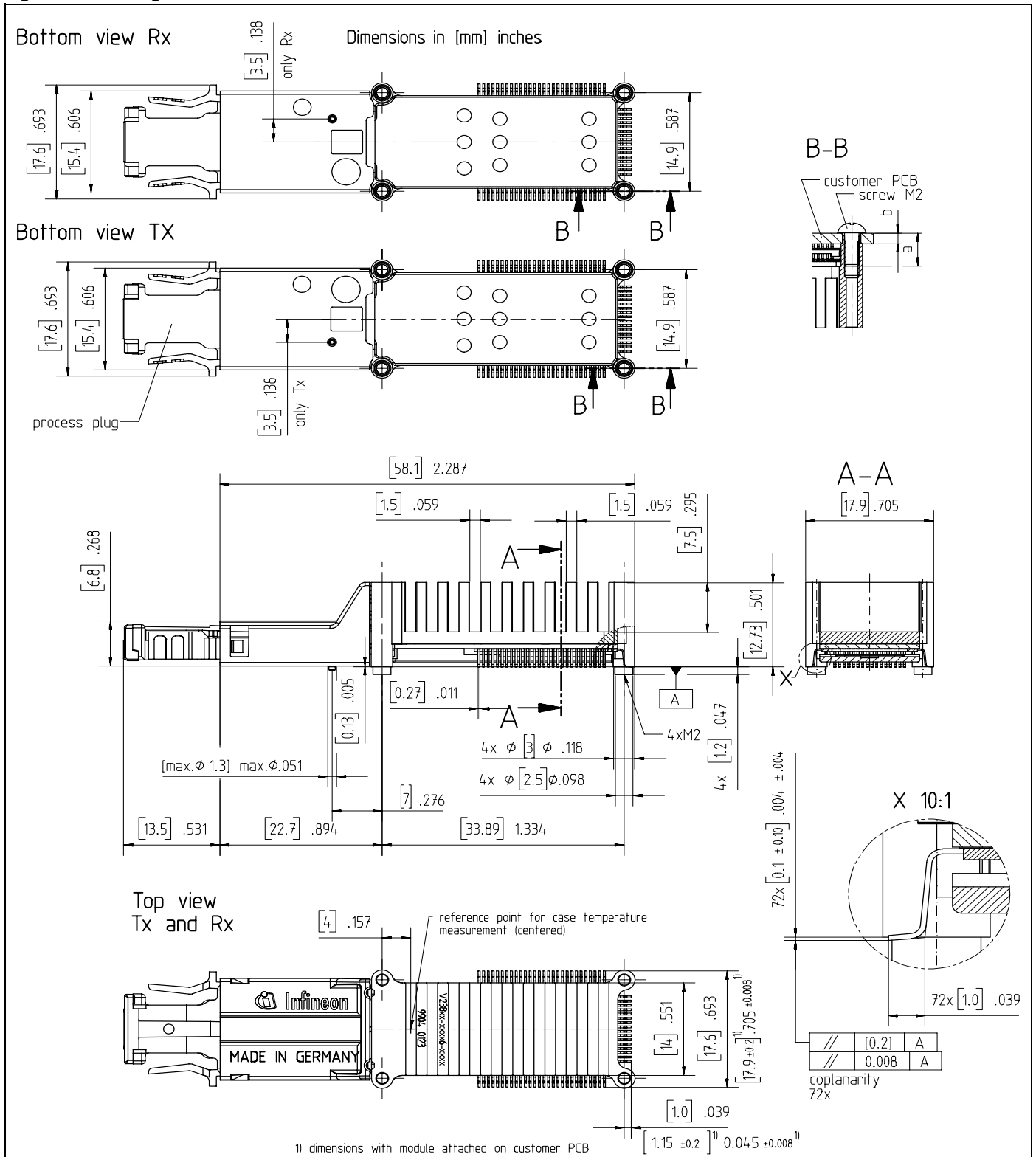


Figure 12. Recommended circuit board layout: transmitter

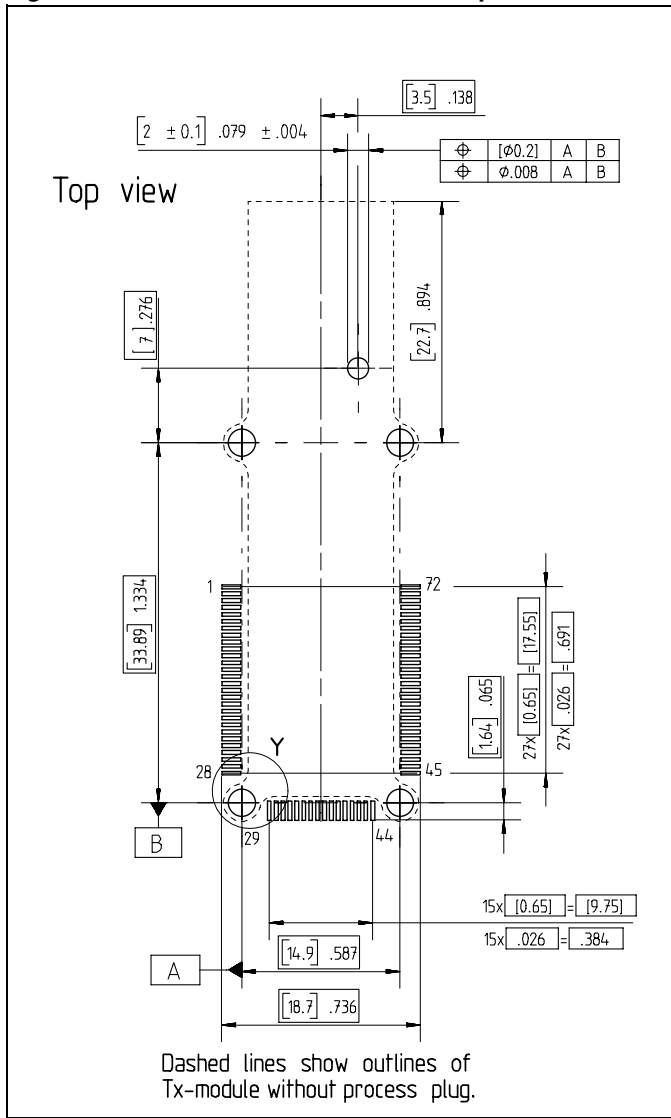
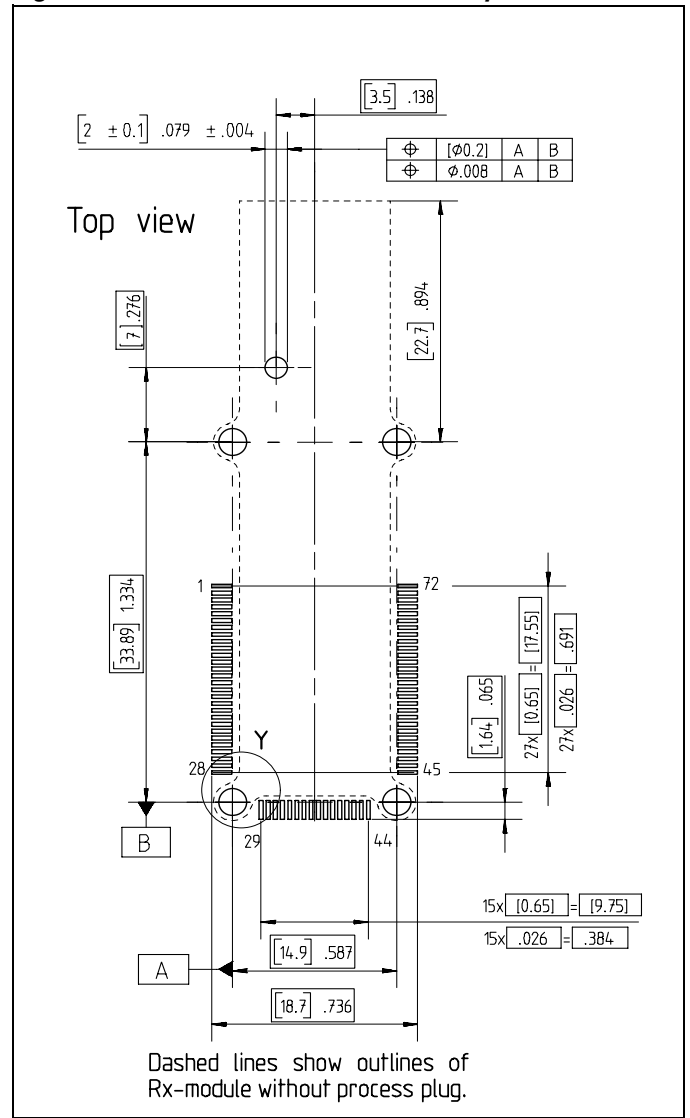
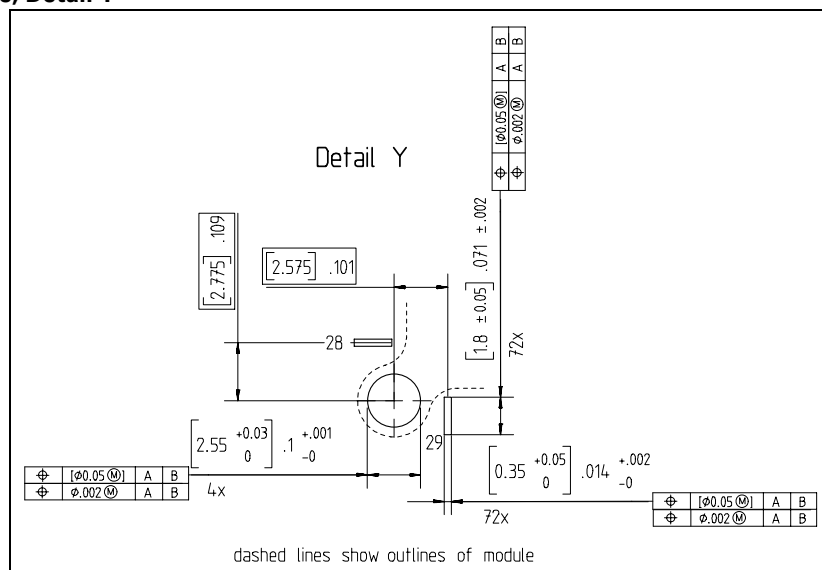


Figure 13. Recommended circuit board layout: receiver

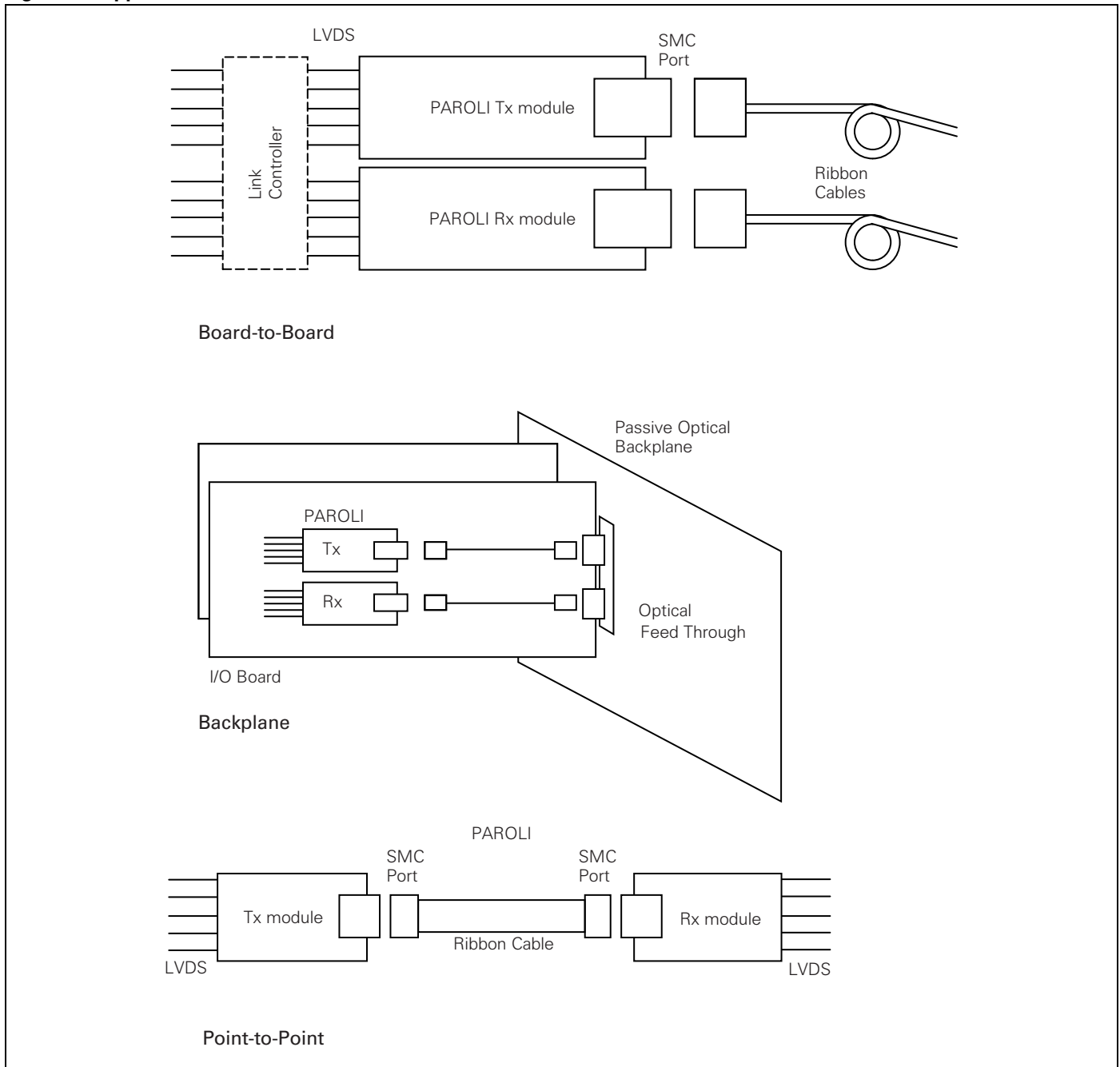


No electronic components are allowed on the customer PCB within the area covered by the PAROLI module and the jumper used to attach a ribbon fiber cable.

Figure 14. Mounting hole, Detail Y



**Figure 15. Applications**



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