Errata Sheet

Rel. 1.3, 2018-06-11

Device	**TC23x**
Marking/Step	**ES-AC, AC**
Package	**see Data Sheet**

No. 063/18

This Errata Sheet describes the deviations from the current user documentation.

Table 1 Current Documentation[1)]

TC21x/TC22x/TC23x User's Manual	V1.1	2014-12
TC233/TC234/TC237 AC-Step Data Sheet	V1.0	2017-03
TriCore TC1.6P & TC1.6E Core Architecture, Instruction Set	V1.0D10, V1.0D15	2012-02, 2013-07

1) Newer versions replace older versions, unless specifically noted otherwise.

Make sure you always use the corresponding documentation for this device (User's Manual, Data Sheet, Documentation Addendum (if applicable), TriCore Architecture Manual, Errata Sheet) available in category 'Documents' at **www.infineon.com/AURIX** and **www.myInfineon.com**.

Conventions used in this document

Each erratum identifier follows the pattern **Module_Arch.TypeNumber**:

- **Module**: subsystem, peripheral, or function affected by the erratum
- **Arch**: microcontroller architecture where the erratum was initially detected
  - **AI**: Architecture Independent
  - **TC**: TriCore
- **Type**: category of deviation
  - **[none]**: Functional Deviation
  - **P**: Parametric Deviation

  - **H**: Application Hint
  - **D**: Documentation Update
- **Number**: ascending sequential number within the three previous fields. As this sequence is used over several derivatives, including already solved deviations, gaps inside this enumeration can occur.

Notes

1. This Errata Sheet applies to all temperature and frequency versions and to all memory size variants, unless explicitly noted otherwise. For a derivative synopsis, see the latest Data Sheet/User's Manual.
   This Errata Sheet covers several device versions. If an issue is related to a particular module, and this module is not specified for a specific device version, this issue does not apply to this device version.
   E.g. issues with identifier "ETH" only apply to devices with a specific extended feature set.
2. Devices marked with EES or ES are engineering samples which may not be completely tested in all functional and electrical characteristics, therefore they should be used for evaluation only.
   The specific test conditions for EES and ES are documented in a separate Status Sheet.
3. This device is equipped with TriCore "TC1.6E" core(s). Some of the errata have workarounds which are possibly supported by the tool vendors. Some corresponding compiler switches need possibly to be set. Please see the respective documentation of your compiler.
   For effects of issues related to the on-chip debug system, see also the documentation of the debug tool vendor.

1 History List / Change Summary

Table 2 History List

Version	Date	Remark
1.0	2016-10-21	• New/updated text modules see columns “Change” in tables 4..6 of errata sheet V1.0. • The following text modules have been removed, as no device variant exists of this design step (AC) that includes EMEM, ETH, FFT modules: – EMEM_TC.H002 (EMEM will raise ECC errors when not properly initialized) – ETH_AI.003 (Overflow Status bits of Missed Frame and Buffer Overflow counters get cleared without a Read operation) – ETH_AI.H001 (Sequence for Switching between MII and RMII Modes) – ETH_TC.004 (DMA Access to Reserved/Protected Resources: FPI Error Response not correctly evaluated) – ETH_TC.H002 (Minimum operation frequency for Ethernet MAC) – ETH_TC.H003 (Interrupt Generation by Wake-up or Magic Packet Frames) – FFT_TC.001 (FFT Access with disabled FFT Module) – FFT_TC.002 (FFT Kernel Reset Function) – FFT_TC.003 (No Error reported upon Write to FFT Registers in User Mode) • The following text module has been removed, as no ADAS variant exists of this design step (AC) – SCU_TC.H012 (Overlay Feature for ADAS Variants)

Table 2 History List (cont'd)

Version	Date	Remark
1.1	2017-03-31	• New/updated text modules see columns "Change" in tables 4..6 of errata sheet V1.1. • Removed reference to "GTM-IP 210 Errata Sheet" in Table 1 - all GTM errata relevant for this design step are considered in this TC23x errata sheet • The following text modules have been included in Table 3 (Errata fixed in this step): – ADC_TC.P007 (Additional Parameter for Data Sheet: Wakeup Time t_{WU}): see specification of t_{WU} in TC23x AC-Step Data Sheet – I0_TC.P003 (Calculating the 1.3 V Current Consumption for TC23x): see corresponding section in TC23x AC-Step Data Sheet – PADS_TC.P007 (Connection of Ball U17 in LFBGA-292 Package): see chapter "Package and Pinning Definitions" in TC23x AC-Step Data Sheet
1.2	2017-11-03	• Update: new/updated text modules see columns "Change" in tables 4..6 of errata sheet V1.2.
1.3	2018-06-11	• New/updated text modules see columns "Change" in tables 4..6 • Replaced: – DMA_TC.029 (DMA Double Buffering Overflow), – DMA_TC.047 (DMA Double Buffering Buffer Switch), – DMA_TC.057 (Double Buffering Overflow Causes Other Channel Corruption) – >> replaced by DMA_TC.061 (DMA Double Buffering Operations)

Table 2 History List (cont'd)

Version	Date	Remark
... 1.3 (cont'd)	...	... • Removed: – GTM_TC.010 (Effects of GTM Resets) - TC23x..TC21x do not have GTM SRAM

Table 3 Errata fixed in this step

Errata	Short Description	Change
ADC_TC.P007	Additional Parameter for Data Sheet: Wakeup Time t_{WU}	Fixed
CCU_TC.002	Clock Monitors - Target Monitoring Frequency Selection	Fixed
CCU_TC.003	Maximum Amplitude for Frequency Modulation	Fixed
FLASH_TC.044	Repetitive Erase Suspend Requests on Data Flash	Fixed
I0_TC.P003	Calculating the 1.3 V Current Consumption for TC23x	Fixed
MTU_TC.016	Wrong Address(es) Tracked in Registers ETRRx of TC1.6E CPU0 PSPR and DSPR	Fixed
MultiCAN_AI.047	Transmit Frame Corruption after Protocol Exception (CAN FD only)	Fixed
MultiCAN_TC.043	CAN FD: Idle Condition	Fixed (node 0,1 only)
MultiCAN_TC.044	CAN FD: Missing Hardsync	Fixed (node 0,1 only)

Table 3 Errata fixed in this step (cont'd)

Errata	Short Description	Change
PADS_TC.P007	Connection of Ball U17 in LFBGA-292 Package	Fixed
RESET_TC.007	Unexpected SMU Reset during SSW execution if no HARR requested	Fixed
SMU_TC.005	Unexpected/Incorrect Reset caused by SMU Alarms	Fixed

Note: Changes to the previous errata sheet version are particularly marked in column "Change" in the following tables.

Table 4 Functional Deviations

Functional Deviation	Short Description	Change	Page
ADC_AI.016	No Channel Interrupt in Fast Compare Mode with GLOBRES		24
ADC_TC.068	Effect of VAGND Cross Coupling on Conversion Result		24
ASCLIN_TC.004	SLSO in SPI mode still active after module disable		27
ASCLIN_TC.005	Unjustified collision detection error in half-duplex SPI mode		27
ASCLIN_TC.006	Unjustified response timeout in LIN slave mode		28
ASCLIN_TC.007	Break Detected in LIN Frames in Soft Suspend mode		28
ASCLIN_TC.008	Response timeout in LIN Mode in case of header only		28
ASCLIN_TC.009	RFL flag set in Buffer Mode when Receive FIFO Inlet is disabled		29

Table 4 Functional Deviations (cont'd)

Functional Deviation	Short Description	Change	Page
ASCLIN_TC.010	Flush of TXFIFO leads to frame transmission		29
BROM_TC.008	Sporadic Power-on Reset after Wake-up from Standby Mode		30
CPU_TC.123	Data Corruption possible when CPU GPR accesses made via SRI slave with CPU running		30
CPU_TC.127	Pending Interrupt Priority Number PIPN in Register ICR		31
DAP_TC.002	DAP client_blockread has Performance issue in Specific Operation Modes		31
DAP_TC.003	DAP CRC32 definition and algorithm		32
DAP_TC.004	DAP client_blockwrite telegram with CRC6 and CRC32 protection options		33
DAP_TC.005	DAP client_read: dirty bit feature of Cerberus' Triggered Transfer Mode		34
DAP_TC.006	CRC6 error in telegram following a get_CRCdown telegram prevents reset of CRC32 calculator		34
DAP_TC.007	Incomplete client_blockread telegram in DXCM mode when using the "read CRCup" option		35
DAP_TC.009	CRC6 error in client_blockwrite telegram	New	35
DMA_TC.015	DMA Double Buffering: No Timestamp Support		36
DMA_TC.016	Byte and Half-word Write Accesses to specific Registers not supported		36
DMA_TC.017	Pattern Detection Double Interrupt Trigger when INTCT = 11_B		37

Table 4 Functional Deviations (cont'd)

Functional Deviation	Short Description	Change	Page
DMA_TC.018	FPI timeout can cause pipelined register reads to break		38
DMA_TC.019	CBS Accesses with Large SPB:SRI Clock Ratios Configured		38
DMA_TC.020	DMA Conditional Linked List: Circular Buffer Enabled		38
DMA_TC.021	Combined Software/Hardware Controlled Mode Spurious Errors		39
DMA_TC.022	Conditional Linked List: Bus Error		39
DMA_TC.024	Suspend Request coincident with Channel Activation		40
DMA_TC.025	Conditional Linked List: new non-CLL mode TCS load can corrupt SDCRC RAM write		41
DMA_TC.026	Linked List: Failed TCS load can trigger wrap interrupt		41
DMA_TC.028	Transaction Request Lost (TRL) Interrupt Service Request Behaviour	Update	41
DMA_TC.031	CHCSR.ICH can be incorrectly set after pattern match		42
DMA_TC.034	DMA Timestamp and Destination Circular Buffer	Update	42
DMA_TC.035	Last DMA Transaction in a Linked List triggers a DMA Daisy Chain		44
DMA_TC.036	Linked List: SADR/DADR can be overwritten when loading a non-LL TCS		44
DMA_TC.037	Conditional Linked List: Bit TSR.CH not cleared for a CLL transaction upon pattern match		45

Table 4 Functional Deviations (cont'd)

Functional Deviation	Short Description	Change	Page
DMA_TC.038	Linked List: SIT interrupt when SIT bit set in newly loaded TCS		45
DMA_TC.039	Read Data CRC		46
DMA_TC.040	DMA Linked Lists: Intermittent Clearing of Hardware Transaction Request Enable with mixed mode Transaction Control Sets		46
DMA_TC.041	DMA Circular Buffer Wrap Interrupt		47
DMA_TC.042	DMA Interrupt from Channel reported before Completion of DMA Transaction		48
DMA_TC.043	DMA Write Move Data Corruption for non 32-byte Aligned Cacheable Source Address		48
DMA_TC.044	Clock Switch after SPB Error Reported results in Spurious SRI Error		49
DMA_TC.045	DMA Reconfigures DMA Channels Lockup		49
DMA_TC.046	Shadow Operation Read Only Mode		50
DMA_TC.049	Bus Error Reported During LL TCS Load		50
DMA_TC.050	Clearing CHCSR.FROZEN during Double Buffering		51
DMA_TC.052	SER and DER During Linked List Operations	Update	51
DMA_TC.053	TS16_ERR Type of Error Reporting Unreliable		52
DMA_TC.054	DMA Channel Halt Acknowledge Unreliable		52
DMA_TC.055	ICU to DMA Interface in Sleep Mode		53
DMA_TC.056	TSR and SUSENR Access Protection Unreliable		53
DMA_TC.058	Linked List Load Transaction Control Set (TCS) Integrity Error		55

Table 4 Functional Deviations (cont'd)

Functional Deviation	Short Description	Change	Page
DMA_TC.061	DMA Double Buffering Operations	New	56
DMA_TC.062	Termination of DMA Transaction for Pattern Match	New	58
DMA_TC.063	DMA Timestamp Destination Address	New	59
DMA_TC.064	DMA Daisy Chain Request	New	59
DMA_TC.065	DMA Move Concurrent Bus Accesses	New	60
DTS_TC.001	Temperature Sensor Formula		60
FlexRay_AI.087	After reception of a valid sync frame followed by a valid non-sync frame in the same static slot the received sync frame may be ignored		61
FlexRay_AI.088	A sequence of received WUS may generate redundant SIR.WUPA/B events		61
FlexRay_AI.089	Rate correction set to zero in case of SyncCalcResult=MISSING_TERM		62
FlexRay_AI.090	Flag SFS.MRCS is set erroneously although at least one valid sync frame pair is received		63
FlexRay_AI.091	Incorrect rate and/or offset correction value if second Secondary Time Reference Point (STRP) coincides with the action point after detection of a valid frame		64
FlexRay_AI.092	Initial rate correction value of an integrating node is zero if pMicroInitialOffsetA,B = 0x00		64
FlexRay_AI.093	Acceptance of startup frames received after reception of more than gSyncNodeMax sync frames		65
FlexRay_AI.094	Sync frame overflow flag EIR.SFO may be set if slot counter is greater than 1024		66

Table 4 Functional Deviations (cont'd)

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FlexRay_AI.096	Noise following a dynamic frame that delays idle detection may fail to stop slot		67
FlexRay_AI.097	Loop back mode operates only at 10 MBit/s		68
FlexRay_AI.099	Erroneous cycle offset during startup after abort of startup or normal operation		68
FlexRay_AI.100	First WUS following received valid WUP may be ignored		69
FlexRay_AI.101	READY command accepted in READY state		70
FlexRay_AI.102	Slot Status vPOC!SlotMode is reset immediately when entering HALT state		71
FlexRay_AI.103	Received messages not stored in Message RAM when in Loop Back Mode		71
FlexRay_AI.104	Missing startup frame in cycle 0 at coldstart after FREEZE or READY command		72
FlexRay_AI.105	RAM select signals of IBF1/IBF2 and OBF1/OBF2 in RAM test mode		73
FlexRay_AI.106	Data transfer overrun for message transfers Message RAM to Output Buffer (OBF) or from Input Buffer (IBF) to Message RAM		74
GTM_AI.132	GTM_TOP level: AEI write to BRIDGE_MODE register can result in blocking of AEI configuration interface		77

Table 4 Functional Deviations (cont'd)

Functional Deviation	Short Description	Change	Page
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GTM_AI.142	TIM: Incorrect data captured to GPR registers and routed via ARU when EGPRi_SEL,GPRi_SEL= 100 in TIM channel mode TBCM		79
GTM_AI.143	GTM_TOP level: AEI pipelined write to GTM_BRIDGE_MODE register directly after setting aei_reset='0' can result in blocking of AEI configuration interface		80
GTM_AI.144	TIM: TIM interrupts as trigger source from TIM to TOM/ATOM not functional		80
GTM_AI.153	TIM: Incorrect data captured to CNTS register when TIM channel operates in mode TPWM or TPIM and CNTS_SEL = 1 and selected CMU_CLK ≠ sys_clk		81
GTM_AI.154	TOM: Incorrect duty cycle in PCM mode (bit reversed mode)		82
GTM_AI.157	CMU: Incorrect AEI status by writing 1 to bit 24 of register CMU_CLK_6/7_CTRL		82
GTM_AI.163	TIM: timeout signaled when TDU unit is reenabled		83
GTM_AI.164	TIM: capturing of data into TIM[i]_CH[x]_CNTS with setting CNTS_SEL=1 not functional in TPWM and TPIM mode		84
GTM_AI.181	TIM: Incorrect signal level bit ECNT[0] in mode TIEM, TPWM, TIPM, TPIM, TGPS		84

Table 4 Functional Deviations (cont'd)

Functional Deviation	Short Description	Change	Page
GTM_AI.202	(A)TOM: no CCU1 interrupt in case of CM1=0 or 1 and RST_CCU0=1		85
GTM_AI.205	TIM: unexpected CNTS register update in TPWM OSM mode		86
GTM_AI.209	TOM/ATOM: no update of CM0/CM1/CLK_SRC via trigger signal from preceding instance if selected CMU_CLKx is not SYS_CLK		86
GTM_AI.270	(A)TOM: output signal is postponed one period for the values CM0=1 and CM1>CM0 if CN0 is reset by the trigger of a preceding channel (RST_CCU0=1)		87
GTM_AI.298	TOM/ATOM: wrong output behaviour in SOMP oneshot mode when oneshot pulse is triggered by TIM_EXT_CAPTURE(x)29		88
GTM_AI.299	TOM/ATOM: wrong output behaviour in SOMP oneshot mode when oneshot pulse is triggered by trig_[x-1]		89
GTM_TC.009	TBU signals not wired to debug logic		89
GTM_TC.012	Read Access Control by Register ODA		90
IOM_TC.002	Missed or spurious IOM events when pulse length exceeds Event Window counter range		91
IOM_TC.003	Unexpected Event upon Kernel Reset		91
IOM_TC.004	Write to IOM register space when IOM_CLC.RMC > 1		92
MTU_TC.005	Access to MCx_ECCD and MCx_ETRRi while MBIST disabled		92
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Table 4 Functional Deviations (cont'd)

Functional Deviation	Short Description	Change	Page
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MultiCAN_TC.044	CAN FD: Missing Hardsync		96
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OCDS_TC.042	OTGS capture registers can miss single clock cycle triggers		99
OCDS_TC.043	Read-Modify-Write Bus Transactions to Cerberus Registers		99
PLL_ERAY_TC.001	PLL_ERAY Initialization after Cold Power-up or Wake-up from Standby mode		100
PLL_TC.005	PLL Initialization after Cold Power-up or Wake-up from Standby mode		100
PMC_TC.002	Switch Capacitor Regulator Mode, Frequency Spreading - Documentation Update to Register EVRSDCTRL1		101
PMC_TC.003	Usecase limitation of LDO mode with on chip pass device for SAL devices		103
QSPI_TC.006	Baud rate error detection in slave mode (error indication in current frame)		104
RESET_TC.005	Indication of Power Fail Events in SCU_RSTSTAT		104
SMU_TC.006	OCDS Trigger Bus OTGB during Application Reset		105
SMU_TC.007	Size and Position of Field ACNT in Register SMU_AFCNT		105
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Table 4 Functional Deviations (cont'd)

Functional Deviation	Short Description	Change	Page
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IDD_TC.H001	IPC Limits used in Production Test for IDD Max Power Pattern		110
PADS_TC.H004	PN-Junction Characteristics for Pad Type S		111
RTH_TC.H001	Thermal characteristics of the package - Footnote update for LF-BGA-292-6 package	New	111
VDDPPA_TC.H001	Voltage to ensure defined pad states - Footnote update	New	111

Table 6 Application Hints

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ADC_TC.H015	Conversion Time with Broken Wire Detection		115
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Table 6 Application Hints (cont'd)

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CCU_TC.H005	References to f_{PLL2}, f_{PLL2_ERAY} and K3 Divider in User's Manual		124
CCU_TC.H006	Clock Monitor Support - Documentation Update		125
CCU_TC.H007	Oscillator Watchdog Trigger Conditions for ALM3[0]		125
CPU_TC.H006	Store Buffering in TC1.6/P/E Processors		126
CPU_TC.H008	Instruction Memory Range Limitations		128
CPU_TC.H009	Details on CPU Clock Control		129
CPU_TC.H012	Behavior of bit-wise operations on certain peripheral register bits which need to be written back with the same value		129
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CPU_TC.H015	Register Access Modes for Safety Protection Registers - Documentation Update	New	131
DAP_TC.H002	DAP client_blockread in Combination with TGIP and all Parcels with CRC6		131
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Table 6 Application Hints (cont'd)

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DMA_TC.H009	Resetting Bits ICH and IPM in register CHCSRz		136
DMA_TC.H010	Calculation of DMA Address Checksum for DMA read moves to Cacheable Addresses		137
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Table 6 Application Hints (cont'd)

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2 Functional Deviations

ADC_AI.016 No Channel Interrupt in Fast Compare Mode with GLOBRES

In fast compare mode, the compare value is taken from bitfield RESULT of the selected result register and the result of the comparison is stored in the respective bit FCR.

A channel event can be generated when the input becomes higher or lower than the compare value.

In case the global result register GLOBRES is selected, the comparison is executed correctly, the target bit is stored correctly, source events and result events are generated, but a channel event is not generated.

Workaround

If channel events are required, choose a local result register GxRESy for the operation of the fast compare channel.

ADC_TC.068 Effect of VAGND Cross Coupling on Conversion Result

Due the implementation of the clock dividers as fractional dividers, a statistical phase shift of one f_{VADC} clock can occur between the operation of different converter groups. If the last f_{VADC} clock of the sample phase of a converter group Gx coincides with the first f_{VADC} clock of a conversion step of (one or more) other converter groups Gy, the Total Unadjusted Error (TUE) of the conversion result of Gx is increased due to cross coupling via VAGND.

For TC26x, TC23x, TC22x, and TC21x, the TUE is increased up to ± 25 LSB_{12}

Workarounds - Introduction

Workaround 1..3 may be used with any device step.

Workaround 4 can only be used with TC21x, TC22x, TC23x ≥ step AB.

Workaround 1

Synchronize the trigger events of different converter groups as follows:

- Operate the arbiters and the analog parts of the VADC at the same clock frequency, i.e. select the divider factors DIVA and DIVD in register GLOBCFG such that $f_{ADCD} = f_{ADCI}$ for all converter groups:
  - Note: As $f_{ADCD} = f_{VADC}/4$ with the maximum divider (DIVD = 3), this implies that $f_{VADC} = f_{SPB}$ must be limited to 80 MHz to achieve $f_{ADCD} = f_{ADCI}$ with the error limits specified for f_{ADCI} = 20 MHz in the Data Sheet.
- Enlarge the length of an arbitration round to a minimum of 16 arbitration slots (i.e. bit field GxARBCFG.ARBRND ≥ 2 for any x).
- Select the conversion time (including sample time) of the longest conversion of any group Gx to be shorter than two arbitration rounds. This ensures that all converters are idle when the arbiters have determined the next conversion request.
- Synchronize the digital and the analog clock by switching off/on the Module Disable Request bit, i.e. set CLC.DISR = 1_B and then CLC.DISR = 0_B.
- Initiate the start-up calibration by setting bit GLOBCFG.SUCAL = 1_B (mandatory after switching off/on VADC clocks via CLC.DISR).

Workaround 2

Ensure that conversions never overlap for any two converter groups Gx and Gy.

This may be achieved under software control, or by exclusively using the VADC background request source.

For this workaround, no restrictions apply on clock and arbitration round settings.

Workaround 3

Use the converters within a synchronization group in master/slave configuration, such that they are synchronized for parallel sampling, triggered by one common master. In this case, the cross coupling effect will not occur as long as only one synchronization group is performing conversions.

For devices that support more than one synchronization group, operate the synchronization groups in an interleaving manner.

For this workaround, no restrictions apply on clock and arbitration round settings.

Workaround 4

To avoid the cross coupling effect, this device step (see “Workarounds - Introduction” above) supports selection of signal CCU6061_TRIG1 to synchronize the start of the converter groups to a raster of $5/f_{SPB}$ (i.e. 50 ns @f_{SPB} = 100 MHz). The resulting jitter (delay from trigger to start of conversion) is thus limited to max. $5/f_{SPB}$.

For this workaround, either CCU60_T13 or CCU61_T13 is configured (reserved) to provide the synchronization signal. The selection is performed via bit field TRIG1SEL in register CCU60_MOSEL:

- TRIG1SEL = 000_B: signal CCU60_COUT63 from CCU60_T13 is selected
- TRIG1SEL = 001_B: signal CCU61_COUT63 from CCU61_T13 is selected

The synchronization signal is enabled inside the VADC module by setting bit GLOBCFG.DCMSB = 1_B. The default function of this bit (DCMSB = 0_B: one clock cycle for MSB conversion step) is hardwired and thus stays unaffected.

The following examples describe the initialization of CCU60 or CCU61, respectively, to provide a 20 MHz synchronization signal @f_{SPB} = 100 MHz:

Example for CCU60 initialization

```
CCU60_CLC = 0x0;        // enable CCU60 kernel
CCU60_T13PR = 0x4;      // 4+1 clock periods with ..
CCU60_CC63SR = 0x1;     // duty cycle 40 ns low / 10 ns high
CCU60_PSLR |= 0x0080;   // passive state level of COUT63 = 1
CCU60_MODCTR |= 0x8000;// ECT13O = 1 enables T13 output
                        //  (CC63ST -> COUT63)
CCU60_TCTR4 |= 0x4200; //set bit T13STR and T13RS ..
                // to enable shadow transfer and start T13
CCU60_MOSEL &= 0x1C7;  // CCU6061_TRIG1 is CCU60_COUT63
```

Example for CCU61 initialization

```
CCU61_CLC = 0x0;        // enable CCU61 kernel
```

Note: In case an application only uses kernel CCU61, ensure that kernel CCU60 is also clocked until register CCU60_MOSEL is configured.

```
CCU60_CLC = 0x0;        // ensure CCU60 kernel is clocked
                        // until CCU60_MOSEL is configured
CCU61_T13PR = 0x4;      // 4+1 clock periods with ..
CCU61_CC63SR = 0x1;     // duty cycle 40 ns low / 10 ns high
CCU61_PSLR |= 0x0080;  // passive state level of COUT63 = 1
CCU61_MODCTR |= 0x8000;// ECT13O = 1 enables T13 output
                        //  (CC63ST -> COUT63)
CCU61_TCTR4 |= 0x4200; //set bit T13STR and T13RS ..
                 // to enable shadow transfer and start T13
CCU60_MOSEL |= 0x8;     // CCU6061_TRIG1 is CCU61_COUT63
```

ASCLIN_TC.004 SLSO in SPI mode still active after module disable

It is expected that in SPI mode, after module disable, the Slave Select Output signal SLSO should be in idle state according to configuration of Slave Polarity in Synchronous mode (IOCR.SPOL).

However, in this design step, when the module is disabled, the Slave Select Output signal SLSO is always 0 (low) independent of IOCR.SPOL, i.e., it is still active even when IOCR.SPOL = 1_B.

Workaround

Before disabling the ASCLIN module, set SLSO to the desired level in the corresponding Port control registers.

ASCLIN_TC.005 Unjustified collision detection error in half-duplex SPI mode

In Half Duplex SPI mode, when collision detection is enabled and the number of stop bits in SPI frame is configured as any value from 1 to 7 in FRAMECON.STOP, a Collision Error (FLAGS.CE) is triggered during the trailing phase (i.e., during stop bits), although RX and TX signal are identical.

Workaround

In half-duplex SPI mode, set FRAMECON.STOP = 0 if trailing phase is irrelevant, or ignore/disable collision error if FRAMECON.STOP > 0.

ASCLIN_TC.006 Unjustified response timeout in LIN slave mode

When ASCLIN is configured as LIN slave and Response timeout is configured as DATCON.RM = 1_B, Response timeout is triggered even when an incomplete LIN Header frame is received. The timeout counter runs further after Header timeout detection without reset and triggers Response Timeout when it reaches the Response Timeout Threshold value defined by DATCON.RESPONSE.

Workaround

Ignore the Response Timeout which comes directly after a Header Timeout has occurred and before the next break is detected.

ASCLIN_TC.007 Break Detected in LIN Frames in Soft Suspend mode

When ASCLIN has entered Soft Suspend mode (OCS.SUS = 0x2), it still detects a Break Field in LIN frames and triggers an interrupt if enabled (FLAGSENABLE.BDE = 1_B).

Workaround

Ignore a detected break event when the module has been soft-suspended (e.g. set FLAGSENABLE.BDE = 0_B when using soft suspend mode).

ASCLIN_TC.008 Response timeout in LIN Mode in case of header only

In LIN (Master/Slave) mode, when Header Only (DATCON.HO = 1_B) is configured, Response timeout could occur even though no Response frame is expected.

Workaround

To avoid the unwanted interrupt, disable the interrupt on Response Timeout by FLAGSENABLE.RTE = 0_B whenever Header Only (DATCON.HO = 1_B) is configured.

ASCLIN_TC.009 RFL flag set in Buffer Mode when Receive FIFO Inlet is disabled

When RXFIFO is configured in Buffer Mode (RXFIFOCON.BUF = 1_B) and Receive FIFO Inlet is disabled (RXFIFOCON.ENI = 0_B), the receive FIFO level flag is set (FLAGS.RFL = 1_B) even though RXFIFO is not filled with new incoming data.

Workaround

To avoid the unwanted Receive FIFO Level interrupt, disable it by setting FLAGSENABLE.RFLE = 0_B whenever Receive FIFO Inlet is disabled (RXFIFOCON.ENI = 0_B),

ASCLIN_TC.010 Flush of TXFIFO leads to frame transmission

When the TXFIFO is flushed (TXFIFIOCON.FLUSH = 1_B), it triggers transmission of a frame in the following corner case:

- Starting condition:
  - TXFIFO is not empty and TXFIFOCON.ENO = 0_B
- Triggering condition:
  - Write to TXFIFOCON with both TXFIFOCON.FLUSH = 1_B and TXFIFOCON.ENO = 1_B

Workaround

Do not flush TXFIFO and change bit TXFIFOCON.ENO from 0_B to 1_B in one single write to TXFIFOCON if TXFIFO is not empty.

BROM_TC.008 Sporadic Power-on Reset after Wake-up from Standby Mode

On a wake-up from Standby mode, the Standby RAM redundancy installation procedure is executed. In case there is a sporadic Power-on reset in a time window between 600 µs - 1 ms after Standby mode wake-up, it can happen that the application data stored in specific Standby RAM cells are overwritten.

Note: This effect can occur only on devices where non-zero data are stored in CPU0 DSPR at locations D000 2000$_H$ to D000 203F$_H$ by the Startup Software (SSW) after cold power-on (see section "Preparation before to enter Stand-by mode" in the BootROM chapter of the User's Manual). Only CPU0 DSPR Standby RAM is affected, EMEM in ADAS or ED devices is not affected.

Workarounds

1. Calculate CRC over critical Standby RAM data and store result before Standby mode entry. On a consequent wake-up, CRC of the critical data shall be carried out. The CRC is a general recommended measure for improved robustness of Standby RAM handling.
   Or / and
2. Keep a copy of the critical data at a second location in Standby RAM. On wake-up, compare data from both locations to ascertain their integrity.

CPU_TC.123 Data Corruption possible when CPU GPR accesses made via SRI slave with CPU running

Data corruption may occur when another master accesses a TriCore CPU's General Purpose Registers (GPRs) via its SRI slave port whilst the CPU is running (i.e. not Idle, Halted or Suspended). The TriCore GPRs are A0-A15 and D0-D15. The scenarios in which data corruption may occur are different for the TC1.6P and TC1.6E processors as described below.

TC1.6P - Data corruption may occur when one of the CPU GPRs is **written** via the SRI slave port whilst the CPU is running. Both AGPR and DGPR writes may be affected.

TC1.6E - Data corruption may occur when one of the CPU Address GPRs (A0-A15) is **read** via the SRI slave port whilst the CPU is running. However, data corruption can only occur when the slave AGPR read interacts with the execution of a specific form of store instruction. The store instructions affected by this issue are ST.A and ST.DA, where the address register to be stored is modified by the addressing mode of the store instruction. For example:

```
ST.A [+A0], A0
```

However, such store instructions are architecturally undefined and should not be being used. In the case of this errata all data written to memory by this store instruction may be corrupted.

Workaround

Writes to a CPU's GPRs via its SRI slave port must never be performed whilst the CPU is running. If it is necessary for an external master to write to a CPU's GPR then that CPU must first be placed in Idle, Halt or Suspend mode.

If it is necessary for an external master to read a TC1.6E CPU's AGPR whilst that CPU is running then store instructions of the form above (where any source register is modified by the addressing mode of the store instruction) are not allowed.

CPU_TC.127 Pending Interrupt Priority Number PIPN in Register ICR

In the TriCore Architecture Manual, it is described for the Pending Interrupt Priority Number ICR.PIPN that it is reset to 0x0 in case there is no request pending.

However, the AURIX™ hardware implementation behaves differently, as the value of PIPN is not changed after the interrupt is serviced in case there is no further request pending.

DAP_TC.002 DAP client_blockread has Performance issue in Specific Operation Modes

For achieving the highest block read bandwidth, the following word is already read chip internally while a word is transmitted on DAP. This read ahead is

under certain conditions disabled in the case that the “All parcels with CRC6” bit is set in the telegram. In this case the distance between the reply parcels becomes significantly longer, due to the missing read ahead. This effect occurs also in Wide Mode.

The data values in the parcels are always correct, it is just a performance issue.

Workaround

Don’t use the “All parcels with CRC6” option, use “Read CRCup” instead.

This mode is anyway better in terms of performance for larger blocks (no CRC6 overhead for each parcel) and data protection (32 bit CRC). For a few words, the impact of this performance issue might be tolerable. For the first word a read ahead is not possible anyway.

DAP_TC.003 DAP CRC32 definition and algorithm

The DAP CRC32 algorithm is different from the IEEE 802.3 Ethernet CRC.

Workaround

Use the following (VHDL) algorithm for each incoming data bit. The CRC32 value is initialized with all ones.

In Wide Mode the function is called for both DAP data bits in each DAP0 clock cycle.

```
subtype  crc32_t is std_ulogic_vector(31 downto 0);
function calc_crc32_f(crc_now : crc32_t;
                      bit_new : std_ulogic)
                     return crc32_t is
  variable crc : crc32_t;
begin
  crc(31 downto 1) := crc_now(30 downto 0);
  crc(0)  := bit_new xor crc_now(31);
  crc(1)  := bit_new xor crc_now(0)  xor crc_now(31);
  crc(2)  := bit_new xor crc_now(1)  xor crc_now(31);
  crc(4)  := bit_new xor crc_now(3)  xor crc_now(31);
  crc(5)  := bit_new xor crc_now(4)  xor crc_now(31);
```

```
  crc(7)  := bit_new xor crc_now(6)  xor crc_now(31);
  crc(8)  := bit_new xor crc_now(7)  xor crc_now(31);
  crc(10) := bit_new xor crc_now(9)  xor crc_now(31);
  crc(11) := bit_new xor crc_now(10) xor crc_now(31);
  crc(12) := bit_new xor crc_now(11) xor crc_now(31);
  crc(16) := bit_new xor crc_now(15) xor crc_now(31);
  crc(22) := bit_new xor crc_now(21) xor crc_now(31);
  crc(23) := bit_new xor crc_now(22) xor crc_now(31);
  crc(26) := bit_new xor crc_now(25) xor crc_now(31);
  return crc;
end calc_crc32_f;
```

DAP_TC.004 DAP client_blockwrite telegram with CRC6 and CRC32 protection options

Note: This problem is only relevant for tool development, not for application development.

When issuing a DAP client_blockwrite telegram from the tool to the device several CRC protection options are available, namely CRC6 and CRC32.

Expected Behavior

- For CRC6 the expected behavior is:
  - (1) A CRC6 will be appended to the reply of only the last parcel of the telegram.
  - (2) An optional CRC6 can be appended to the devices “single startbit response” by setting DAPISC.RC6.
- For CRC32 the expected behavior is:
  - (3) The telegram can optionally send the CRCdown value as the last parcel.

Actual Implementation

- For the actual implementation the CRC6 slightly differs as follows:
  - (1) The CRC6 of the last parcel will be erroneous if DAPISC.RC6 is set or if the CRCdown option is enabled.

  - (2) If DAPISC.RC6 = 1_B, an unintentional CRC6 will be appended to the device response of parcels which are not the last parcel.
- For the actual implementation the CRC32 option slightly differs as follows:
  - (3) If also the CRC6option is set, the CRCdown option will not return the correct CRCdown value.

Workaround for (3)

Workaround for (3) is not to use the CRCdown feature of the client_blockwrite telegram, but to use the dedicated get_CRCdown telegram.

DAP_TC.005 DAP client_read: dirty bit feature of Cerberus' Triggered Transfer Mode

Note: This problem is only relevant for tool development, not for application development.

The DAP telegram client_read reads a certain number of bits from an IOclient (e.g. Cerberus). The parameter k can be selected to be zero, which is supposed to activate reading of 32 bits plus dirty bit.

However, in the current implementation, the dirty bit feature does not work correctly.

It is recommended not to use this dirty bit feature, meaning the number k should not evaluate to "0".

DAP_TC.006 CRC6 error in telegram following a get_CRCdown telegram prevents reset of CRC32 calculator

Note: This problem is only relevant for tool development, not for application development.

If a CRC6 error occurs in the telegram following a get_CRCdown telegram the AURIX™ internal CRC32 calculator does not get reset, as is the expected behavior for get_CRCdown.

This effect can lead to unexpected CRC32 values for the next get_CRCdown telegram. This corresponds to the perception of the tool that there has been a CRC32 error, even if the data was transmitted correctly.

Workaround 1

Accept extra traffic for a required retransmission: In this case the tool could see a CRC32 error which is not based on a wrong transmission, but on the missing reset of the AURIX™ internal CRC32 calculator. This would trigger the retransmission of correctly sent data.

Workaround 2

Check for no-reply after a get_CRCdown telegram: If the tool does not receive an answer for the telegram following a get_CRCdown, it needs to re-send the get_CRCdown telegram and ignore the data.

DAP_TC.007 Incomplete client_blockread telegram in DXCM mode when using the “read CRCup” option

In DXCM (DAP over CAN Messages) mode, the last parcel containing the CRC32 might be skipped in a client_blockread telegram using the “read CRCup” option.

Workaround

Do not use CRCup option with client_blockread telegrams in DXCM mode.

Instead the CRCup can be read by a dedicated getCRCup telegram.

DAP_TC.009 CRC6 error in client_blockwrite telegram

Note: This problem is only relevant for tool development, not for application development.

If a CRC6 error happens in a client_blockwrite telegram, the DAP module will not execute the write and the tool will run into timeout according to the DAP protocol.

But in this case a following client_blockwrite (with start address) will be ignored by the DAP module.

Workaround

If the tool is running into a timeout after a client_blockwrite telegram it should transmit a dummy client_blockread telegram (e.g. len=0, arbitrary address) which will clean up the DAP client_blockwrite function.

DMA_TC.015 DMA Double Buffering: No Timestamp Support

When a DMA channel is configured for DMA Double Buffering, and flow control (or appendage of time stamp) is selected, i.e. `DMA_ADICRz.STAMP` = 1_B, the Move Engine may lock up.

Workaround

When a DMA channel is configured for DMA Double Buffering then flow control (or appendage of time stamp) should not be selected, i.e. bit `DMA_ADICRz.STAMP` must be = 0_B.

DMA_TC.016 Byte and Half-word Write Accesses to specific Registers not supported

Note: This erratum might affect the SFR C Header Definitions. In such cases, SFR usage in the software shall be analyzed within the applications for their correct handling.

Byte and half-word write accesses via the SPB (System Peripheral Bus) to the Regfile and Request Control logic are not supported.

This affects the following registers:

- DMA_OTSS (OCDS Trigger Set Select)
- DMA_ERRINTR (Error Interrupt)
- DMA_PRR0 (Pattern Read Register 0)
- DMA_PRR1 (Pattern Read Register 1)
- DMA_MODEy (Hardware Resource Mode)

- DMA_HRRz (Hardware Resource Partition)
- DMA_SUSENRz (Channel Suspend Enable)
- DMA_TSRz (Transaction State)

Workaround

Make sure only 32-bit word data is written to the registers listed above by selecting the appropriate data types.

DMA_TC.017 Pattern Detection Double Interrupt Trigger when INTCT = 11_B

A DMA channel z is configured for pattern detection by programming the DMA_CHCFGRz.PATSEL to reference a data value set in one of the pattern read registers DMA_PRR0 or DMA_PRR1. If DMA_ADICRz.INTCT = 11_B then DMA channel z will generate a channel interrupt trigger and set CHSRz.ICH each time TCOUNT is decremented.

If a pattern match is detected then a channel interrupt trigger will be correctly generated but a second channel interrupt trigger will be generated when TCOUNT decrements. The second interrupt trigger is a bug and should not occur.

If the DMA channel z interrupt trigger is directed via the Interrupt Router to generate a DMA hardware request to another DMA channel then the second interrupt trigger may result in a Transaction Request Lost event.

Workaround

Workaround is to ignore the generation of the Transaction Request Lost event:

- Either disable the generation of error interrupt service requests by setting ADICRz.ETRL = 0_B
- Or if the error interrupt service request is enabled, check all error status bits. If only the TRL bit for DMA channel x (pattern detection channel) is set then clear TRL and continue normal DMA operation.

DMA_TC.018 FPI timeout can cause pipelined register reads to break

Due to a problem in the FPI slave interface (SIF) to the System Peripheral Bus (SPB) in the DMA module, a register access which is pipelined behind an access which is timed-out may terminate early and return the wrong data to the bus.

The scenario for this problem to occur is as follows:

1. An FPI read transaction is performed which takes a long time in the data phase. Pipelined behind this is a register access to DMA or Cerberus.
2. The first transaction is timed out, and in the same cycle the register access is taken by the SIF.

Workaround

Timeout indicates a severe problem, meaning that something took unexpectedly long. In the event of an FPI timeout on the SPB, an error routine should be run to determine the error, and perform a system reset.

DMA_TC.019 CBS Accesses with Large SPB:SRI Clock Ratios Configured

When operating in debug mode and a large SPB:SRI clock ratio is configured then Cerberus accesses to the SRI address space may be unreliable and result in the Cerberus hanging.

Workaround

Limit the SPB:SRI clock ratio to 1:1, 2:1, 3:1 or 4:1, and do not perform Cerberus accesses to the SRI address space while switching the SPB:SRI clock ratio.

DMA_TC.020 DMA Conditional Linked List: Circular Buffer Enabled

When a DMA channel is configured for Conditional Linked List (i.e. ADICRz.SHCT = 1111_B) and circular buffer operation (i.e. ADICRz.SCBE = 1_B OR ADICRx.DCBE = 1_B) then if the source and destination addresses are not

set to wrap boundaries then the behaviour will not be as intended, e.g. the wrap bits CHCSRz.WRPS and CHCESRz.WRPD may be spuriously set.

Workaround

If a DMA channel is configured for Conditional Linked List and circular buffers are enabled then the user must set the source and destination addresses to wrap boundaries.

DMA_TC.021 Combined Software/Hardware Controlled Mode Spurious Errors

A DMA channel is configured for combined software/hardware controlled mode. If the Move Engine is servicing a DMA channel software request and a DMA channel hardware trigger is received then a Transaction Request Lost event is set. When the Move Engine completes the current DMA access the TSRz.CH bit is not cleared. The DMA channel will continue to request channel arbitration as the CH bit is set. If the DMA channel wins arbitration then the Move Engine will continue to service the DMA channel.

In summary, 2 DMA requests (software and hardware) have resulted in 2 X DMA transfers and 1 X Transaction Request Lost (i.e. 3 X DMA actions for 2 X DMA triggers) i.e. a spurious error is generated.

Workaround

If a DMA channel is configured for combined software/hardware mode then increased attention must be paid to de-conflict the triggering of DMA channels from the servicing of DMA requests. The workaround will remove the source of spurious errors.

DMA_TC.022 Conditional Linked List: Bus Error

When a DMA channel is configured for Conditional Linked List (i.e. ADICRz.SHCT = 1111_B) then if a bus error is reported then:

- If there is a pattern match then the number of DMA moves subsequently executed may not be as intended.

- If there is an error during the loading of a new Transaction Control Set then the DMA channel does not clear the TSRz.CH bit and begins the next DMA transaction with an erroneous Transaction Control Set.

Workaround

If a DMA channel is configured for Conditional Linked List then the user must enable the error interrupt service request. On receiving notification of an error interrupt service request the user must read the Move Engine Error Status Registers to confirm that no bus errors were reported:

- If DMA_ERRSRx.DER = 0_B and DMA_ERRSRx.SER = 0_B then no bus errors reported.
- If a bus error is reported then check the last error channel DMA_ERRSRx.LEC.
- If DMA_ERRSRx.DLLER = 1_B then there was an error during the loading of a new Transaction Control Set.

DMA_TC.024 Suspend Request coincident with Channel Activation

If DMA channel z is suspend enabled (SUSENRz.SUSEN = 1_B) and the DMA receives a suspend request then if during the same clock cycle the DMA channel becomes active in a Move Engine, the following effects will occur:

- SUSACRz.SUSAC is set for a cycle and then cleared
- A DMA transfer is performed for DMA channel z
- SUSACRz.SUSAC is set again on completion of the DMA transfer and the DMA channel is finally suspended.

Workaround

When polling SUSACRz.SUSAC in software, additionally check whether DMA channel z is active in a Move Engine x by reading bit field MExSR.CH.

DMA_TC.025 Conditional Linked List: new non-CLL mode TCS load can corrupt SDCRC RAM write

When a Conditional Linked List (CLL) transaction is running and gets a CLL pattern match, this will stop the running transaction and cause a transaction control set (TCS) load.

In case the new TCS load is set up so that it is not in CLL mode, then the SDCRC value of the new TCS may get corrupted.

Workaround

Avoid selection of non-CLL mode in the TCS loaded after a CLL pattern match.

DMA_TC.026 Linked List: Failed TCS load can trigger wrap interrupt

When a Transaction Control Set (TCS) linked list load is performed, and an error is received during the load process, this terminates the load. A DMA linked list error is indicated by the error status flag ERRSRx.DLLER.

If the DADR address left in the register matches the destination wrap boundary, this results in the issuing of a destination wrap interrupt in case the destination wrap interrupt enable is set. Hence a failed TCS load has triggered an interrupt.

Note: This only happens for destination interrupts. Logic is already in place to exclude source interrupts.

Workaround

An error interrupt for the DMA linked list error is triggered by the status flag ERRSRx.DLLER if enabled by EERx.ELER. Therefore the destination wrap buffer interrupt can be ignored in this case.

DMA_TC.028 Transaction Request Lost (TRL) Interrupt Service Request Behaviour

The DMA channel TRL error interrupt service request is a DMA safety measure signalling a lost DMA request to the system. For each DMA channel TRL event, the DMA may trigger one or more error interrupt service requests.

The application software should include a DMA error handler to resolve all DMA errors including TRL.

Workaround

None.

DMA_TC.031 CHCSR.ICH can be incorrectly set after pattern match

If a pattern match is seen during a transaction, the transaction is halted for the current active channel. The move engine zeroes its internal move counter, and holds the transfer count status MEx_CHCSR_TCOUNT at the last value. However, the MEx_CHCSR.ICH bit will still be set indicating a TCOUNT decrement.

Workaround

As there is a pattern match, a DMA channel pattern match interrupt service request will be generated. The pattern match interrupt routine can service the interrupt and clear the status bits including ICH.

DMA_TC.034 DMA Timestamp and Destination Circular Buffer

The DMA must not write a DMA timestamp at an address that overwrites DMA move data stored at a DMA destination address. If the DMA channel is configured for linear DMA destination address generation (DMA channel ADICRz.DCBE = 0_B), the DMA appends the DMA timestamp to the end of a DMA transaction (i.e. beyond the last DMA write move data).

If the DMA channel is configured for destination circular buffer (DMA channel ADICRz.DCBE = 1_B), there are three use cases:

- **Use Case 1:** the size of the DMA transaction **equals** the size of the destination circular buffer. If the DMA writes the last DMA write move data at the last address in the destination circular buffer, the DMA correctly writes the DMA timestamp beyond the destination circular buffer.
- **Use Case 2:** the size of the DMA transaction is **less than** the size of the destination circular buffer. If the DMA writes the last DMA write move data

NOT at the last address in the destination circular buffer, the DMA writes the DMA timestamp inside the destination circular buffer. Erroneously, the DMA may store the DMA timestamp at an address that overwrites DMA write move data.

- **Use Case 3:** the size of the DMA transaction is **greater than** the size of the destination circular buffer. After the DMA destination address has wrapped, the DMA will overwrite DMA write move data with fresh DMA write move data.

Note: DMA Timestamp works as specified when using only source circular buffer.

Workaround 1

If a DMA channel is configured

- for destination circular buffering (ADICRz.DCBE = 1_B) AND
- the appendage of a DMA timestamp (ADICRz.STAMP =1_B), AND
- the size of the DMA transaction (defined by CFCFGRz.TREL) **equals** the size of the destination circular buffer (defined by ADICRz.CBLD),

the DMA shall append the DMA timestamp beyond the destination circular buffer if

- For increment of DMA destination address (ADICRz.INCD = 1_B), the initial DMA destination address is at the bottom of the destination circular buffer.
- For decrement of DMA destination address (ADICRz.INCD = 0_B), the initial DMA destination address is at the top of the destination circular buffer.

Workaround 2

If DMA channel z is configured

- for destination circular buffering (ADICRz.DCBE = 1_B) AND
- increment of DMA destination address (ADICRz.INCD = 1_B) AND
- the appendage of a DMA timestamp (ADICRz.STAMP = 1_B) AND
- the size of the DMA transaction (defined by CFCFGRz.TREL) is **less than** the size of the destination circular buffer (defined by ADICRz.CBLD),

the DMA shall append the DMA timestamp to the DMA write move data if the following DMA channel parameters are configured:

- ADICRz.DMF = 001_B (address offset is 2 x CHCFGRz.CHDW) AND

- CHCFGRz.CHDW = 010_B (32-bit data width for moves, SDTW).

In all other DMA destination circular buffer use cases, the DMA channel shall be configured to disable the appendage of DMA timestamp (ADICRz.STAMP = 0_B).

DMA_TC.035 Last DMA Transaction in a Linked List triggers a DMA Daisy Chain

DMA Channels can be daisy chained by setting the bit CHCFGRz.PRSEL = 1_B. When a higher priority DMA channel z completes a DMA transaction then it will initiate a DMA transaction on the next lower priority DMA channel z-1 by setting the access pending bit TSRz-1.CH.

However, if the current transaction was the last one in a linked list, and PRSEL is set to daisy chain, TSRz-1.CH of the next lower channel z-1 is set just after the TCS (transaction control set) load, that is, before the last transaction of the linked list has even started. Therefore the last TCS is not executed by the Linked List.

Workaround

Do not use Daisy Chain with Linked Lists (i.e. if ADICRz.SHCT[3:2] = 11_B then CHCFGRz.PRSEL = 0_B).

If the use case needs to trigger a further TCS in the next lower DMA channel then the trigger should be routed via the Interrupt Router.

DMA_TC.036 Linked List: SADR/DADR can be overwritten when loading a non-LL TCS

If a Linked List (LL) loads in a non-LL Transaction Control Set (TCS) which has a shadow mode selected (ADICRz.SHCT = 0001_B or 0010_B or 0100_B or 0101_B), during the write-back it can overwrite the contents of SADR/DADR in the newly loaded TCS before the DMA transaction has been run.

Workaround

Do not use shadow address modes with DMA Conditional Linked List.

Note: The Application Note AP32245 “DMA Linked List” will highlight that shadow address modes are not required.

DMA_TC.037 Conditional Linked List: Bit TSR.CH not cleared for a CLL transaction upon pattern match

When a Conditional Linked List (CLL) pattern match is found, the transaction ends. TSR.CH should be cleared, and set later during write-back of the Transaction Control Set (TCS) if the newly loaded TCS is auto-starting (i.e. CHCSRz.SCH = 1_B).

Due to an internal problem TSR.CH is not cleared in this case.

Workaround

There is no workaround.

The assessment is that a DMA CLL transaction that does not get a match will transition to the next DMA transaction. The CH bit will be cleared.

DMA_TC.038 Linked List: SIT interrupt when SIT bit set in newly loaded TCS

The Set Interrupt Trigger (SIT) bit is a means of generating a DMA channel interrupt service request via software. It is a debug feature that allows to trigger the Interrupt Router, without configuring the DMA channel and executing a DMA transaction.

When a new Transaction Control Set (TCS) is loaded in linked list mode, and the SIT bit in the new TCS being loaded is set in the value written to register CHCSRz, a channel interrupt trigger will be activated.

Therefore, the SIT bit should always be set to 0_B when using linked lists.

Note: The latest versions of the documentation are/will be updated to reflect this.

DMA_TC.039 Read Data CRC

The Read Data CRC (RDCRC) calculates an IEEE 802.3 ethernet CRC32 checksum as DMA moves read data through the DMA. The DMA implementation of the algorithm does not zero extend the read data for SDTB (8-bit) and SDTH (16-bit) accesses resulting in the calculation of a wrong checksum value

The RDCRC must only be used with STDW (32-bit), SDTD (64-bit), BTR2 (128-bit) and BTR4 (256-bit) access sizes. It must be noted that SDTD, BTR2 and BTR4 are only supported for SRI-source to SRI-destination transactions.

DMA_TC.040 DMA Linked Lists: Intermittent Clearing of Hardware Transaction Request Enable with mixed mode Transaction Control Sets

When a DMA channel is configured for linked list operation, if a Transaction Control Set (TCS) is configured for Continuous Mode (DMA_CHCFGRz.CHMODE = 1_B) and the next TCS is configured for Single Mode (DMA_CHCFGRz.CHMODE = 0_B) then DMA_TSRz.HTRE may be intermittently cleared disabling the servicing of DMA hardware requests.

Workaround

If a DMA channel is configured for linked list operation then all application DMA transactions must be configured for Continuous Mode (DMA_CHCFGRz.CHMODE = 1_B). If there is a need for the application to clear the Hardware Transaction Request Enable (DMA_TSRz.HTRE = 0_B) then two additional dummy DMA transactions should be serviced by the DMA in the linked list:

- Dummy Transaction 1:
  the TCS is configured as a linked list TCS (DMA_ADICRz.SHCT = 0xC, 0xD or 0xE) in Single Mode (DMA_CHCFGRz.CHMODE = 0) and auto start (DMA_CHCSRz.SCH = 1_B). The TCS should configure a single DMA move to read a word from memory in order to write DMA_TSRz.DCH = 1_B and disable subsequent DMA hardware requests.
- Dummy Transaction 2:
  the TCS is configured for normal shadow control mode

(DMA_ADICRz.SHCT = 0000_B) and Single Mode. A dummy DMA move is performed.

DMA_TC.041 DMA Circular Buffer Wrap Interrupt

If a DMA channel is configured for source circular buffer operation (ADICRz.SCBE = 1_B), the DMA shall correctly calculate the DMA source addresses. When the DMA source address wraps, the DMA is unreliable in updating the wrap source buffer status (CHCSRz.WRPS). If the wrap source buffer interrupt is enabled (ADICRz.WRPSE = 1_B), the DMA is unreliable in triggering a source wrap buffer interrupt.

If a DMA channel is configured for destination circular buffer operation (ADICRz.DCBE = 1_B), the DMA shall correctly calculate the DMA destination addresses. When the DMA destination address wraps, the DMA is unreliable in updating the wrap destination buffer status (CHCSRz.WRPD). If the wrap destination buffer interrupt is enabled (ADICRz.WRPDE = 1_B), the DMA is unreliable in triggering a destination wrap buffer interrupt.

Workaround

The source wrap buffer interrupt shall be disabled (ADICRz.WRPSE =0_B).

The destination wrap buffer interrupt shall be disabled (ADICRz.WRPDE =0_B).

If a DMA channel is configured for circular buffer operation (ADICRz.SCBE = 1_B or ADICRz.DCBE = 1_B), the DMA channel shall be configured as follows:

- The size of the DMA transaction shall equal the size of the circular buffer.
- If a source circular buffer is configured (ADICRz.SCBE = 1_B), the initial DMA source address shall be the start address of the source circular buffer.
- If a destination circular buffer is configured (ADICRz.DCBE = 1_B), the initial DMA destination address shall be the start address of the destination circular buffer.
- The DMA channel interrupt control shall be configured to trigger an interrupt on completion of the DMA transaction (DMA_ADICRz.INTCT = 10_B and DMA_ADICRz.IRDV = 0000_B).

If a DMA channel is configured for both source circular buffer operation (ADICRz.SCBE = 1_B) AND destination circular buffer operation

(ADICRz.DCBE = 1_B), the size of the source circular buffer shall equal the size of the destination circular buffer.

DMA_TC.042 DMA Interrupt from Channel reported before Completion of DMA Transaction

The Interrupt from Channel (ICH) status bit should be set on completion of a DMA transaction. If the DMA channel is configured to append a DMA Timestamp then validation have discovered that the ICH bit is set before the DMA timestamp has been written.

Workaround 1

On receipt of a DMA channel interrupt service request software shall poll the Move Engine (ME) Status Register(s) to confirm the DMA channel is no longer active.

1. Check active DMA channel in ME SR.
2. Check Write Status in ME SR.

If these fields in both ME are no longer the DMA channel that triggered the DMA channel interrupt service request then the DMA transaction has completed.

Workaround 2

To avoid polling the Move Engine status, the user may use a DMA linked list to execute the following DMA transactions:

- DMA transaction 1:
  - move operation (DMA timestamp shall not be selected)
- DMA transaction 2:
  - single 32-bit DMA move to copy DMA timestamp from DMA TIME register to next 32-bit aligned destination after DMA transaction 1.

DMA_TC.043 DMA Write Move Data Corruption for non 32-byte Aligned Cacheable Source Address

If the DMA channel TCS selects a 256-bit channel data width and a non 32-byte aligned source address then the beat order of the DMA write move will be

different for DMA read moves to cacheable (segments 8 and 9) and non-cacheable (segments A and B) source addresses. The effect is data corruption for accesses to cacheable addresses.

Workarounds

1. Use 32-byte aligned source addresses for DMA read move to cacheable addresses (segments 8 and 9).
2. Use non-cacheable source addresses (segments A and B).

DMA_TC.044 Clock Switch after SPB Error Reported results in Spurious SRI Error

If an SPB error is reported, and then immediately the SRI:SPB clock ratio is changed, then if the next DMA read move is to an SRI source address a spurious error may be reported.

Workaround

1. The system shall not change the SRI:SPB clock ratio while the DMA is active.
2. The DMA error handler should monitor the reporting of SPB and SRI errors after a clock switch.

DMA_TC.045 DMA Reconfigures DMA Channels Lockup

If two or more DMA channels are used to re-configure other DMA channels (i.e. perform a DMA write move to DMA address space) the DMA may lock up if the re-configuration DMA channels are assigned to different DMA hardware resource partitions.

The effect of the DMA lock up is to lock up other SPB master interfaces which attempt a write access to DMA address space.

Workaround

All DMA channels used to re-configure other DMA channels shall be assigned to the same hardware resource partition in their corresponding DMA Channel Hardware Resource Registers HRRz.

DMA_TC.046 Shadow Operation Read Only Mode

If a DMA channel is configured for Source Address Buffering Read Only (ADICR.SHCT = 0001_B) or Destination Address Buffering Read Only (ADICR.SHCT = 0010_B), the DMA is unreliable when performing a shadow address update. In these modes, the SADR/DADR registers may get directly updated (instead of SHADR) in the middle of a transaction, potentially resulting in a DMA data transfer corruption.

Workaround

The DMA channel configuration for Read Only Modes (SHCT = 0001_B or SHCT = 0010_B) must not be used.

Instead, to update the SADR/DADR in the middle of a transaction, use the corresponding Direct Write Mode for Source Address Buffering (ADICR.SHCT = 0101_B) or Destination Address Buffering (ADICR.SHCT = 0110_B), and write the new address to the SHADR register.

DMA_TC.049 Bus Error Reported During LL TCS Load

If a DMA channel is configured for Linked List (LL) operation AND a bus error is reported during the load of a new Transaction Control Set (TCS), the DMA shall set the DMA_ERRSRx.DLLER status bit (Move Engine x DMA Linked List Error).

Erroneously, the DMA additionally sets the DMA_ERRSRx.SER status bit (Move Engine x Source Error).

Workaround

None.

DMA_TC.050 Clearing CHCSR.FROZEN during Double Buffering

If a DMA channel is configured for one of the following Double Buffering operations:

- 1001_B Double Source Buffering Automatic Hardware and Software Switch
- 1011_B Double Destination Buffering Automatic Hardware and Software Switch

AND the active buffer fills/empties before software has cleared the DMA channel CHCSRz.FROZEN bit, the DMA shall overflow/underflow the active buffer.

Erroneously, the DMA will not trigger a Transaction Request Lost (TRL) error.

Workaround

Software shall clear DMA channel CHCSRz.FROZEN before the active buffer overflows/underflows.

DMA_TC.052 SER and DER During Linked List Operations

Software may configure a DMA channel for one of the DMA linked list operations:

- DMA linked list
  - (DMA channel DMA_ADICRz.SHCT = 1100_B),
- Accumulated linked list
  - (DMA channel DMA_ADICRz.SHCT = 1101_B),
- Safe linked list
  - (DMA channel DMA_ADICRz.SHCT = 1110_B),
- Conditional linked list
  - (DMA channel DMA_ADICRz.SHCT = 1111_B).

If the DMA is servicing a DMA request for a DMA channel configured for one of the linked list operations and the DMA indicates a Source Error (SER) (i.e. DMA_ERRSRx.SER = 1_B) or a Destination Error (DER) (i.e. DMA_ERRSRx.DER = 1_B), the DMA completes the current DMA transaction. If the DMA channel is configured for conditional linked list, the DMA disables pattern matching for each DMA read move reporting a SER. When the DMA

completes the current DMA transaction, the DMA stops servicing the linked list operation and the DMA will not load the next transaction control set to allow debug of the current DMA transaction.

Erroneously, upon a SER or DER, the DMA does not reliably stop the linked list operation (when it should) on completion of the current DMA transaction.

If the Move Engine is configured to enable DMA error interrupt service request for SER (DMA_EERx.ESER =1_B) and for DER (DMA_EERx.EDER = 1_B), the DMA triggers a DMA error interrupt service request.

The application software should include a DMA error handler to resolve all DMA errors including SER and DER.

Workaround

None.

DMA_TC.053 TS16_ERR Type of Error Reporting Unreliable

During debugging, the error trigger set (TS16_ERR) may be used to identify the type of DMA error and the number of the DMA channel. After TS16_ERR reports an error the error type bits (ME0SE, ME0DE, ME1SE and ME1DE) are not cleared. If TS16_ERR reports a subsequent error, the type of error reporting is unreliable.

Workaround

After TS16_ERR reports an error, the error type bits must be cleared.

DMA_TC.054 DMA Channel Halt Acknowledge Unreliable

Software may halt a DMA channel by writing to the halt request bit (TSRz.HLTREQ = 1_B). When a DMA channel enters the halt state, the DMA reports DMA channel halt acknowledge (TSRz.HLTACK = 1_B).

The reporting of DMA channel halt acknowledge is unreliable when software sets the TSRz.HLTREQ bit just as channel z is about to be scheduled to a move

engine. In this case, the DMA may report a DMA channel is halted when the DMA channel is active in a move engine.

Workaround

If the DMA reports a DMA channel is halted, the software should check the DMA channel is not active in a move engine by monitoring the active channel in the move engine status register(s).

DMA_TC.055 ICU to DMA Interface in Sleep Mode

The Interrupt Router triggers DMA hardware requests via the ICU interface. If the DMA is in sleep mode, the DMA will not acknowledge DMA hardware requests. The effect is to lock up the ICU to DMA interface.

Workaround

The application must disable the triggering of DMA hardware requests before placing the DMA in sleep mode.

DMA_TC.056 TSR and SUSENR Access Protection Unreliable

The DMA access protection is part of a system wide access protection scheme to restrict write accesses to DMA registers to individual on-chip bus masters.

If the application software configures DMA freedom from interference measures (i.e. when any on-chip bus master write to the DMA is prohibited by a DMA access enable setting), then on-chip bus master writes to the DMA channel TSR and SUSENR registers are unreliable and may result in the following effects:

1. Safety Related Effects

- 1.1. An illegal write access to a DMA channel TSR register will succeed with no indication.

The safety related effects (in point 1.1) relate to the DMA channel reset, halt and hardware request control functions in the TSR register. The most severe safety effect is that a DMA operation may be lost.

Workaround (for 1.1):

If the application software implements temporal monitoring of DMA transactions (e.g. using DMA timestamp) to detect lost DMA operations, the application software will detect the effect of the illegal access to DMA channel TSR register.

2. Non Safety Related Effects

- 2.1. An illegal write access to a DMA channel SUSENR register may succeed with no indication.
  - Impact of 2.1: The SUSENR register is a debug only register. No impact is foreseen during a normal application.
- 2.2. A legal write access to a DMA channel TSR register may fail with an indication - this means unexpected bus errors may be triggered when accessing TSR registers.
- 2.3. A legal write access to a DMA channel SUSENR register may fail with an indication - this means unexpected bus errors may be triggered when accessing SUSENR registers.
  - Impact of 2.2 & 2.3: Unexpected SPB bus errors and hence CPU traps and SPB error alarms may occur during application run.

Workaround (for 2.2 & 2.3):

If the system implements DMA freedom from interference measures, then the Impact of 2.2 & 2.3 will occur, and cause unexpected SPB bus errors and hence CPU traps and SPB error alarms when writing to TSR and SUSENR registers.

In order to work around this problem, the application software shall implement all of the following steps:

- W1: Before an intended write access to a DMA channel TSR or SUSENR register, perform an additional preceding write access to a DMA channel Transaction Control Set (TCS) register of the same DMA channel.
  - TCS registers include the DMA channel RDCRC, SDCRC, SADR, DADR, SHADR, ADICR, CHCSR and CHCFGR registers.

- W2: Ensure that this additional preceding write access to a DMA channel TCS register has no real effect. Recommendation: Simply read and write back the RDCRCR register.
- W3: Perform the write access to the DMA channel TSR register.

Ensure that no other on-chip bus master can access any DMA register of a different resource partition between steps W2 and W3 in the workaround above.

Example Code Snippet:

To update TSR register of DMA channel 25 with value:

```
1. Uint32 temp = DMA_RDCRCR25.U;
2. DMA_ RDCRCR25.U = temp;
3. DMA_TSR25.U = value;
```

DMA_TC.058 Linked List Load Transaction Control Set (TCS) Integrity Error

If DMA channel z is configured for one of the following linked list operations:

- DMA Linked List
  - (DMA channel ADICRz.SHCT = 1100_B)
- Accumulated Linked List
  - (DMA channel ADICRz.SHCT = 1101_B)
- Safe Linked List
  - (DMA channel ADICRz.SHCT = 1110_B)
- Conditional Linked List
  - (DMA channel ADICRz.SHCT = 1111_B)

Then on completion of a DMA transaction a new TCS is loaded into DMA channel z from the on-chip bus.

The DMA ignores data integrity errors in the new TCS:

- The DMA does not trigger an alarm to the SMU.
- The DMA does not store any DMA error status.
- The DMA may execute a corrupted DMA transaction.

Detection of most corrupted DMA transactions is provided by the DMA safety mechanisms as follows:

- Use of the DMA address checksum to detect address generation faults.
- Use of the DMA timestamp[1] to detect temporal faults.

Workaround

None.

DMA_TC.061 DMA Double Buffering Operations

Note: This erratum DMA_TC.061 (DMA Double Buffering Operations) substitutes the following errata text modules
- DMA_TC.029 (DMA Double Buffering Overflow),
- DMA_TC.047 (DMA Double Buffering Buffer Switch), and
- DMA_TC.057 (Double Buffering Overflow Causes Other Channel Corruption)
included in previous TC2xx errata sheet releases.

Software may configure a DMA channel for one of the DMA double buffering operations:

- DMA Double Source Buffering Software Switch Only
  – (DMA channel DMA_ADICRz.SHCT = 1000_B),
- DMA Double Source Buffering Automatic Hardware and Software Switch
  – (DMA channel DMA_ADICRz.SHCT = 1001_B),
- DMA Double Destination Buffering Software Switch Only
  – (DMA channel DMA_ADICRz.SHCT = 1010_B),
- DMA Double Destination Buffering Automatic Hardware and Software Switch
  – (DMA channel DMA_ADICRz.SHCT = 1011_B).

If the DMA is servicing a DMA request for a DMA channel configured for one of the double buffering operations AND the software executes a Software Buffer Switch operation (DMA_CHCSRz.SWB = 1_B), the DMA will not perform the buffer switch reliably.

1) Conditional Linked List does not support the appendage of timestamps (ADICRz.STAMP = 0_B).

The following sections provide recommendations for the implementation of DMA double buffering operations.

Supported DMA double buffering operations:

As a consequence, the software should configure for a limited number of DMA double buffering operations:

- DMA Double Source Buffering Automatic Hardware Switch
  – (DMA channel DMA_ADICRz.SHCT = 1001_B),
- DMA Double Destination Buffering Automatic Hardware Switch
  – (DMA channel DMA_ADICRz.SHCT = 1011_B).

The software must

- NOT perform a Software Buffer Switch (DMA_CHCSRz.SWB = 0_B),
- NOT set the frozen bit (DMA_CHCSRz.FROZEN = 1_B).

DMA channel ETRL configuration:

The software must set the Enable Transaction Request Lost (ETRL) bit (DMA_ADICRz.ETRL = 1_B) to prevent the DMA locking up during a DMA double buffering operation.

DMA channel monitoring:

The software should configure the DMA to trigger a DMA channel interrupt service request when the DMA empties (source buffering) or fills (destination buffering) a buffer on the completion of a DMA transaction. The software must service the DMA channel interrupt service requests. As soon as the software has analysed a buffer, the software must clear the frozen bit (DMA_CHCSRz.FROZEN = 0_B) and re-initialise the buffer address pointer.

DMA channel underflow or overflow:

If the software fails to analyse a frozen buffer before the next DMA channel interrupt service request, the DMA channel will underflow (source buffering) or overflow (destination buffering) on receiving the next DMA request. Erroneously, the DMA will not trigger a DMA error interrupt service request.

As soon as the CPU receives a DMA channel interrupt service request, the software must check for an underflow or overflow by monitoring the DMA

transaction count. If the software reads a zero transaction count (DMA_CHCSRz.TCOUNT = 0_D), the DMA channel is in an underflow or overflow state.

DMA channel interference:

Erroneously a DMA channel underflow or overflow may cause the setting of the TRL flag and the clearing of a DMA request in one or more other DMA channels (note: dependent on the scheduling of DMA channels around this DMA request). The DMA channel interference is independent of resource partition assignment.

DMA channel reset:

If the software detects a DMA channel underflow or overflow, the software must apply a DMA channel reset to all used DMA channels. On completion of the DMA channel reset, the software must re-configure all used DMA channels.

Alternatively, the software may apply an application reset.

Workaround

None.

DMA_TC.062 Termination of DMA Transaction for Pattern Match

If a DMA channel is configured for pattern detection and the DMA detects a pattern match, the DMA should terminate the DMA transaction. The DMA should provide the software with the capability to use the DMA channel status to identify the transfer number of the DMA move data.

Erroneously, the DMA may decrement 1 from the TCOUNT value making identification of the DMA move data unreliable.

Workaround

None.

DMA_TC.063 DMA Timestamp Destination Address

If software configures a DMA channel

- for increment of DMA destination address (DMA_ADICRz.INCD = 1_B) AND
- to append a DMA timestamp (DMA_ADICRz.STAMP = 1_B);

and the intended write address of the DMA timestamp is in a different 32 Kbyte page to the last DMA destination address to write DMA move data, the DMA erroneously calculates the DMA timestamp write address. The DMA writes the DMA timestamp to an incorrect address inside the same 32 Kbyte page as the last DMA destination address.

Workaround

The last DMA destination address and the write address of the DMA timestamp shall exist in the same 32 Kbyte page (i.e. and shall not cross the 32 Kbyte page boundary).

DMA_TC.064 DMA Daisy Chain Request

If software configures a DMA channel for one of the following DMA operations:

- DMA Pattern Detection
  – (DMA channel DMA_CHCFGRz.PATSEL[1:0] != 00_B),
- DMA Double Source Buffering Software Switch Only
  – (DMA channel DMA_ADICRz.SHCT = 1000_B),
- DMA Double Source Buffering Automatic Hardware and Software Switch
  – (DMA channel DMA_ADICRz.SHCT = 1001_B),
- DMA Double Destination Buffering Software Switch Only
  – (DMA channel DMA_ADICRz.SHCT = 1010_B),
- DMA Double Destination Buffering Automatic Hardware and Software Switch
  – (DMA channel DMA_ADICRz.SHCT = 1011_B),
- DMA linked list
  – (DMA channel DMA_ADICRz.SHCT = 1100_B),
- Accumulated linked list
  – (DMA channel DMA_ADICRz.SHCT = 1101_B),
- Safe linked list

  - (DMA channel DMA_ADICRz.SHCT = 1110_B),
- Conditional linked list
  - (DMA channel ADICRz.SHCT = 1111_B),

the software must not select daisy chain (DMA channel CHCFGRz.PRSEL = 0_B).

DMA_TC.065 DMA Move Concurrent Bus Accesses

The highest number DMA channel always wins arbitration to shared DMA resources (Move Engine and DMA on-chip bus master interfaces). The configuration of the DMA priority (DMA_CHCFGRx.DMAPRIO) has no effect on internal DMA arbitration.

The DMA priority is used by the System Peripheral Bus (SPB) controller to arbitrate between requests from all the SPB master interfaces.

Workaround

None.

DTS_TC.001 Temperature Sensor Formula

The formula documented in older Data Sheet versions may result in an increased temperature error when calculating the junction temperature Tj of the device from a DTS temperature measurement.

To properly calculate the temperature measured by the DTS in [°C] from the RESULT bit field of register SCU_DTSSTAT, it is recommended to use the following formulas depending on the contents of bit field SCU_DTSCON[30:29]:

- While bit field SCU_DTSCON[30:29] = 00_B: Tj = (RESULT - 607_D) / 2.13
- While bit field SCU_DTSCON[30:29] = 01_B: Tj = (RESULT - 646_D) / 2.11

Bit field SCU_DTSCON[30:29] can only deliver one of the two values (00_B, 01_B) listed above (constant for a given device).

Make sure the application software does not modify the values installed during device start-up in register SCU_DTSCON.

Note: The description in the Data Sheet will be updated appropriately.

FlexRay_AI.087 After reception of a valid sync frame followed by a valid non-sync frame in the same static slot the received sync frame may be ignored

Description:

If in a static slot of an even cycle a valid sync frame followed by a valid non-sync frame is received, and the frame valid detection (prt_frame_decoded_on_X) of the DEC process occurs one sclk after valid frame detection of FSP process (fsp_val_syncfr_chx), the sync frame is not taken into account by the CSP process (devte_xxs_reg).

Scope:

The erratum is limited to the case where more than one valid frame is received in a static slot of an even cycle.

Effects:

In the described case the sync frame is not considered by the CSP process. This may lead to a SyncCalcResult of MISSIMG_TERM (error flag SFS.MRCS set). As a result the POC state may switch to NORMAL_PASSIVE or HALT or the Startup procedure is aborted.

Workaround

Avoid static slot configurations long enough to receive two valid frames.

FlexRay_AI.088 A sequence of received WUS may generate redundant `SIR.WUPA/B` events

Description:

If a sequence of wakeup symbols (WUS) is received, all separated by appropriate idle phases, a valid wakeup pattern (WUP) should be detected after every second WUS.The E-Ray detects a valid wakeup pattern after the second WUS and then after each following WUS.

Scope:

The erratum is limited to the case where the application program frequently resets the appropriate SIR.WUPA/B bits.

Effects:

In the described case there are more SIR.WUPA/B events seen than expected.

Workaround

Ignore redundant SIR.WUPA/B events.

FlexRay_AI.089 Rate correction set to zero in case of SyncCalcResult=MISSING_TERM

Description:

In case a node receives too few sync frames for rate correction calculation and signals a SyncCalcResult of MISSING_TERM, the rate correction value is set to zero instead to the last calculated value.

Scope:

The erratum is limited to the case of receiving too few sync frames for rate correction calculation (SyncCalcResult=MISSING_TERM in an odd cycle).

Effects:

In the described case a rate correction value of zero is applied in NORMAL_ACTIVE / NORMAL_PASSIVE state instead of the last rate correction value calculated in NORMAL_ACTIVE state. This may lead to a desynchronisation of the node although it may stay in NORMAL_ACTIVE state (depending on gMaxWithoutClockCorrectionPassive) and decreases the probability to re-enter NORMAL_ACTIVE state if it has switched to NORMAL_PASSIVE (pAllowHaltDueToclock=false).

Workaround

It is recommended to set gMaxWithoutClockCorrectionPassive to 1. If missing sync frames cause the node to enter NORMAL_PASSIVE state, use higher level application software to leave this state and to initiate a re-integration into the cluster. HALT state can also be used instead of NORMAL_PASSIVE state by setting pAllowHaltDueToClock to true.

FlexRay_AI.090 Flag `SFS.MRCS` is set erroneously although at least one valid sync frame pair is received

Description:

If in an odd cycle 2c+1 after reception of a sync frame in slot n the total number of different sync frames per double cycle has exceeded gSyncNodeMax and the node receives in slot n+1 a sync frame that matches with a sync frame received in the even cycle 2c, the sync frame pair is not taken into account by CSP process. This may cause the flags `SFS.MRCS` and `EIR.CCF` to be set erroneously.

Scope:

The erratum is limited to the case of a faulty cluster configuration where different sets of sync frames are transmitted in even and odd cycles and the total number of different sync frames is greater than gSyncNodeMax.

Effects:

In the described case the error interrupt flag `EIR.CCF` is set and the node may enter either the POC state NORMAL_PASSIVE or HALT.

Workaround

Correct configuration of gSyncNodeMax.

FlexRay_AI.091 Incorrect rate and/or offset correction value if second Secondary Time Reference Point (STRP) coincides with the action point after detection of a valid frame

Description:

If a valid sync frame is received before the action point and additionally noise or a second frame leads to a STRP coinciding with the action point, an incorrect deviation value of zero is used for further calculations of rate and/or offset correction values.

Scope:

The erratum is limited to configurations with an action point offset greater than static frame length.

Effects:

In the described case a deviation value of zero is used for further calculations of rate and/or offset correction values. This may lead to an incorrect rate and/or offset correction of the node.

Workaround

Configure action point offset smaller than static frame length.

FlexRay_AI.092 Initial rate correction value of an integrating node is zero if pMicroInitialOffsetA,B = 0x00

Description:

The initial rate correction value as calculated in figure 8-8 of protocol spec v2.1 is zero if parameter pMicroInitialOffsetA,B was configured to be zero.

Scope:

The erratum is limited to the case where pMicroInitialOffsetA,B is configured to zero.

Effects:

Starting with an initial rate correction value of zero leads to an adjustment of the rate correction earliest 3 cycles later (see figure 7-10 of protocol spec v2.1). In a worst case scenario, if the whole cluster is drifting away too fast, the integrating node would not be able to follow and therefore abort integration.

Workaround

Avoid configurations with pMicroInitialOffsetA,B equal to zero. If the related configuration constraint of the protocol specification results in pMicroInitialOffsetA,B equal to zero, configure it to one instead. This will lead to a correct initial rate correction value, it will delay the startup of the node by only one microtick.

FlexRay_AI.093 Acceptance of startup frames received after reception of more than gSyncNodeMax sync frames

Description:

If a node receives in an even cycle a startup frame after it has received more than gSyncNodeMax sync frames, this startup frame is added erroneously by process CSP to the number of valid startup frames (zStartupNodes). The faulty number of startup frames is delivered to the process POC. As a consequence this node may integrate erroneously to the running cluster because it assumes that it has received the required number of startup frames.

Scope:

The erratum is limited to the case of more than gSyncNodeMax sync frames.

Effects:

In the described case a node may erroneously integrate successfully into a running cluster.

Workaround

Use frame schedules where all startup frames are placed in the first static slots. gSyncNodeMax should be configured to be greater than or equal to the number of sync frames in the cluster.

FlexRay_AI.094 Sync frame overflow flag `EIR.SFO` may be set if slot counter is greater than 1024

Description:

If in the static segment the number of transmitted and received sync frames reaches gSyncNodeMax and the slot counter in the dynamic segment reaches the value cStaticSlotIDMax + gSyncNodeMax = 1023 + gSyncNodeMax, the sync frame overflow flag `EIR.SFO` is set erroneously.

Scope:

The erratum is limited to configurations where the number of transmitted and received sync frames equals to gSyncNodeMax and the number of static slots plus the number of dynamic slots is greater or equal than 1023 + gSyncNodeMax.

Effects:

In the described case the sync frame overflow flag `EIR.SFO` is set erroneously. This has no effect to the POC state.

Workaround

Configure gSyncNodeMax to number of transmitted and received sync frames plus one or avoid configurations where the total of static and dynamic slots is greater than cStaticSlotIDMax.

FlexRay_AI.095 Register RCV displays wrong value

Description:

If the calculated rate correction value is in the range of [-pClusterDriftDamping .. +pClusterDriftDamping], vRateCorrection of the CSP process is set to zero. In this case register RCV should be updated with this value. Erroneously RCV.RCV[11:0] holds the calculated value in the range [-pClusterDriftDamping .. +pClusterDriftDamping] instead of zero.

Scope:

The erratum is limited to the case where the calculated rate correction value is in the range of [-pClusterDriftDamping .. +pClusterDriftDamping].

Effects:

The displayed rate correction value RCV.RCV[11:0] is in the range of [-pClusterDriftDamping .. +pClusterDriftDamping] instead of zero. The error of the displayed value is limited to the range of [-pClusterDriftDamping .. +pClusterDriftDamping]. For rate correction in the next double cycle always the correct value of zero is used.

Workaround

A value of RCV.RCV[11:0] in the range of [-pClusterDriftDamping .. +pClusterDriftDamping] has to be interpreted as zero.

FlexRay_AI.096 Noise following a dynamic frame that delays idle detection may fail to stop slot

Description:

If (in case of noise) the time between ’potential idle start on X’ and ’CHIRP on X’ (see Protocol Spec. v2.1, Figure 5-21) is greater than gdDynamicSlotIdlePhase, the E-Ray will not remain for the remainder of the current dynamic segment in the state ’wait for the end of dynamic slot rx’. Instead, the E-Ray continues slot counting. This may enable the node to further transmissions in the current dynamic segment.

Scope:

The erratum is limited to noise that is seen only locally and that is detected in the time window between the end of a dynamic frame's DTS and idle detection ('CHIRP on X').

Effects:

In the described case the faulty node may not stop slot counting and may continue to transmit dynamic frames. This may lead to a frame collision in the current dynamic segment.

Workaround

None.

FlexRay_AI.097 Loop back mode operates only at 10 MBit/s

Description:

The looped back data is falsified at the two lower baud rates of 5 and 2.5 MBit/s.

Scope:

The erratum is limited to test cases where loop back is used with the baud rate prescaler (`PRTC1.BRP[1:0]`) configured to 5 or 2.5 MBit/s.

Effects:

The loop back self test is only possible at the highest baud rate.

Workaround

Run loop back tests with 10 MBit/s (`PRTC1.BRP[1:0]` = 00_B).

FlexRay_AI.099 Erroneous cycle offset during startup after abort of start-up or normal operation

Description:

An abort of startup or normal operation by a READY command near the macotick border may lead to the effect that the state INITIALIZE_SCHEDULE is one macrotick too short during the first following integration attempt. This leads to an early cycle start in state INTEGRATION_COLDSTART_CHECK or INTEGRATION_CONSISTENCY_CHECK.

As a result the integrating node calculates a cycle offset of one macrotick at the end of the first even/odd cycle pair in the states INTEGRATION_COLDSTART_CHECK or INTEGRATION_CONSISTENCY_CHECK and tries to correct this offset.

If the node is able to correct the offset of one macrotick (pOffsetCorrectionOut >> gdMacrotick), the node enters NORMAL_ACTIVE with the first startup attempt.

If the node is not able to correct the offset error because pOffsetCorrectionOut is too small (pOffsetCorrectionOut ≤ gdMacrotick), the node enters ABORT_STARTUP and is ready to try startup again. The next (second) startup attempt is not effected by this erratum.

Scope:

The erratum is limited to applications where READY command is used to leave STARTUP, NORMAL_ACTIVE, or NORMAL_PASSIVE state.

Effects:

In the described case the integrating node tries to correct an erroneous cycle offset of one macrotick during startup.

Workaround

With a configuration of pOffsetCorrectionOut >> gdMacrotick • (1+cClockDeviationMax) the node will be able to correct the offset and therefore also be able to successfully integrate.

FlexRay_AI.100 First WUS following received valid WUP may be ignored

Description:

When the protocol engine is in state WAKEUP_LISTEN and receives a valid wakeup pattern (WUP), it transfers into state READY and updates the wakeup status vector CCSV.WSV[2:0] as well as the status interrupt flags SIR.WST and SIR.WUPA/B. If the received wakeup pattern continues, the protocol engine may ignore the first wakeup symbol (WUS) following the state transition and signals the next SIR.WUPA/B at the third instead of the second WUS.

Scope:

The erratum is limited to the reception of redundant wakeup patterns.

Effects:

Delayed setting of status interrupt flags SIR.WUPA/B for redundant wakeup patterns.

Workaround

None.

FlexRay_AI.101 READY command accepted in READY state

Description:

The E-Ray module does not ignore a READY command while in READY state.

Scope:

The erratum is limited to the READY state.

Effects:

Flag CCSV.CSI is set. Cold starting needs to be enabled by POC command ALLOW_COLDSTART (SUCC1.CMD = 1001_B).

Workaround

None.

FlexRay_AI.102 Slot Status vPOC!SlotMode is reset immediately when entering HALT state

Description:

When the protocol engine is in the states NORMAL_ACTIVE or NORMAL_PASSIVE, a HALT or FREEZE command issued by the Host resets vPOC!SlotMode immediately to SINGLE slot mode (CCSV.SLM[1:0] = 00_B). According to the FlexRay protocol specification, the slot mode should not be reset to SINGLE slot mode before the following state transition from HALT to DEFAULT_CONFIG state.

Scope:

The erratum is limited to the HALT state.

Effects:

The slot status vPOC!SlotMode is reset to SINGLE when entering HALT state.

Workaround

None.

FlexRay_AI.103 Received messages not stored in Message RAM when in Loop Back Mode

After a FREEZE or HALT command has been asserted in NORMAL_ACTIVE state, and if state LOOP_BACK is then entered by transition from HALT state via DEF_CONFIG and CONFIG, it may happen that acceptance filtering for received messages is not started, and therefore these messages are not stored in the respective receive buffer in the Message RAM.

Scope:

The erratum is limited to the case where Loop Back Mode is entered after NORMAL_ACTIVE state was left by FREEZE or HALT command.

Effects:

Received messages are not stored in Message RAM because acceptance filtering is not started.

Workaround

Leave HALT state by hardware reset.

FlexRay_AI.104 Missing startup frame in cycle 0 at coldstart after FREEZE or READY command

When the E-Ray is restarted as leading coldstarter after it has been stopped by FREEZE or READY command, it may happen, depending on the internal state of the module, that the E-Ray does not transmit its startup frame in cycle 0. Only E-Ray configurations with startup frames configured for slots 1 to 7 are affected by this behaviour.

Scope:

The erratum is limited to the case when a coldstart is initialized after the E-Ray has been stopped by FREEZE or READY command. Coldstart after hardware reset is not affected.

Effects:

During coldstart it may happen that no startup frame is sent in cycle 0 after entering COLDSTART_COLLISION_RESOLUTION state from COLDSTART_LISTEN state.

Severity:

Low, as the next coldstart attempt is no longer affected. Coldstart sequence is lengthened but coldstart of FlexRay system is not prohibited by this behaviour.

Workaround

Use a static slot greater or equal 8 for the startup / sync message.

FlexRay_AI.105 RAM select signals of IBF1/IBF2 and OBF1/OBF2 in RAM test mode

When accessing Input Buffer RAM 1,2 (IBF1,2) or Output Buffer RAM 1,2 (OBF1,2) in RAM test mode, the following behaviour can be observed when entering RAM test mode after hardware reset.

- Read or write access to IBF2:
  - In this case also IBF1 RAM select **eray_ibf1_cen** is activated initiating a read access of the addressed IBF1 RAM word. The data read from IBF1 is evaluated by the respective parity checker.
- Read or write access to OBF1:
  - In this case also OBF2 RAM select **eray_obf2_cen** is activated initiating a read access of the addressed OBF2 RAM word. The data read from OBF2 is evaluated by the respective parity checker.

If the parity logic of the erroneously selected IBF1 resp. OBF2 detects a parity error, bit **MHDS.PIBF** resp. **MHDS.POBF** in the E-Ray Message Handler Status register is set although the addressed IBF2 resp. OBF1 had not error. The logic for setting **MHDS.PIBF** / **MHDS.POBF** does not distinguish between set conditions from IBF1 or IBF2 resp. OBF1 or OBF2.

Due to the IBF / OBF swap mechanism as described in section 5.11.2 in the E-Ray Specification, the inverted behaviour with respect to IBF1,2 and OBF1,2 can be observed depending on the IBF / OBF access history.

Scope:

The erratum is limited to the case when IBF1,2 or OBF1,2 are accessed in RAM test mode. The problem does not occur when the E-Ray is in normal operation mode.

Effects:

When reading or writing IBF1,2 / OBF1,2 in RAM test mode, it may happen, that the parity logic of IBF1,2 / OBF1,2 signals a parity error.

Severity:

Low, workaround available.

Workaround

For RAM testing after hardware reset, the Input / Output Buffer RAMs have to be first written and then read in the following order: IBF1 before IBF2 and OBF2 before OBF1

FlexRay_AI.106 Data transfer overrun for message transfers Message RAM to Output Buffer (OBF) or from Input Buffer (IBF) to Message RAM

The problem occurs under the following conditions:

1) A received message is transferred from the Transient Buffer RAM (TBF) to the message buffer that has its data pointer pointing to the first word of the Message RAM's Data Partition located directly after the last header word of the Header Partition of the Last Configured Buffer as defined by **MRC.LCB**.

2) The Host triggers a transfer from / to the Last Configured Buffer in the Message RAM with a specific time relation to the start of the TBF transfer described under 1).

Under these conditions the following transfers triggered by the Host may be affected:

a) Message buffer transfer from Message RAM to OBF

When the message buffer has its payload configured to maximum length (**PLC** = 127), the OBF word on address 00h (payload data bytes 0 to 3) is overwritten with unexpected data at the end of the transfer.

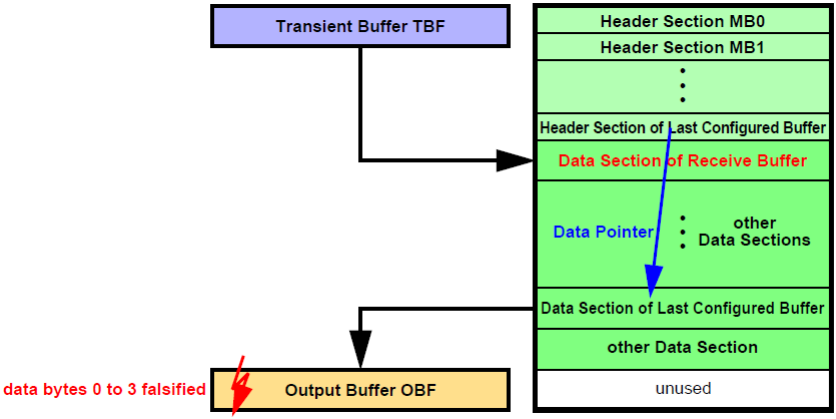

Figure 1 Message buffer transfer from Message RAM to OBF

b) Message buffer transfer from IBF to Message RAM

After the Data Section of the selected message buffer in the Message RAM has been written, one additional write access overwrites the following word in the Message RAM which might be the first word of the next Data Section.

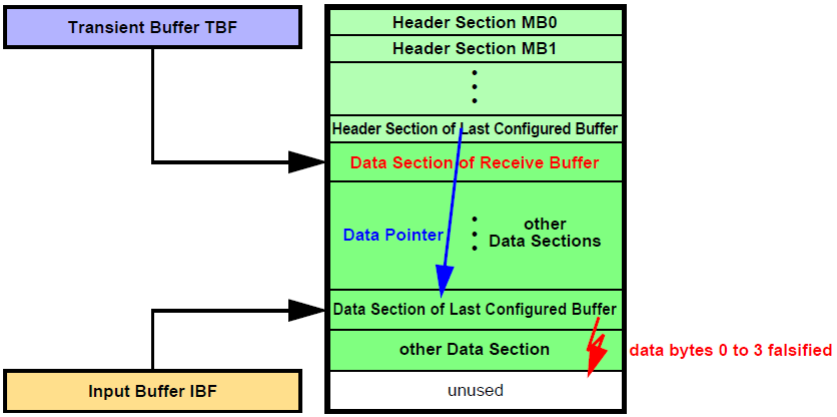

Figure 2 Message buffer transfer from IBF to Message RAM

Scope:

The erratum is limited to the case when (see **Figure 3** “Bad Case”):

1) The first Data Section in the Data Partition is assigned to a receive buffer (incl. FIFO buffers)

AND

2) The Data Partition in the Message RAM starts directly after the Header Partition (no unused Message RAM word in between)

Effects:

a) When a message is transferred from the Last Configured Buffer in the Message RAM to the OBF and **PLC** = 127 it may happen, that at the end of the transfer the OBF word on address 00h (payload data bytes 0 to 3) is overwritten with unexpected data (see **Figure 1**).

b) When a message is transferred from IBF to the Last Configured Buffer in the Message RAM, it may happen, that at the end of the transfer of the Data Section one additional write access overwrites the following word, which may be the first word of another message's Data Section in the Message RAM (see **Figure 2**).

Severity:

Medium, workaround available, check of configuration necessary.

Workaround

1) Leave at least one unused word in the Message RAM between Header Section and Data Section.

OR

2) Ensure that the Data Section directly following the Header Partition is assigned to a transmit buffer.

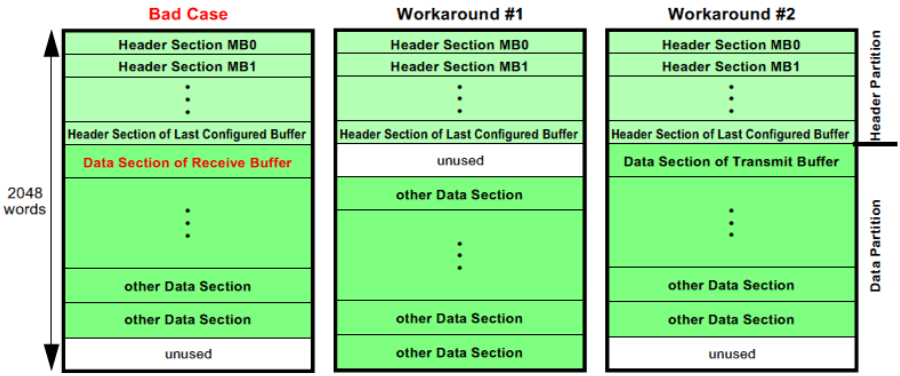

Figure 3 Message RAM Configurations

GTM_AI.132 GTM_TOP level: AEI write to BRIDGE_MODE register can result in blocking of AEI configuration interface

If the GTM bus bridge operates in MSK_WR_RESP=1 mode, a requested change of the GTM_IP bridge mode (Bit BRG_MODE) can result in blocking of the bus interface.

Scope

All AEI protocols.

Effects

GTM Bus interface does not issue aei_ready/aei_response_ready which could lead to bus timeout of the serving bus master.

Workaround

Ensure that the write command to the BRIDGE_MODE register bit BRG_MODE which switches the mode of the bridge (ASYNC/SYNC) is assigned only when in addition the bit BRG_RST is set to '1'.

GTM_AI.141 TIM: Incorrect data captured to GPR registers and routed via ARU when EGPRi_SEL,GPRi_SEL= 100 in TIM channel mode TIEM, TPWM, TIPM, TPIM, TGPS

In case of a TIM channel capture event issued by a rising edge at TIM[i]_CH[x]_FOUT the capturing of the TIM[i]_CH[x]_ECNT register to the TIM[i]_CH[x]_GPRi register is incorrect. The captured value will be ECNT_REG+2; bit 0 (signal level) will be 0. The correct operation would be to capture ECNT_REG+1; bit 1 (signal level) would be 1.

Scope

TIM.

Note: The described effects related to the ARU do not apply to devices where no ARU is implemented.

Effects

a) Inconsistency of ARU signal level bit and bit[0] of ARU word which shows the captured ECNT.

b) Reading of TIM[i]_CH[x]_GPRi shows inconsistency when comparing bits [31:24] to [7:0].At the point in time of capture event the bits [31:24] contain the correct value and are subject to be changed with new incoming edge.

Workaround

a) When using captured data via ARU routing the correct data can be reconstructed by:
IF ARU_SIGNAL_LEVEL ==1 AND ARU_DATA[0] == 0 THEN ARU_DATA = ARU_DATA -1;

b) When reading TIM[i]_CH[x]_GPRi by configuration interface the data can be corrected as long as there is no GPR overflow and no new edge by:
IF TIM[i]_CH[x]_GPRi[24] == 1 AND TIM[i]_CH[x]_GPRi[0] == 0 THEN TIM[i]_CH[x]_GPRi[23:0] = TIM[i]_CH[x]_GPRi[23:0] -1

GTM_AI.142 TIM: Incorrect data captured to GPR registers and routed via ARU when EGPRi_SEL,GPRi_SEL= 100 in TIM channel mode TBCM

In case of a TIM channel capture event issued by an input pattern match to condition TIM[i]_CH[x]_CNTS the capturing of the TIM[i]_CH[x]_ECNT register to the TIM[i]_CH[x]_GPRi register can be incorrect. Starting at t=0 with counter value ECNT_REG(t=0), the captured values of two consecutive edges can be ECNT_REG(t=0)+2 followed by ECNT_REG(t=0)+2 instead of ECNT_REG(t=0)+1 followed by ECNT_REG(t=0)+2.

Scope

TIM.

Note: The described effects related to the ARU do not apply to devices where no ARU is implemented.

Effects

a) In 2 following ARU transfers the ARU word which shows the captured ECNT do not increment by 1.

b) Reading of TIM[i]_CH[x]_GPRi shows inconsistency between [31:24] and [7:0]

Workaround

a) Ignore captured data via ARU and build with MCS independent counter which increments on each ARU transfer.

b) When reading TIM[i]_CH[x]_GPRi by configuration interface use only TIM[i]_CH[x]_GPRi[31:24] as EDGE counter; don't use TIM[i]_CH[x]_GPRi[23:0].

GTM_AI.143 GTM_TOP level: AEI pipelined write to GTM_BRIDGE_MODE register directly after setting aei_reset='0' can result in blocking of AEI configuration interface

If the GTM bus bridge is reset with aei_reset= '0' and the next AEI transfer is a write command to GTM_BRIDGE_MODE register the AEI configuration interface can be blocked.

Scope

AEI pipelined protocol.

Effects

GTM Bus interface does not issue aei_ready which could lead to bus timeout of the serving bus master.

Workaround

Ensure that after setting aei_reset to inactive state the next command must be a read to any other register except GTM_BRIDGE_MODE. Issue desired write to GTM_BRIDGE_MODE register afterwards.

GTM_AI.144 TIM: TIM interrupts as trigger source from TIM to TOM/ATOM not functional

According to specification one could select with the configuration bits EXT_CAP_SRCx(2:0) of register TIM[i]_CH[x]_ECTRL one of six TIM channel x+1 interrupts as a source for signal TIM_EXT_CAPTURE(x).

The signal is used internally in TIM channel x and forwarded to a corresponding ATOM/TOM channel.

For the signal path TIM_EXT_CAPTURE(x) which is forwarded to ATOM/TOM the selection is incorrect for the values of EXT_CAP_SRCx(2:0) = 000, 010, 100, 101, 110, 111.

Only the selection of TIM_IN(x-1), TIM_IN(x) or AUX_IN(x) is possible with the values EXT_CAP_SRCx(2:0) = 001 or 011.

For the signal path TIM_EXT_CAPTURE(x) which is used inside TIM channel x, the selection works as specified.

Scope

TIM.

Effects

The selection of an interrupt of TIM channel x+1 by EXT_CAP_SRCx(2:0) = 000, 010, 100, 101, 110, 111 to trigger corresponding TOM/ATOM channel leads to erroneous trigger behavior.

As a result the TOM/ATOM does not react on the intended interrupt.

Workaround

None.

Do not use the configuration EXT_CAP_SRCx(2:0) = 000, 010, 100, 101, 110, 111.

GTM_AI.153 TIM: Incorrect data captured to CNTS register when TIM channel operates in mode TPWM or TPIM and CNTS_SEL = 1 and selected CMU_CLK ≠ sys_clk

In case of CNTS_SEL = 1 and TIM_MODE = TPWM or TPIM in the CNTS_REG register the value of TBU_TS0 shall be captured. This does not happen when the selected CMU_CLK ≠ sys_clk.

Scope

TIM.

Effects

Unexpected values in CNTS_REG.

Workaround

Setup the TIM channel to operate on a CMU_CLK (Divider =1) which is identical to sys_clk. Please notice that the measurement with TIM_CNT has resolution of sys_clk.

GTM_AI.154 TOM: Incorrect duty cycle in PCM mode (bit reversed mode)

The generated duty cycle on the TOM output in PCM mode is always one smaller than the configured value in the CM1 register. So if the value 1 is configured, a duty cycle of 0% will be generated. Configuring the max value (0xFFFF) in the CM1 register results in a duty cycle of max-1. Expected is 100% duty cycle in this case. A zero in CM1 register results in 100% duty cycle.

Scope

TOM.

Effects

Unexpected duty cycle in PCM mode.

Workaround

Configure always the value for the expected duty cycle in the CM1 register with expected duty cycle + 1.

To get 0% duty cycle, value 1 has to be configured. To get 100% duty cycle, 0 has to be configured to CM1 register while CM0 is always configured with max. value of 0xFFFF. Configuring CM0=0x1000 and CM1=0xFFFF will also get a duty cycle of 100%.

GTM_AI.157 CMU: Incorrect AEI status by writing 1 to bit 24 of register CMU_CLK_6/7_CTRL

If according to GTM device configuration no DPLL is available, bit 24 of register CMU_CLK_6_CTRL and CMU_CLK_7_CTRL is reserved.

Erroneously, writing a '1' to bit 24 is possible and leads to AEI status 0.

Scope

CMU: GTM device configurations without DPLL.

Effects

No functional influence to specified GTM.

After writing a ‘1’ to bit 24 of register CMU_CLK_6_CTRL or CMU_CLK_7_CTRL, a ‘1’ is read back from this register bit.

Writing a ‘1’ to bit 24 of register CMU_CLK_6_CTRL or CMU_CLK_7_CTRL leads to AEI status 0.

Workaround

Do not write ‘1’ to bit 24 of register CMU_CLK_6/7_CTRL.

GTM_AI.163 TIM: timeout signaled when TDU unit is reenabled

In the following situation an undesired timeout event is signaled:

After stopping the TDU the TO_CNT bitfield will have an arbitrary value TO_CNT0 <= TOV0 bitfield. Assume TOV will be reconfigured to value TOV1 with TOV1 <= TO_CNT0. If the TDU will be enabled again by writing to TOCTRL a value !=0 and at the same time the TCS selected CMU_CLK has an active edge an unintended timeout is signaled. This results due to the fact that for one clock cycle TO_CNT0 >= TOV1.

Scope

TIM.

Effects

Unexpected timeout event when TIM TDU is enabled.

Workaround

If TDU unit has to be reenabled with a TOV value TOV1 which is less than the previous one in use TOV0 (2 alternatives are available):

a) Wait with disabling TDU until condition TOV1 > TO_CNT is fulfilled. Configure TOV with TOV1 reenable TDU Unit.

b) Disable TDU; if TOV1 <= TO_CNT write TOV with FF_H; enable TDU unit; reconfigure TOV to desired value TOV1.

GTM_AI.164 TIM: capturing of data into TIM[i]_CH[x]_CNTS with setting CNTS_SEL=1 not functional in TPWM and TPIM mode

If CNTS_SEL=1 is selected and a new input edge is signaled by the TIM Filter unit while the selected CMU_CLK has no rising edge the register TIM[i]_CH[x]_CNTS will capture data TIM[i]_CH[x]_CNT instead of TBU_TS0.

Scope

TIM.

Effects

Captured data in TIM[i]_CH[x]_CNTS is not as expected.

Workaround

a) Select with CLK_SEL a CMU_CLK which is identical to sys_clk (clock divider=1 applied in CMU channel and for global fractional divider).

b) Use TIEM mode to capture TBU_TS0 for rising and falling input edges.

c) PWM mode: Use CNTS_SEL=0 with CMU_CLK source selected as in use for TBU_TS0 counting. Capture with EGPR0_SEL=0, GPR0_SEL=0 in GPR0_REG TBU_TS0 and with EGPR1_SEL=0, GPR1_SEL= 3 in GPR1_REG CNT. Calculate the desired timestamp with GPR0_REG - GPR1_REG + CNTS_REG.

GTM_AI.181 TIM: Incorrect signal level bit ECNT[0] in mode TIEM, TPWM, TIPM, TPIM, TGPS

In case of re-enabling a previously disabled TIM channel the bit ECNT[0] might not reflect the actual signal level of the corresponding input TIM[i]_CH[x]_FOUT

until the next input edge occurs. This situation can only occur if between disabling and re-enabling the ECNT register is not read.

Scope

TIM.

Effects

Inconsistency of input signal level with ECNT bit[0].

Workaround

- After disabling the TIM channel, ensure that the ECNT register is read at least once and afterwards the TIM channel can be re-enabled.
- Before re-enabling a TIM channel, issue a TIM channel reset and reconfigure the TIM channel control registers.

GTM_AI.202 (A)TOM: no CCU1 interrupt in case of CM1=0 or 1 and RST_CCU0=1

In case of channel x has configuration of RST_CCU0=1 (i.e. CN0 is reset by trigger input) and CN0 counts from 0 to MAX:

- if CM1=0, CM0>0 -> no CCU1 interrupt is generated
- if CM1=1, CM0=MAX+1 -> only one time a CCU1 interrupt is generated

Scope

TOM / ATOM SOMP mode.

Effects

For the described configuration no CCU1 interrupt is generated.

Workaround

Use for triggering channel y (i.e. the channel that triggers on channel x the reset of counter CN0) the configuration of CM0=MAX, CM1=1.

In case of duty cycle configuration of CM1=0 and CM0>0 on channel x use instead of CCU1 interrupt on channel x the CCU0 interrupt of triggering channel y.

In case of duty cycle configuration of CM1=1 and CM0=MAX+1 on channel x use instead of CCU1 interrupt on channel x the CCU1 interrupt of triggering channel y.

GTM_AI.205 TIM: unexpected CNTS register update in TPWM OSM mode

If OSM=1 and TIM_MODE="000" (TPWM) an active edge defined by DSL will stop the measurement. In case of an inactive edge following after 1 GTM system clock cycle the active edge the CNTS register will be reset unexpected.

Scope

TIM.

Effects

Unexpected CNTS register content.

Workaround

a) Use CMU clock in TIM channel with frequency lesser than system clock.

b) Enable filter and configure filter parameter in a way that two consecutive edges will never occur with distance of GTM system clock.

GTM_AI.209 TOM/ATOM: no update of CM0/CM1/CLK_SRC via trigger signal from preceding instance if selected CMU_CLKx is not SYS_CLK

The trigger signal between (A)TOM instances (e.g. signal TOM_TRIG_[i]) is registered between each TOM and between each 2nd ATOM and with this delayed by one SYS_CLK period to break long combinational path.

For each register in the trigger path between (A)TOM instance i and the succeeding (A)TOM instance i+1, this trigger from instance i does not trigger the update of register CM0, CM1 and CLK_SRC with content of SR0, SR1 and

CLK_SRC_SR if the triggered channel of instance i+1 is not running with a selected CMU_CLKx = SYS_CLK.

Scope

TOM/ATOM.

Effects

In the described configuration no update of CM0, CM1 and CLK_SRC is done although the update is enabled by register TOM[i]_TGC[y]_GLB_CTRL / ATOM[i]_AGC_GLB_CTRL.

Workaround

For each register in trigger path between (A)TOM instance i and (A)TOM instance i+1, the channel of instance i+1 that should be triggered has to use a clock of period identical to SYS_CLK period.

A second workaround could be to set up on instance i+1 a redundant channel to trigger other channel of instance i+1 like it was set up on instance i to trigger other channel. Then, start both instances synchronously by using the TBU time base comparator of AGC/TGCx unit (i.e. the ATOM[i]_AGC_ATC_TB / TOM[i]_TGC[y]_ACT_TB register).

GTM_AI.270 (A)TOM: output signal is postponed one period for the values CM0=1 and CM1>CM0 if CN0 is reset by the trigger of a preceding channel (RST_CCU0=1)

If counter CN0 is reset by the trigger of a preceding channel (bit RST_CCU0 of register TOM[i]_CH[x]_CTRL/ATOM[i]_CH[x]_CTRL is set), then the value of CM0 defines the signal edge to SL (signal level), whereas CM1 defines the edge to !SL (inverted signal level).

If - in this case - the value 1 is configured for the output edge to SL (CM0=1) and CM1 is configured to greater than CM0 (CM1>CM0) the expected output edge will be postponed by one period.

Scope

TOM, ATOM SOMP mode

Effects

The expected output edge will be postponed by one period.

Workaround

Instead of configuring CM0=1 it is also possible to configure CM1=1 and to invert SL to get the expected edge at counter value 1 (CN0=1).

GTM_AI.298 TOM/ATOM: wrong output behaviour in SOMP oneshot mode when oneshot pulse is triggered by TIM_EXT_CAPTURE(x)29

If TOM/ATOM is configured in SOMP oneshot mode (OSM = 1) and the oneshot trigger is configured to TIM_EXT_CAPTURE(x) (OSM_TRIG = 1, EXT_TRIG = 1) the output behaviour is not as expected depending on the selected CMU clock.

1. If the selected CMU clock is configured to sys_clk (ATOM: CMU_CLK_[z]_CTRL = 0, TOM: CMU_FXCLK0 used) no initial oneshot period (CN0 is set to zero and then counts until CN0 >= CM0) is executed and the output is set to SL immediately and not as expected after the first initial period.
2. If the selected CMU clock is configured to CMU_CLK_[z]_CTRL > 0 (ATOM)/CMU_FXCLK[1..n] (TOM) then an initial period is executed but the output is set immediately to SL and not as expected when the second oneshot period starts.

Scope

TOM/ATOM SOMP oneshot mode

Effects

The TOM/ATOM output is set immediately to SL and not as expected with a delay of the first initial oneshot period.

Workaround

For GTM generation v2 no workaround is available.

If it is possible configure the selected CMU clock to sys_clk period. Then the generated oneshot pulse length is correct but without executing of the initial period.

GTM_AI.299 TOM/ATOM: wrong output behaviour in SOMP oneshot mode when oneshot pulse is triggered by trig_[x-1]

If TOM/ATOM is configured in SOMP oneshot mode (OSM = 1) and the oneshot trigger is configured to trigger signal from trigger chain trig_[x-1] (OSM_TRIG = 1, EXT_TRIG = 0) the output signal is set immediately to SL and not as expected after a delay of the first initial oneshot period (CN0 counts from 0 until it reaches the value of CM0). The first initial oneshot period isn't executed.

Scope

TOM/ATOM SOMP oneshot mode

Effects

The TOM/ATOM output is set immediately to SL and not as expected with a delay of the first initial oneshot period.

Workaround

For GTM generation v2 no workaround is available.

If it is possible work without the initial period for GTM generation v2 because the generated pulse length is correct.

GTM_TC.009 TBU signals not wired to debug logic

The TBU signals are not wired from the GTM kernel to the OTGB interface. Therefore, TBU signals are not available for debug purposes.

The other GTM signals are connected to the debug system as specified.

Note: This limitation will not be present on TC23x Emulation Devices.

GTM_TC.012 Read Access Control by Register ODA

Specific GTM registers have by default “destructive read” behavior as their normal read behavior (see section “GTM Software Debugger Support” in the GTM chapter of the User’s Manual for further details.)

Depending on the reading master and the configuration of bits DREN and DDREN in register GTM_ODA (OCDS Debug Access Register), the read can be performed “non-destructive” for debug related read operation.

According to the User’s Manual the read is performed “non-destructive” (i.e. debug related read operation)

- for all masters when ODA.DREN = 1_B,
- for the Cerberus (OCDS) FPI master when ODA.DREN = 0_B and ODA.DDREN = 0_B.

Problem Description

In the current implementation the read is performed “non-destructive” (i.e. debug related read operation)

- for all masters when ODA.DREN = 1_B,
- for the DMA Partition 2 FPI master when ODA.DREN = 0_B and ODA.DDREN = 0_B.

Workaround

The problem described above has 2 aspects:

1. For DMA Partition 2 Access to GTM

When the DMA Partition 2 FPI master is used to perform a normal (“destructive”) read of the GTM registers that by default have “destructive read” behavior as their normal read behavior, setting ODA.DREN = 0_B and ODA.DDREN = 1_B is required to avoid an unintended debug related (“non-destructive”) read access that would be caused by this issue.

2. For Cerberus (OCDS) Access to GTM

When ODA.DREN = 0_B and ODA.DDREN = 0_B, any read access of the Cerberus (OCDS) FPI master to the registers that by default have “destructive read” behavior as their normal read behavior will cause the normal (“destructive”) read behavior. To get the intended debug related (“non-destructive”) read behavior, ODA.DREN needs to be set to 1_B before each access of the Cerberus and set back to 0_B afterwards to not affect the access of other FPI masters on the registers described above.

IOM_TC.002 Missed or spurious IOM events when pulse length exceeds Event Window counter range

When using the Logic Analyzer Module (LAM) of the IOM, if the 24-bit counter for the Event Window exceeds its maximum value (0xFFFFFF) it wraps around and starts counting again from 0x0.

If the Event Window is not inverted (LAMCFG.IVW = 0_B), for example for measuring long pulses, and the edge that generates an event comes after the counter exceeded its maximum value, the event will not be generated if the counter, due to the rollover, is again below the threshold value (LAMEWS.THR), outside of the Event Window.

As an additional side effect of the wraparound, spurious events may be generated when expecting an alarm only in case of pulses that are too short, if a pulse is longer than the counter can handle.

Workaround

Avoid measuring pulses longer than the Event Window counter range.

IOM_TC.003 Unexpected Event upon Kernel Reset

If a kernel reset (via bits RST in registers KRST0/1) is performed on the IOM, an unexpected event may be signalled to the SMU.

Workaround

Before triggering a kernel reset via software, set the alarm reaction in SMU to “No Action” to avoid reaction on the unexpected event.

IOM_TC.004 Write to IOM register space when IOM_CLC.RMC > 1

If a clock divider value RMC > 1 is selected in register IOM_CLC, more than one write access may be performed to the IOM register address space within one IOM clock cycle.

This will cause unpredictable effects on the internal state for the following scenarios where two (or even multiples of 2) write accesses are performed within one IOM clock cycle to the following register groups:

- ECM registers ECMCCFG and/or ECMSELR, or
- ECM Event Trigger History registers ECMETH0 and/or ECMETH1, or
- FPC registers FPCESR, FPCCTRk and/or FPCTIMk, or
- LAM registers LAMCFGm and/or LAMEWSm.

Note: No problem will occur for read accesses.

Workaround

Set IOM_CLC.RMC = 1 when configuring (writing to the registers of) the IOM.

During runtime (not configuring IOM) IOM_CLC.RMC > 1 is not an issue.

MTU_TC.005 Access to MCx_ECCD and MCx_ETRRi while MBIST disabled

It is possible to access the memory controller registers MCx_ECCD and MCx_ETRRi without the need of the MBIST mode being enabled (i.e. without MTU_MEMTEST.MEMxEN = 1_B). This may be used to avoid a complete SRAM initialization on certain security relevant SRAMs.

However, when a MBIST controller is disabled (MTU_MEMTEST.MEMxEN = 0_B), there is an inevitable corner case that causes the value read/written from/to registers MCx_ECCD and MCx_ETRRi of a disabled MBIST controller to be wrong. There is also a possibility that an SPB error is triggered when accessing

the MCx_ECCD and MCx_ETRRi registers if other masters concurrently use the SPB bus in this situation.

Note: No workaround is required to access the registers of an enabled MBIST controller.

Workaround

When MBIST mode is disabled (MTU_MEMTEST.MEMxEN = 0_B) for a MBIST controller,

- ensure that the module kernel clock is enabled for the access to MCx_ECCD and MCx_ETRRi,
- and perform a dummy write to MCx_ECCD with value $780F_H$ before any read/write access to MCx_ECCD or MCx_ETRRi.

Note: The module kernel clock (of the module in which the SRAM is present) does not need to be enabled if it can be ensured that no concurrent SPB bus accesses by other masters (CPU, DMA, HSM, debugger, ..) to other modules are performed during the MCx_ECCD/ETRRi access while the module kernel clock is disabled.

The module kernel clock is enabled under the following conditions:

1. For CPU memories, the clock is enabled after reset (for CPUx with x>0 even when CPUx is still in BOOT-HALT mode), when the CPU is not explicitly put into IDLE mode by software.
2. For SRAMs in peripherals, the module kernel clock is enabled when the module clock is enabled via the CLC register.

The value $780F_H$ has been chosen as an example based on the following use cases and assumptions:

- If error reporting is turned on (i.e. notification enable bits *ENE are set), it does not disturb the system to write back $780F_H$ to register ECCD (write back of reset values, write to read-only bits and write of 1_B to error indication bits has no effect).
- If error reporting is turned off (i.e. notification enable bits *ENE are cleared), write back of $780F_H$ to register ECCD may trigger SMU alarms (if SMU is configured). It is assumed that the corresponding errors are already known by the system since error reporting had previously been deactivated.

MTU_TC.007 Error Overflow Indication ECCD.EOV

The Error Overflow Indication bit EOV in register ECCD does not work correctly in specific cases for the following modules:

E-Ray, ETH, GTM, CIF (in ADAS devices), MCDS (in emulation devices), DAM.

The problem occurs in the following cases:

- If an error (correctable, uncorrectable, address error) was detected at address 0, this error is correctly stored in the ETRR register (ETRR.ADDR = 0x0, flags SERR, CERR, UERR are set accordingly), and bit ECCD.5 (least significant bit of bit field VAL) is set to 1_B.
  - However, a subsequent error on a different address doesn't generate an error overflow, i.e. bit ECCD.EOV isn't set to 1_B.
- If an error (correctable, uncorrectable, address error) was detected at an address addr_x > 0, this error is correctly stored in the ETRR register (ETRR.ADDR = addr_x, flags SERR, CERR, UERR are set accordingly), and bit ECCD.5 (least significant bit of bit field VAL) is set to 1_B.
  - However, a subsequent read from same addr_x which is still erroneous will erroneously generate an error overflow, i.e. bit ECCD.EOV is set to 1_B.

Workaround

Test address 0x0 by software to identify whether the device is sensitive to the first effect described above.

Periodically check bit field VAL in register ECCD. If VAL ≠ 0, save the contents stored in ETRR (ADDR and MBI), and clear ECCD and ETRR afterwards (via ECCD.TRC = 1_B). If an error overflow is signaled, compare the current contents of ETRR with the saved value to identify an unmotivated error overflow (second effect described above).

MTU_TC.011 MBIST Bitmap not working for w0 - r1

The simple test case of writing all 0 and checking for 1 should return a full bitmap.

However, in this device step, only one (the last) address of the SRAM is returned.

Workaround

Use the reverse test w1 - r0, which is working as expected and returns the full bitmap.

MTU_TC.012 Security of CPU Cache Memories During Runtime is Limited

MTU chapter “Security Applications” in the User’s Manual describes that selected memories with potentially security relevant content are initialized under certain conditions to prevent reading of their data or supplying manipulated data.

The description is correct, but the initialization of CPU cache and cache tag memories triggered by MBIST enable/disable and when mapping/un-mapping these memories to/from system address space using MEMMAP register is of limited value:

- These memories stay functional as cache in the address mapped state. Therefore software can enable address mapping and afterwards watch cache usage of the application (this is a debug feature). Even manipulation of the cache content is feasible.
- It is possible to abort an ongoing memory initialization.

The security of memory initialization during startup is not affected. Also protection of FSI0 and HSM memories is not limited.

Workaround

Handle security relevant data exclusively inside HSM. Protect the application code by locking external access (e.g. lock debug interface, prevent boot via serial interface). Consider validation of application code by HSM secure boot.

MultiCAN_TC.043 CAN FD: Idle Condition

Note: This problem does not affect the nodes in TC23xED and ADAS devices. In TC23x step AC, this problem only affects node 2 of modules MultiCAN and MultiCAN1.

The CAN FD ISO draft hardens the idle condition for the integration phase. Now it is also required that the 11 consecutive recessive bits occur without any synchronization in between. This is to ensure that integration of a node during a fast CAN FD data phase is not irritated by the fast baudrate.

Problem Description

If a fast CAN FD data phase is overlapping with the integration phase, the CAN module might end the integration phase too early.

As a result, the node is not properly synchronized and might produce an error on the bus.

Workaround

None

MultiCAN_TC.044 CAN FD: Missing Hardsync

Note: This problem does not affect the nodes in TC23xED and ADAS devices. In TC23x step AC, this problem only affects node 2 of modules MultiCAN and MultiCAN1.

The CAN FD specification requires hard synchronization from the transition recessive FDF bit to dominant res bit being enabled. Hard-synchronization insures perfect synchronization, even for large timing offsets, due to arbitration loss.

Current Implementation

Soft synchronization is implemented at FDF bit, no hard synchronization as required.

Problem Description

Soft-synchronization is enabled for the transition recessive FDF bit to dominant res bit. In case of a time offset higher than the SJW (Synchronization Jump Width), only partial synchronization is achieved. This might not be sufficient for high speed CAN FD data phase.

Incorrect Behavior

If a transmitter is losing arbitration late (e.g. in an extended frame - see **Figure 4** the node which wins arbitration and **Figure 5** the transmitting node loosing arbitration), then the FDF bit to res bit is the last chance to synchronize to the winning node (here as a receiver **Figure 6** the same node as in **Figure 5**). A timing offset will occur between the now receiving node and the actual transmitter.

Consequence

The device is producing more error frames within a network than a device with a hardsync at the FDF bit.

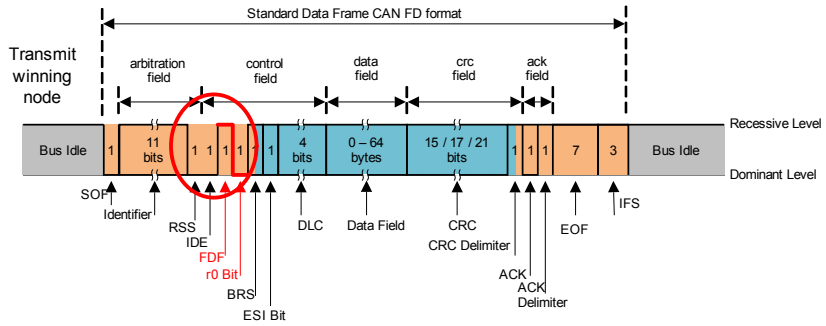

Figure 4 Transmitter - winning CAN FD node

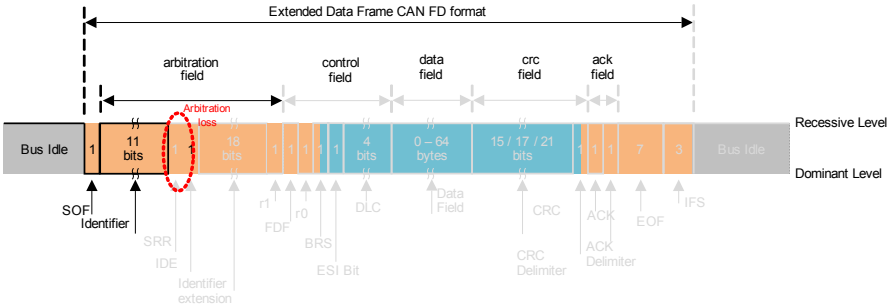

Figure 5 Transmitter - loosing CAN FD node

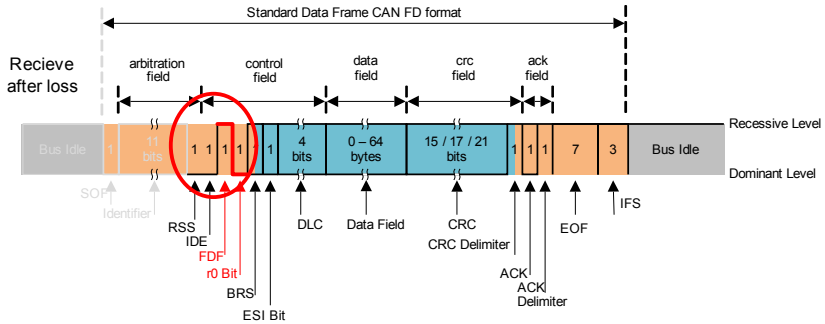

Figure 6 Now receiver (same node as previous figure) - loosing CAN FD node

Workaround

This workaround is not 100% solving the “Missing Hardsync“ issue, but setting the SJW to the highest possible value will hide the problem in most cases.

OCDS_TC.038 Disconnecting a debugger without device reset (“hot detach”) may require reading of OCS registers

If a debugger disconnects, it should activate at least the Debug Reset. This will reset all the main OCDS resources like CPUs, Cerberus, etc. However for peripherals having a BPI interface, there is the following issue: The Debug

Reset is implemented as a synchronous clear on this level. If the OCDS registers are not clocked (e.g. for power saving reasons), the effect of this synchronous clear will be delayed to the next activation of the clock.

In general this will be more a theoretical problem. It's very unlikely that there is a use case, where a hot detach is required and critical OCDS resources of peripherals were used before. In nearly all cases this effect is invisible for a user, since any register access of the peripheral will generate the clock cycles which are required for the synchronous clear.

Workaround

In case of a hot detach, a tool should - after the Debug Reset activation - read the OCS registers of all peripherals where it used critical OCDS resources. These reads will initiate the required peripheral kernel clocks for the synchronous clear of the OCDS resources.

OCDS_TC.042 OTGS capture registers can miss single clock cycle triggers

The Cerberus OTGS capture registers (TCTL, TCCB, TCCH, TCIP, TCTGB, TCM) can fail to capture a trigger if the trigger is of single clock cycle duration and arrives in the same cycle as the same trigger register is being read by the bus.

Workaround

Avoid polling of OTGS capture registers while the system is running.

If polling while running can't be avoided use TLCCx counters for capturing critical Trigger Lines.

OCDS_TC.043 Read-Modify-Write Bus Transactions to Cerberus Registers

During read-modify-write (RMW) bus transactions to writable registers in the Cerberus (CBS), the target register is incorrectly updated with an undefined value during the Read-part. The correct value is always returned to the bus

master for the Read-part, and the correct value is written to the register when the Write-part completes. But the register may contain an undefined value for a number of clock cycles between the Read-part and the Write-part.

The bus master (CPU) will see the RMW complete normally, but any logic driven by the hardware register's writable bits may be unexpectedly toggled.

This effects all registers that can be written by the SPB (using the FPI protocol) in the CBS block. It does not effect external access from the tool via JTAG/DAP.

Workaround

Do not use RMW bus operations targeting the CBS registers.

PLL_ERAY_TC.001 PLL_ERAY Initialization after Cold Power-up or Wake-up from Standby mode

When the PLL_ERAY is configured by the application software after cold power-on reset or wake-up from Standby mode, it may not always reach the intended target frequency (either lock at a lower frequency, or go into unlock state), in particular at high temperature.

Workaround

The following code sequence, executed after power-on reset or wake-up from Standby mode and before initializing the PLL_ERAY, avoids the problem:

```
SCU_PLLERAYCON0.B.PLLPWD = 0;  // set PLL_ERAY to power
                                   saving mode
wait(10);                      // wait 10µs
SCU_PLLERAYCON0.B.PLLPWD = 1;  // set PLL_ERAY to normal
                                   behavior
...                            // initialize PLL_ERAY
```

PLL_TC.005 PLL Initialization after Cold Power-up or Wake-up from Standby mode

When the system PLL is configured by the application software after cold power-on reset or wake-up from Standby mode, it may not always reach the

intended target frequency (either lock at a lower frequency, or go into unlock state), in particular at high temperature.

Workaround

The following code sequence, executed after power-on reset or wake-up from Standby mode and before initializing the system PLL, avoids the problem:

```
SCU_CCUCON0.B.CLKSEL = 0;  // switch system clock to
      another source different from PLL, e.g. back-up clock
SCU_CCUCON0.B.UP = 1;      // request update
SCU_PLLCON0.B.PLLPWD = 0;  // set PLL to power saving mode
wait(10);                  // wait 10µs
SCU_PLLCON0.B.PLLPWD = 1;  // set PLL to normal behavior
...                        // initialize PLL
```

Note: For devices with PLL_ERAY, see also problem PLL_ERAY_TC.001

PMC_TC.002 Switch Capacitor Regulator Mode, Frequency Spreading - Documentation Update to Register EVRSDCTRL1

The documentation of bit fields SDFREQSPRD, TON, TOFF in register EVRSDCTRL1 will be updated with the next revision of the User's Manual.

1. Documentation Update to SDFREQSPRD

The correct encoding of bit field SDFREQSPRD (Frequency Spread Mode) in register EVRSDCTRL1 is as documented in **Table 7**:

Table 7 EVR13 SD Control Register 1 (EVRSDCTRL1) - Frequency Spread Mode Encoding

Field	Bits	Type	Description
SDFREQSPRD	[3:0]	rw	**Frequency Spread Mode** This bit field defines the maximum number of back-up clock cycles (f_{BACK}) which are added to both charge (TON) and discharge (TOFF) switching phases thus increasing the average switching period. The number of clock cycles added are randomized equally over the listed cycle count range. The resulting TON and TOFF phase lengths are the same and 50% duty cycle is maintained. 0_H No frequency spreading activated. 1_H 0 to 3 clock cycles are added (default). 2_H 0 to 7 clock cycles are added. All other values are reserved.

2. Documentation Update to TON/TOFF

The effect of bit field EVRSDCTRL1.SDFREQSPRD on the SC DCDC switching period is as documented in **Table 8**:

Table 8 EVR13 SD Control Register 1 (EVRSDCTRL1) - Switching Period

Field	Bits	Type	Description
TON	[15:8]	rw	**Charge Phase Length** The charge phase length is defined in back-up clock cycles (f_{BACK}, nominal 100 MHz): • In case SDFREQSPRD = 0: – Switching period (in cycles) = TON + TOFF + 18. • In case SDFREQSPRD ≠ 0: – Switching period (in cycles) = TON + TOFF + 18 + 2 * [$2^{(SDFREQSPRD + 1)}$ - 1].
TOFF	[23:16]	rw	**Discharge Phase Length** The discharge phase length in clock cycles should be the same as the charge phase length.

PMC_TC.003 Usecase limitation of LDO mode with on chip pass device for SAL devices

Note: This problem only affects devices with temperature range classification "SAL" (ambient temperature range -40/150°C). For devices classified as "SAK" (-40/125°C), T_J is limited to 150°C anyway (see Data Sheet).

The LDO mode of the internal EVR13 regulator with on-chip pass device shall not be used at condition $T_J > 150°C$.

Junction temperature $T_J > 150°C$ leads to degradation of the pass device characteristics resulting in a deviation of the static accuracy (V_{OUTT}) of the EVR13 core regulator.

If the junction temperature is increased above 150°C in an application with the on-chip pass device, deviation of the static accuracy down to -3% of the nominal voltage is possible for I_{DD} load currents above 150 mA at the respective device junction temperature. The application shall be tolerable to such deviation of the output voltage accuracy considering limits for the dynamic regulation of the EVRC.

QSPI_TC.006 Baud rate error detection in slave mode (error indication in current frame)

According to the specification, a baud rate error is detected if the incoming shift clock supplied by the master has less than half or more than double the expected baud rate (determined by bit field GLOBALCON.TQ).

However, in this design step, a baud rate error is detected not only if the incoming shift clock has less than half the expected baud rate (as specified), but also already when the incoming shift clock is somewhat (i.e. less than double) higher than the expected baud rate.

In this case, the baud rate error is indicated in the current frame.

Workaround

It is recommended not to rely on the baud rate error detection feature, and not to use the corresponding automatic reset enable feature (i.e. keep GLOBALCON.AREN=0_B).

The baud rate error detection feature in slave mode is of conceptually limited use and is not related to data integrity. Data integrity can be ensured e.g. by parity, CRC, etc., while clocking problems of an AURIX™ master are detected by mechanisms implemented in the master.

Protection against the effects of high frequency glitches is provided by the spike detection feature in slave mode.

RESET_TC.005 Indication of Power Fail Events in SCU_RSTSTAT

In case of consecutive cold resets triggered by EVR13, EVR33 or SWD power fail events, then only the last power fail event is registered in register SCU_RSTSTAT. It is not possible to distinguish individually between EVR13, EVR33 or SWD power fail events from RSTSTAT information.

Workaround

In case any power fail reset indication bit is set among EVR13, EVR33 or SWD power fail events in register SCU_RSTSTAT, it has to be assumed that all power fail events may have happened before.

SMU_TC.006 OCDS Trigger Bus OTGB during Application Reset

The SMU provides an alarm trigger and trace interface (Trigger Set TS16_SMU) using the OCDS Trigger Bus OTGB.

While the Application Reset is active, the SMU outputs the reset state of the OTGB interface instead of TS16_SMU.

This OTGB interface reset state is identical to TS16_SMU when no alarm is active.

After the Application Reset TS16_SMU is output again.

Workaround

Just ignore the phase in the OTGB trace where an alarm seems to become inactive while the Application Reset is active.

SMU_TC.007 Size and Position of Field ACNT in Register SMU_AFCNT

Note: This erratum might affect the SFR C Header Definitions. In such cases, SFR usage in the software shall be analyzed within the applications for their correct handling.

In the SMU chapter of the User's Manual, in the description of register SMU_AFCNT (Alarm and Fault Counter),

- Size and position of field ACNT (Alarm Counter) are incorrectly described as SMU_AFCNT.[15:8], and
- Bits SMU_AFCNT.[7:4] are incorrectly shown as "Reserved; read as 0".

The **correct** size and position of field ACNT (Alarm Counter) in register SMU_AFCNT is SMU_AFCNT.[**15:4**], as shown in the following **Table 9**.
The position of the "Reserved" bits is aligned accordingly.

Table 9 Field ACNT in Register SMU_AFCNT - Correction

Field	Bits	Type	Description
ACNT	[15:4]	rh	**Alarm Counter** This field is incremented by hardware when the SMU processes an **internal** action related to an alarm event (see Figure **"Alarm operation"**). The counter value holds if the maximum value is reached.
0	[29:16]	r	**Reserved** Read as 0; should be written with 0.

Note: The other fields (ACO, FCO, FCNT) of register SMU_AFCNT are correctly described in the User's Manual.

SMU_TC.008 Behavior of Action Counter ACNT

Register SMU_AFCNT (Alarm and Fault Counter) implements a Fault Counter (FCNT) that counts the number of transitions from the RUN state to the FAULT state. Register AFCNT is only reset by a power-on-reset.

Whenever a pending alarm event is processed, the corresponding status bit is set to 1_B by hardware in the Alarm Status register AG<x>.

If an internal SMU action is configured for this alarm, the Action Counter (ACNT) in register AFCNT is incremented anytime the SMU processes this internal action.

Corner Case

In this device step, some of the alarm signals may increment the Action Counter ACNT multiple times for a single alarm event.

Workaround

Do not rely on the value in the action counter ACNT.

SMU_TC.010 Transfer to SMU_AD register not triggered correctly

Background

The SMU contains Alarm Debug registers which can be used for diagnostic purposes. If an alarm which is configured to generate a reset (application or system reset) is sent to the SMU, a copy of the Alarm Status registers – AGi – into the Alarm Debug registers – ADi – is automatically triggered.

The AGi are reset by Application reset while the ADi are reset only by power-on reset.

Corner Case

In the case that a first SMU alarm AGi[j] generates a reset request, and a second alarm AGx[y] (where x=i and y=j is possible) configured for a reset occurs a few cycles before the reset is actually executed, then the reset values of the AGi registers will be transferred to the ADi register.

In this case, the ADi registers will not reflect the root cause that lead to a SMU alarm/reset.

Note: This corner case will always be met for level alarms.

SRI_TC.003 XBAR_PRIOL/H Register Layout and Reset Values

Note: This erratum might affect the SFR C Header Definitions. In such cases, SFR usage in the software shall be analyzed within the applications for their correct handling.

The CPU0 SRI masters (CPU0.DMI, CPU0.PMI) are mapped to the XBar_SRI Master Connection Interfaces MCI12 and MCI13 as described in table “Mapping of TC21x/TC22x/TC23x SRI master devices to MCI” of the User’s Manual.

Note: This implementation in the TC23x .. TC21x devices is compatible with the other devices (TC29x .. TC26x) of the AURIX™ family.

However, the description of the register layout and reset values for the XBAR_PRIOL/H registers in chapter “TC21x/TC22x/TC23x Control Registers” of the TC21x/TC22x/TC23x Family User’s Manual V1.1 is partially incorrect.

The corrected parts of the description are shown in the following tables.

Table 10 XBAR_PRIOL Registers - Reset Values TC23x

Short Name	Description	Reset Value
XBAR_PRIOLD	Arbiter Priority Register D	0020 0002$_H$
XBAR_PRIOL0	Arbiter Priority Register 0	0020 0002$_H$
XBAR_PRIOL4	Arbiter Priority Register 4	0020 0002$_H$
XBAR_PRIOLx (x = 6-7)	Arbiter Priority Register x	0020 0002$_H$

Table 11 XBAR_PRIOL Registers - Fields TC23x

Field	Bits	Type	Description
MASTER0	[2:0]	rw	**Master 0 Priority** (Priority of DMA Access)
MASTER5	[22:20]	rw	**Master 5 Priority** (Priority of SFI Access)
0	[31:23], [19:3]	r	**Reserved** Read as 0; should be written with 0.

Table 12 XBAR_PRIOH Registers - Reset Values TC23x .. TC21x

Short Name	Description	Reset Value
XBAR_PRIOHD	Arbiter Priority Register D	0055 0000$_H$
XBAR_PRIOH0	Arbiter Priority Register 0	0055 0000$_H$
XBAR_PRIOH4	Arbiter Priority Register 4	0055 0000$_H$
XBAR_PRIOHx (x = 6-7)	Arbiter Priority Register x	0055 0000$_H$

Table 13 XBAR_PRIOH Registers - Fields TC23x .. TC21x

Field	Bits	Type	Description
MASTER12	[18:16]	rw	**Master 12 Priority** (Priority of CPU0.DMI Access)
MASTER13	[22:20]	rw	**Master 13 Priority** (Priority of CPU0.PMI Access)
0	[31:23], 19, [15:0]	r	**Reserved** Read as 0; should be written with 0.

3 Deviations from Electrical- and Timing Specification

ADC_TC.P010 Increased Gain Error (EA_{GAIN}) for T_J < 0°C

For devices with Analog-Digital-Converters (VADC) providing 16:1 analog multiplexers (TC26x, TC23x..TC21x), the maximum Gain Error (EA_{GAIN}) increases as follows for T_J < 0°C:

- from ±3.5 LSB_{12} to ±4.5 LSB_{12} when V_{DDM} = 4.5 V to 5.5 V (upper voltage range) and sample time t_S < 200 ns,
- from ±5.5 LSB_{12} to ±6.5 LSB_{12} when V_{DDM} = 2.97 V to 4.5 V (lower voltage range) and sample time t_S < 400 ns.

Note:

1. The resulting Total Unadjusted Error (TUE) is not affected and remains as specified in the corresponding Data Sheet.
2. For temperatures T_J ≥ 0°C, the Gain Error (EA_{GAIN}) remains as specified in the corresponding Data Sheet.
3. For t_S ≥ 200 ns (upper voltage range) or t_S ≥ 400 ns (lower voltage range), the Gain Error (EA_{GAIN}) remains as specified in the corresponding Data Sheet.

IDD_TC.H001 IPC Limits used in Production Test for IDD Max Power Pattern

Instructions per cycle for a CPU is measured by dividing ICNT instruction counter value with the CCNT clock counter value.

Note: For a complete description of registers ICNT and CCNT refer to the TriCore Architecture Manual, chapter "Performance Counter Registers".

Parameters using the max power pattern for device individual testing of power consumption limits (IDD) are tested for a maximum IPC rate of 1.3 for all CPUs available in the device.

PADS_TC.H004 PN-Junction Characteristics for Pad Type S

As described in chapter “Package and Pinning Definitions” in the Data Sheet, symbol “S” in column “Type” is defined as class D ADC input with digital input.

Consequently, for pad type S, the PN-junction characteristics for pad type D apply.

The corresponding values for U_{IN} are listed in tables “PN-Junction Characteristics for positive Overload” and “PN-Junction Characteristics for negative Overload” in chapter “Pin Reliability in Overload” in the Data Sheet.

RTH_TC.H001 Thermal characteristics of the package - Footnote update for LF-BGA-292-6 package

The references to the JEDEC standards (JESD51-3/5/7) for RQJA in the footnote for the LF-BGA-292-6 package in table “Thermal characteristics of the package” are not correct. They only apply to the TQFP package.

Correction

The correct footnote for the LF-BGA-292-6 package is:

[3]) Value is defined in accordance with JESD51-9.

VDDPPA_TC.H001 Voltage to ensure defined pad states - Footnote update

In the footnote for parameter “Voltage to ensure defined pad states” (symbol V_{DDPPA}) in table “Operating Conditions” of the Data Sheet, V_{DDP3} is mentioned as representative for “non-core supply voltages” in the text.

Update

The footnote for V_{DDPPA} should be extended to include all “non-core supply voltages” as follows:

*) This parameter is valid under the assumption the PORST signal is constantly at low level during the power-up/power-down of the “non-core supply voltages”

(V_{DDP3}, V_{EXT}, V_{FLEX}, V_{DDFL3}, V_{DDM}, ..., depending on the respective TC2x device version).

4 Application Hints

ADC_AI.H003 Injected conversion may be performed with sample time of aborted conversion

For specific timing conditions and configuration parameters, a higher prioritized conversion c_i (including a synchronized request from another ADC kernel) in cancel-inject-repeat mode may erroneously be performed with the sample time parameters of the lower prioritized cancelled conversion c_c. This can lead to wrong sample results (depending on the source impedance), and may also shift the starting point of following conversions.

The conditions for this behavior are as follows (all 3 conditions must be met):

1. **Sample Time setting**: injected conversion c_i and cancelled conversion c_c use different sample time settings, i.e. bit fields `STC*` in the corresponding Input Class Registers for c_c and for c_i (`GxICLASS0/1, GLOBICLASS0/1`) are programmed to different values.
2. **Timing condition**: conversion c_i starts during the first f_{ADCI} clock cycle of the sample phase of c_c.
3. **Configuration parameters**: the ratio between the analog clock f_{ADCI} and the arbiter speed is as follows:

   $$N_A > N_D*(N_{AR}+3),$$

   with

   a) N_A = ratio f_{ADC}/f_{ADCI} (N_A = 1 .. 32, as defined in bit field `DIVA`),

   b) N_D = ratio f_{ADC}/f_{ADCD} = number of f_{ADC} clock cycles per arbitration slot (N_D = 1 .. 4, as defined in bit field `DIVD`),

   c) N_{AR} = number of arbitration slots per arbitration round (N_{AR} = 4, 8, 16, or 20, as defined in bit field `GxARBCFG.ARBRND`).

Bit fields `DIVA` and `DIVD` mentioned above are located in register `GLOBCFG`.

As can be seen from the formula above, a problem typically only occurs when the arbiter is running at maximum speed, and a divider $N_A > 7$ is selected to obtain f_{ADCI}.

Recommendation 1

Select the same sample time for injected conversions c_i and potentially cancelled conversions c_c, i.e. program all bit fields `STC*` in the corresponding Input Class Registers for c_c and for c_i (`GxICLASS0/1, GLOBICLASS0/1`) to the same value.

Recommendation 2

Select the parameters in register `GLOBCFG` and `GxARBCFG` according to the following relation:

$N_A \leq N_D*(N_{AR}+3)$.

ADC_TC.H011 Bit DCMSB in register GLOBCFG

The default setting for bit DCMSB (Double Clock for the MSB Conversion) in register GLOBCFG is 0_B, i.e. one clock cycle for the MSB conversion step is selected.

DCMSB = 1_B is reserved in future documentation and must not be used.

Note: In devices supporting Workaround 4 of problem ADC_TC.068, DCMSB = 1_B may be used to control synchronization of converter groups (for details, see ADC_TC.068, Workaround 4).

ADC_TC.H014 VADC Start-up Calibration

The formula for the duration of the start-up calibration in some versions of the TC2x User's Manuals is incorrect with respect to the used frequency, or missing.

In the following, the contents of chapter "Calibration" is reprinted, including the correct **Formula for Start-up Calibration** below.

Calibration

Calibration automatically compensates deviations caused by process, temperature, and voltage variations. This ensures precise results throughout the operation time.

An initial start-up calibration is required once after a reset for all converters. All converters must be enabled (ANONS = 11_B). The start-up calibration is initiated globally by setting bit SUCAL in register GLOBCFG. Conversions may be started after the initial calibration sequence. This is indicated by bit CALS = 1_B AND bit CAL = 0_B.

Formula for Start-up Calibration

The start-up calibration phase takes 4352 f_{ADCI} cycles (4352 × **50 ns** = 217.6 µs for f_{ADCI} = 20 MHz).

After that, postcalibration cycles will compensate the effects of drifting parameters. The postcalibration cycles can be disabled.

Note: The ADC error depends on the temperature. Therefore, the calibration must be repeated periodically.

ADC_TC.H015 Conversion Time with Broken Wire Detection

As described in a note in section “Broken Wire Detection” of the User’s Manual, the duration of the complete conversion is increased by the preparation phase (same as the sample phase) if the broken wire detection is enabled, i.e. the sample time doubles for standard conversions when broken wire detection is enabled (GxCHCTRy.BWDEN = 1_B):

Formula for Standard Conversions without Broken Wire Detection

- $t_{CN} = t_s + (N + PC) \times t_{ADCI} + 2 \times t_{VADC}$ (see also User’s Manual/Data Sheet)

Formula for Standard Conversions with Broken Wire Detection

- $t_{CN} = 2 \times t_s + (N + PC) \times t_{ADCI} + 2 \times t_{VADC}$

where:

$t_s = (2 + STC) \times t_{ADCI}$ for STC ≤ 15, and

$t_s = (2 + (STC-15) \times 16)) \times t_{ADCI}$ for STC ≥ 16;

N = result width (8/10/12 bits);

PC = 2 if post-calibration selected, PC = 0 otherwise.

Examples

Conversion times for different configurations are shown in the following **Table 14** (without broken wire detection) and **Table 15** (with broken wire detection):

Table 14 Conversion Time for Standard Conversions - Without Broken Wire Detection - Examples

Result	Symbol	Time	Conditions
12-bit result	t_{C12}	(16 + STC) x t_{ADCI} + 2 x t_{VADC}	Post-calibration enabled, STC ≤ 15
10-bit result	t_{C10}	(12 + STC) x t_{ADCI} + 2 x t_{VADC}	Post-calibration disabled, STC ≤ 15
8-bit result	t_{C8}	(10 + STC) x t_{ADCI} + 2 x t_{VADC}	Post-calibration disabled, STC ≤ 15

Table 15 Conversion Time for Standard Conversions - With Broken Wire Detection - Examples

Result	Symbol	Time	Conditions
12-bit result	t_{C12B}	(18 + 2 x STC) x t_{ADCI} + 2 x t_{VADC}	Post-calibration enabled, STC ≤ 15
10-bit result	t_{C10B}	(14 + 2 x STC) x t_{ADCI} + 2 x t_{VADC}	Post-calibration disabled, STC ≤ 15
8-bit result	t_{C8B}	(12 + 2 x STC) x t_{ADCI} + 2 x t_{VADC}	Post-calibration disabled, STC ≤ 15

ADC_TC.H020 Minimum/Maximum Detection Compares 12 Bits Only

In minimum or maximum detection mode (FEN = 11_B or 10_B) new results are compared to the lower 12 bits of the respective result register bitfield RESULT.

Therefore, a value RESULT = $XFFF_H$ ($X > 0_H$) will not be updated for a new result value of $0FFF_H$ in minimum detection mode.

In a real application, this should be no problem, as the minimum detection usually sees values below $0FFF_H$.

Recommendation

For minimum detection, use the start value $0FFF_H$ (instead of $FFFF_H$ as mentioned in the User's Manual).

For maximum detection, use the start value 0000_H as mentioned in the User's Manual.

ADC_TC.H022 Sample Time Control - Formula

Table "Sample Time Coding" in section "Input Class Registers" of the VADC chapter in the User's Manual describes the additional clock cycles (selected in bit fields STCS and STCE) to be added to the minimum sample time of two analog clock cycles.

As can be seen from the table in the User's Manual, the step width in the coding depends on the MSB of STCi (i = S or E). The following **Table 16** has been copied from the User's Manual, with the corresponding formula added in the last column:

Table 16 Sample Time Coding

STCS / STCE	Additional Clock Cycles[1)]	Resulting Sample Time	Clock Cycle Formula
$0\ 0000_B$	0	$2 / f_{ADCI}$	2 + STCi
$0\ 0001_B$	1	$3 / f_{ADCI}$	
...	...	...	
$0\ 1111_B$	15	$17 / f_{ADCI}$	
$1\ 0000_B$	16	$18 / f_{ADCI}$	2 + (STCi - 15) x 16
$1\ 0001_B$	32	$34 / f_{ADCI}$	
...	...	...	
$1\ 1110_B$	240	$242 / f_{ADCI}$	
$1\ 1111_B$	256	$258 / f_{ADCI}$	

1) The number of resulting additional clock cycles listed in this column corresponds to the term “STC” used in the conversion timing formulas in the Data Sheet.

ADC_TC.H024 Documentation: Filter control only in registers GxRCR7/GxRCR15

In sections “Finite Impulse Response Filter Mode (FIR)” and “Infinite Impulse Response Filter Mode (IIR)” of the VADC chapter in the User’s Manual,

- replace this sentence:
  “Several predefined sets of coefficients can be selected via bitfield DRCTR (coding listed in Table xx-6) in registers G0RCRy (y = 0 - 15)ff and GLOBRCR.”
- with this sentence:
  “Several predefined sets of coefficients can be selected via bitfield DRCTR (coding listed in Table xx-6) in registers **GxRCR7** and **GxRCR15**.”

ASCLIN_TC.H001 Bit field FRAMECON.IDLE in LIN slave mode

In LIN slave mode, bit field FRAMECON.IDLE has to be set to 000_B (default after reset), i.e. no pause will be inserted between transmission of bytes.

For FRAMECON.IDLE > 000_B, the inter-byte spacing of the ASCLIN module is not working properly in all cases in LIN slave mode (no bit errors are detected by the ASCLIN module within the inter-byte spacing).

ASCLIN_TC.H003 Behavior of LIN Autobaud Detection Error Flag

Expected Behavior

In ASCLIN, when auto baud detection (LINCON.ABD) is deactivated, the auto baud measurement should still be active and the Autobaud Detection Error Flag FLAGS.LA should be set when the value measured is outside the BRD.LOWERLIMIT and BRD.UPPERLIMIT range.

Actual Behavior

The Autobaud Detection Error Flag FLAGS.LA is not set, as the auto baud measurement is not active when auto baud detection is deactivated (LINCON.ABD = 0).

ASCLIN_TC.H004 Changing the Transmit FIFO Inlet Width / Receive FIFO Outlet Width

Expected Behavior

The Transmit FIFO should write the data to intended location of TxFIFO, even though the Transmit FIFO inlet width TXFIFOCON.INW is changed between the write operations.

The Receive FIFO should read the data from intended location, even though the Receive FIFO outlet width RXFIFOCON.OUTW is changed between the read operations.

Actual Behavior (Transmit FIFO)

The Transmit FIFO does not write the data in the intended location when TXFIFOCON.INW is changed in an increasing order (from 1 to 2 to 4) between write operations.

The Transmit FIFO writes the data only to aligned write index based on the number of bytes to be written (TXFIFOCON.INW).

Example: Assuming that the write index of TxFIFO is from 0 to 15 (16 bytes), when TXFIFOCON.INW = 2, the TxFIFO writes two bytes of data starting only from half-word aligned write index (0, 2, 4, …, 14). Similarly when TxFIFO writes four bytes of data starting only from word aligned write index (0, 4, 8, 12).

Note: This misbehavior is seen only when TXFIFOCON.INW is changed in-between write operations.

Actual Behavior (Receive FIFO)

The Receive FIFO does not read the data from intended location when RXFIFOCON.OUTW is changed in an increasing order (from 1 to 2 to 4) between read operations.

The Receive FIFO reads the data only from aligned read index based on the number of bytes to be read (RXFIFOCON.OUTW).

Example: Assuming that the read index of RxFIFO is from 0 to 15 (16 bytes), when RXFIFOCON.OUTW = 2, the RxFIFO reads two bytes of data starting only from half-word aligned write index (0, 2, 4, …, 14). Similarly when RxFIFO reads four bytes of data starting only from word aligned read index (0, 4, 8, 12).

Note: This misbehavior is seen only when RXFIFOCON.OUTW is changed in-between read operations.

Effect

Previously written data in TxFIFO will be over-written by the new data, when the TxFIFO write index is not aligned with number of data bytes to be written.

Previously read data will be read again, when the RxFIFO read index is not aligned with number of data bytes to be read.

Recommendation

Flush the TxFIFO (TXFIFOCON.FLUSH) or RxFIFO (RXFIFOCON.FLUSH) before TXFIFOCON.INW or RXFIFOCON.OUTW is changed respectively.

ASCLIN_TC.H005 Collision detection error reported twice in LIN slave mode

An ASCLIN module configured as LIN slave node could report a wrong collision detection error during reception of LIN header after detecting a first correct collision detection error during the transmission of a response field of the previous LIN frame.

This misbehavior is observed under the following sequence:

- The LIN slave node detects a collision detection error when there is a bit error in its transmitted response frame, and then it goes to the idle state as expected.
- The master transmits a header onto the LIN bus, and the LIN slave node receives header and tries to capture the identifier inside the header.

- Then the LIN slave node reports another collision error which is wrongly detected during the reception of identifier although there is no corruption of LIN header on the bus.

Recommendation

Ignore the collision detection error which happened during reception phase of a LIN slave node.

BCU_TC.H001 HSM Transaction Information not captured

No HSM transaction information is captured by the System Bus Control Unit (SBCU). Therefore the following HSM related control/status register bits in the SBCU do not have any function:

- Register **SBCU_DBGRNT** (SBCU Debug Grant Mask Register):
  - **HSMCMI**: this control bit has no function. Behavior as described for SBCU_DBGRNT.ONE0.
  - **HSMRMI**: this control bit has no function. Behavior as described for SBCU_DBGRNT.ONE0.
- **Register SBCU_DGNTT** (SBCU Debug Trapped Master Register):
  - **HSMCMI**: this control bit has no function. Behavior as described for SBCU_DBGNTT.ONE0.
  - **HSMRMI**: this control bit has no function. Behavior as described for SBCU_DBGNTT.ONE0.

BROM_TC.H003 Information related to Register FLASH0_PROCOND

Chapters “TC2x BootROM Content” of the User’s Manuals contain a description of parts of the FLASH0_PROCOND register as used by the firmware. This description in subchapter “Configuration by Boot Mode Index (BMI)” shows an incorrect address F800 1030_H.

Correct is the description of this register in the PMU chapter with address F800 2030_H (FLASH0 base address F800 1000_H + offset 1030_H).

CCU6_AI.H001 Update of Register MCMOUT

At every correct Hall event (CM_CHE), the next Hall patterns are transferred from the shadow register MCMOUTS into MCMOUT (Hall pattern shadow transfer HP_ST), and a new Hall pattern with its corresponding output pattern can be loaded (e.g. from a predefined table in memory) by software into MCMOUTS. For the Modulation patterns, signal MCM_ST is used to trigger the transfer.

Loading this register can also be done by writing MCMOUTS.STRHP = 1_B (for EXPH and CURH) or MCMOUTS.STRMCMP = 1_B (for MCMP).

Note: If in a corner case a hardware event occurs simultaneously with a software write where MCMOUTS.STRHP = 1_B or MCMOUTS.STRMCMP = 1_B, the current contents of MCMOUTS is copied to the corresponding bit fields of MCMOUT. The new value written to MCMOUTS will be loaded upon the next event.

CCU6_AI.H002 Description of Bit RWHE in Register ISR

Register ISR (Interrupt Status Reset Register) contains bits to individually clear the interrupt event flags by software. Writing a 1_B clears the bit(s) in register IS at the corresponding bit position(s), writing a 0_B has no effect.

In some versions of the User's Manual, the description of bit RWHE (Reset Wrong Hall Event Flag) in column "Description" of register ISR is wrong (description for status 0_B and 1_B inverted).

The correct description for bit RWHE is (like for all other implemented bits in register ISR) as shown in the following **Table 17**:

Table 17 Bit RWHE in register ISR

Field	Bits	Type	Description
RWHE	13	w	**Reset Wrong Hall Event Flag** 0_B No action 1_B Bit WHE will be cleared

CCU6_AI.H003 Bit TRPCTR.TRPM2 in Manual Mode - Documentation Update

In CCU6 chapter “Trap Control Register” of the User’s Manual, the description for bit TRPCTR.TRPM2 = 1_B (Manual Mode) incorrectly states:

“Manual Mode:
Bit TRPF stays **0** after the trap input condition is no longer valid. It has to be cleared by SW by writing ISR.RTRPF = 1.”

Correction

The correct description is as follows:

Manual Mode:
Bit TRPF stays **1** after the trap input condition is no longer valid. It has to be cleared by SW by writing ISR.RTRPF = 1.

CCU_TC.H001 Clock Monitor Check Limit Values

The values for the check limits of the clock monitor have been updated as shown in **Table 18**. This table replaces the corresponding table in chapter “Clock Monitors” of the User’s Manual.

Table 18 Target trimmed Check limits

Target Frequency	LOWER value	UPPER value	SELXXX [1]	Error can be detected for min. deviation	Error is detected for min. deviation
7.5 MHz	0x23	0x27	11_B	-4.07% +1.54%	-9.40% +6.35%
$6.\overline{6}$ MHz	0x1F	0x23	10_B	-4.07% +2.75%	-9.40% +7.50%
6 MHz	0x1C	0x1F	01_B	-3.35% +1.54%	-8.43% +6.35%
5 MHz	0x17	0x1A	00_B	-2.76% +4.07%	-9.41% +7.50%

1) refers to corresponding bit field xxxSEL in respective CCUCON register

CCU_TC.H002 Oscillator Gain Selection via OSCCON.GAINSEL

The reset value of OSCCON.GAINSEL = 11_B provides the default and recommended setting for the oscillator gain. It is not required to modify this value, as the adaptation to a crystal frequency is done via the external circuitry.

Therefore, all other gain selections should be regarded as reserved for special application topics, as shown in the following **Table 19**.

Table 19 Oscillator Gain Selection via OSCCON.GAINSEL

Field	Bits	Type	Description
GAINSEL	[4:3]	rw	**Oscillator Gain Selection** This value should not be changed from the reset value 11_B. 00_B Low gain 1: reserved for adaptations 01_B Low gain 2: reserved for adaptations 10_B Low gain 3: reserved for adaptations 11_B **Maximum gain: default setting**

Recommendation

Always to keep the default configuration of OSCCON.GAINSEL = 11_B.

CCU_TC.H005 References to f_{PLL2}, f_{PLL2_ERAY} and K3 Divider in User's Manual

The VADC incorporated in this device uses clocks derived from f_{SPB}.

Previous design steps (e.g. TC27x Bx, TC26x Ax, TC29x Ax) incorporated a different VADC module also clocked by f_{ADC}, which could be derived via the K3 divider from f_{PLL2}, f_{PLL2_ERAY}. These clocks were selected in CCUCON0.[27:26], which is described as "Reserved/Should be written with 0" in the present version of the User's Manual.

Clocks f_{PLL2}, f_{PLL2_ERAY} and the K3 divider are still described in the present version of the User's Manual.

Recommendation

- New software implementations should not consider f_{PLL2}, f_{PLL2_ERAY} and the K3 divider.
- Software ported from previous design steps with a VADC module clocked by f_{ADC} may be reused on this device step.

CCU_TC.H006 Clock Monitor Support - Documentation Update

The note at the end of section "Operating the Clock Monitors" in chapter "Clock Monitors":

Note: This feature is supported by the Infineon safety driver [safTlib] and there is no additional customer software required.

should state more precisely:

Note: The Infineon SafeTlib provides a test for the clock monitor. The clock monitor shall be configured by the application software.

CCU_TC.H007 Oscillator Watchdog Trigger Conditions for ALM3[0]

As described in the User's Manual in section "Oscillator Watchdog", the divider value OSCCON.OSCVAL has to be selected in a way that f_{OSCREF} is within the range of 2 MHz to 3 MHz, and should be as close as possible to 2.5 MHz.

The Oscillator Watchdog (OSC_WDT) will trigger the "input clock out of range" alarm ALM3[0] under the following conditions:

- Boundary for **too high** frequencies:
  - for (OSCVAL+1) x 6.25 ≤ f_{OSC} [MHz] ≤ (OSCVAL+1) x 7.5, an alarm can be generated, but there is no guarantee that it is generated,
  - for f_{OSC} [MHz] > (OSCVAL+1) x 7.5, an alarm is always generated.
- Boundary **for too** low frequencies:
  - for (OSCVAL+1) x 1.25 ≤ f_{OSC} [MHz] ≤ (OSCVAL+1) x 1.67, an alarm can be generated, but there is no guarantee that it is generated,

– for f_{OSC} [MHz] <(OSCVAL+1) x 1.25, an alarm is always generated.

The accuracy of these limits [in %] depends on the variation [in %] of the back up clock (see specification of f_{BACKUT} and f_{BACKT} in the Data Sheet).

Example

- For f_{OSC} = 20 MHz, selecting OSCVAL = 7 results in f_{OSC} = 2.5 MHz.
  – An alarm for too high frequencies can be generated for $f_{OSC} \geq$ 50 MHz,
  – An alarm for too high frequencies is always generated for f_{OSC} > 60 MHz.
  – An alarm for too low frequencies can be generated for $f_{OSC} \leq$ 13.36 MHz,
  – An alarm for too low frequencies is always generated for f_{OSC} < 10 MHz.

CPU_TC.H006 Store Buffering in TC1.6/P/E Processors

Overview

Store buffering is a method of increasing processor performance by decoupling memory write operations from the instruction execution flow within the CPU. All write data is placed in a FIFO buffer (known as the store buffer) by the CPU prior to being read by the memory/bus interfaces and written to memory. This allows the processor to continue execution without waiting for the write data to be written to the target memory location. Data is written to the store buffer at processor speed and read from the store buffer at memory/bus speed. Typically the read bandwidth from the store buffer will exceed the write bandwidth from the processor, only if the store buffer fills will the processor stall.

To further increase performance memory read operations are prioritised ahead of memory write operations from the store buffer. This ensures that the processor does not stall on data loads while data writes are pending in the store buffer. A side effect of this prioritising is that memory may not be accessed in program order.

Operational Details

The function of the store buffer is designed to be invisible to the end user under normal operation:

- All CPU load operations are checked against the store buffer contents. Data for matching load addresses is either immediately forwarded to the CPU from the store buffer (TC1.6, TC1.6P) or written to memory prior to the load operation proceeding (TC1.6E).
- All loads and store operations to peripheral regions (typically segments E_H and F_H) are performed in strict program order (no load prioritisation).

The operation of the store buffer can become visible when in-order memory access is required to non-peripheral segments.

This can occur under the following circumstances:

- When programming flash memory.
- When performing memory testing with the processor.
- When data is required to be in memory for inter-core/inter-module communication.

In such cases the following solutions may be employed:

- The store buffer may be explicitly flushed by use of a DSYNC instruction.
- The store buffer may be disabled by setting `SMACON.IODT`. This should not be done during normal operation as it significantly impacts performance.

Examples

The following examples refer to memory accesses to non-peripheral regions (i.e. segments 0_H .. D_H):

Example-1a Out of order memory access due to load prioritisation

```
Program Flow     -     Memory Access
 st-1                    ld-4
 st-2                    ld-5
 st-3                    ld-6
 ld-4                    st-1
 ld-5                    st-2
 ld-6                    st-3
```

Example-1b In order memory access enforced by DSYNC

```
Program Flow     -     Memory Access
```

```
 st-1                  st-1
 st-2                  st-2
 st-3                  st-3
 dsync
 ld-4                  ld-4
 ld-5                  ld-5
 ld-6                  ld-6
```

Example-2a Load forwarding from store buffer - no memory read (TC1.6/1.6P)

```
Program Flow     -    Memory Access
 st.w [a0], d0
 ld.w d1,  [a0]        st.w [a0], d0
```

Example-2b In order memory access enforced by DSYNC (TC1.6/1.6P)

```
Program Flow     -    Memory Access
 st.w [a0], d0         st.w [a0], d0
 dsync
 ld.w d1,  [a0]        ld.w d1,  [a0]
```

CPU_TC.H008 Instruction Memory Range Limitations

To ensure the processor cores are provided with a constant stream of instructions the Instruction Fetch Units will speculatively fetch instructions from up to 64 bytes ahead of the current Program Counter (PC).

If the current PC is within 64 bytes of the top of an instruction memory the Instruction Fetch Unit may attempt to speculatively fetch instructions from beyond the physical range. This may then lead to error conditions and alarms being triggered by the bus and memory systems.

Recommendation

It is therefore recommended that either the MPU is used to define the allowable executable range or that the upper 64 bytes of any memory be initialized but unused for instruction storage for the TC1.6.* class processors. For TC1.3.* class processors this may be reduced to 32 bytes.

CPU_TC.H009 Details on CPU Clock Control

As described in chapter “Clock Control Unit” of the User’s Manual, the effective CPU execution frequency may be reduced by programming the associated bit field CPUxDIV in register CCUCONn (where x is the core number, and n = x+6).

The effective execution frequency f_{CPUx} seen by CPUx is given by the following equation (where f_{SRI} is the base SRI frequency):

- $f_{CPUx} = f_{SRI} * (64 - CPUxDIV) / 64$

A CPUxDIV value of 0 results in the core CPUx being clocked at the SRI frequency (no frequency reduction).

To avoid synchronisation issues typically associated with clock division the clock control mechanism stalls the issue of instructions into the processor pipeline rather than by modifying the actual applied clock. An incoming instruction fetch packet is stalled for the number of cycles required to approximate the required execution frequency. The stall is seen by the processor as a stall in the instruction stream in the same way a stalling instruction memory would be seen.

In most scenarios this mechanism provides a good approximation to clock division based control. The actual reduction in effective frequency will be dependent on the code executed.

When determining IPC rates as described in AP32168 (Application Performance Optimization for TriCore V1.6 Architecture), note that for CPUxDIV > 0, field Count Value in register CCNT still represents SRI clock cycles.

CPU_TC.H012 Behavior of bit-wise operations on certain peripheral register bits which need to be written back with the same value

The LDMST, ST.T, CMPSWAP.W, SWAPMSK.W and SWAP.W instructions in the AURIX™ microcontrollers are instructions intended to provide atomicity as well as bit-wise operations to a targeted memory location or peripheral register. They are also referred to as Read-Modify-Write (RMW) instructions.

In some registers in certain modules, a bit has to be written with the same value (e.g. a bit set to 1_B has to be written with a 1_B to perform an operation).

When using a RMW instruction to write to such a bit, the write is masked away and will not happen at all.

Note: Writing a different value (e.g. writing a 1_B to a bit currently at 0_B) is not affected, and works as expected to modify only the selected bit.

Example: Consider the GxVFR register in the VADC module:

GxVFR (x = 0 - 10)
Valid Flag Register, Group x (x * 0400_H + $05F8_H$) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VF15	VF14	VF13	VF12	VF11	VF10	VF9	VF8	VF7	VF6	VF5	VF4	VF3	VF2	VF1	VF0
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
VFy (y = 0 - 15)	y	rwh	**Valid Flag of Result Register x** Indicates a new result in bitfield RESULT or in bit FCR. 0_B Read access: No new valid data available Write access: No effect 1_B Read access: Result register x contains valid data and has not yet been read, or bit FCR has been updated Write access: Clear this valid flag and bitfield DRC in register GxRESy (overrides a hardware set action)

Figure 7 Register GxVFR in the VADC Module of TC2xx Devices

The bits in the GxVFR register have to be written with 1_B to clear a valid flag VFy indicating a valid result. Assuming VFy = 1_B, if one of the RMW instructions listed above is used, the write to VFy would never happen since VFy is already set to 1_B. This means that the next read of VFy may lead to incorrect conclusions by software.

Affected Modules and Registers in the AURIX™ Platform

- CCU6: IMON
- VADC: GxVFR, GxSEFLAG, GxCEFLAG, GxREFLAG, GLOBEFLAG.

Note: VADC is located outside the addressable range of ST.T, so ST.T need not be considered in the context of VADC.

Recommendation

In the affected modules, use only direct writes (i.e, write the whole register as a 32-bit word), and do not use RMW operations to write to such bits.

For example, to clear bit VF0 in the GxVFR register, the software should write:

```
VADC_GxVFR.U = 0x00000001;
```

Here .U implies writing the whole 32-bit register as an unsigned integer.

CPU_TC.H014 ACCEN* Protection for Write Access to Safety Protection Registers - Documentation Update

The access protection symbol ‘P’ to indicate protection by the ACCEN* register mechanism is missing in column “Access Mode - Write” in table “Safety Protection Registers” in the CPU chapter of the User’s Manual for RGN*x registers with an index x ≥4.

Actually, these registers also have write access attribute ‘P’.

CPU_TC.H015 Register Access Modes for Safety Protection Registers - Documentation Update

The access protection symbol ‘U’ is erroneously included and should be removed in column “Access Mode - Write” for all registers in table “Safety Protection Registers” in the CPU chapter of the User’s Manual.

The note below this table is rephrased as follows:

Note: A disallowed access to any CPU register (e.g. attempted write to non-existent register, attempted write to read only register, attempted access to E without Endinit, etc.) will NOT result in a Bus Error

DAP_TC.H002 DAP client_blockread in Combination with TGIP and all Parcels with CRC6

Note: This problem is only relevant for tool development, not for application development.

When issuing a DAP client_blockread telegram together with the TGIP (Trigger in Protocol) option (DAPISC.TGIP = 1) the TGIP extra bit is appended for each parcel in case “all parcels with CRC6” is enabled. This causes a slight increase in the communication length compared to the correct behavior of having a TGIP bit only for the last parcel.

Recommendation

Do not use the TGIP and “CRC6 for all parcels” features together in case this extra bit can not be tolerated. If the Trigger in Protocol and increased communication safety is required TGIP can be used together with the CRC32 option (see also DAP_TC.002 DAP client_blockread has Performance issue in Specific Operation Modes).

DAP_TC.H003 Not acknowledged DAP telegrams in noisy environments

Note: This problem is only relevant for tool development, not for application development.

DAP telegrams always follow a request-reply scheme. The request is driven by the tool, the reply by the AURIX™. The AURIX™ acknowledges a correctly received telegram always by a reply, which consists at least of a start-bit. DAP communication in noisy environments might result in invalid telegrams. This can leave the IOClient in an intermediate state which requires an IOClient reset.

If AURIX™ receives an invalid telegram with a wrong CRC6 or length field, it does not reply at all and in some cases the selected IOClient might be left in an intermediate state in case of a detected client_write/blockwrite/readwrite tool request.

Recommendation

If a tool does not receive a start bit as an acknowledge for an IOClient request, a client_reset must be sent as the next telegram for the selected IOClient. Tool interaction with the DAP module itself is not affected and can be done in between.

DMA_TC.H002 Bit CHCSRz.BUFFER can be toggled when not in Double Buffer Mode

The purpose of bit CHCSRz.BUFFER is to indicate which buffer is read or filled during DMA double buffering (selected in bitfield ADICRz.SHCT).

However, bit CHCSRz.BUFFER can also be toggled by writing bit CHCSRz.SWB = 1_B when not in Double Buffer Mode.

Recommendation

Do not write bit CHCSRz.SWB = 1_B when not in Double Buffer Mode.

DMA_TC.H004 Transaction Request Lost upon software trigger with pattern match

If a DMA channel is configured for pattern detection and software triggering of each DMA transfer (CHCSRz.RROAT = 0_B), then if there is a new DMA software request received while a DMA transfer is executing then a Transaction Request Lost event may be lost.

Recommendation

The loss of TRL status is a debug feature. A DMA channel should be used such that TRL is not set.

The user must ensure that the CPU triggers a new DMA software request when no DMA access is pending.The software could poll the TSRz.CH bit to confirm it is 0_B before issuing a DMA software trigger.

DMA_TC.H005 Linked List Transfer leading to loading of non-Linked List TCS causes corruption

If on completion of a Linked List (LL) a non-LL Transaction Control Set (TCS) is loaded with shadow address buffering enabled (read only and direct write) then the new non-LL TCS can be corrupted.

Recommendation

Shadow address buffering must be disabled in the non-LL TCS (SHCT[3:0] = 0000_B)

DMA_TC.H006 Clearing of HTRE when DMA channel is configured for Single Mode

The DMA may be used to support a peripheral with a high interrupt rate where the interrupts are generated in quick succession (e.g. a QSPI filling a TXFIFO).

The DMA channel z is configured with the following settings:

- Single Mode (HTRE is reset by hardware on completion of a DMA transaction)
  - TSRz.CHMODE = 0_B
- Request required for each DMA Transfer
  - TSRz.RROAT = 0_B

If the DMA channel is configured to execute a DMA transaction of 1 x DMA transfer of 2 x DMA moves:

- Block Mode: 2 x DMA Move per DMA transfer
  - DMA_CHCFGRz.BLKM = 001_B
- Transfer Reload Value: 1 x DMA transfer
  - DMA_CHCFGRz.TREL = 1_B

then additional DMA moves are executed unexpectedly.

Explanation of Effect

If the peripheral generates two interrupt service requests in relatively quick succession then the first DMA hardware request is serviced by the DMA and performs one DMA transfer comprising two DMA moves. The second DMA hardware request arrives before the completion of the first DMA transfer (i.e. before the clearing of HTRE at the end of the DMA transaction). The second hardware request is serviced by the DMA and performs a second DMA transfer comprising two DMA moves.

Recommendation

If the second DMA hardware request arrives before completion of the first DMA transfer then the DMA channel Block Mode must limit a DMA transfer to one DMA move:

- DMA_CHCFGRz.BLKM = 000_B; //1 x DMA move/DMA transfer

The total number of DMA moves must be defined by the Transfer Reload Value DMA_CHCFGRz.TREL.

DMA_TC.H007 Selecting the Priority for DMA Channels

All used DMA channels should be configured with the **highest** priority on SPB in respect to other used SPB master agents (CPUs, HSSL, ETH) to enable a robust execution of the configured DMA transactions.

The DMA channels are configured per default with the lowest priority on SPB:

- DMA_CHCFGRz.DMAPRIO = 00_B --> maps DMA channel z SPB requests to SPB priority DMAL
- SBCU_PRIOH.DMAL = 1111_B --> configures DMAL with the lowest priority on SPB

Recommendation

There are several ways to configure used DMA channels with the highest priority on SPB with respect to other SPB master agents. Two examples follow:

Example1

Map the used DMA channels to SPB priority DMAH by setting DMA_CHCFGRz.DMAPRIO = 11_B and keep the configuration of the DMAH priority (SBCU_PRIOL.DMAH = 0000_B).

Example2

Keep the mapping of the used DMA channels to DMAL (DMA_CHCFGRz.DMAPRIO = 00_B) and change the priority configuration of DMAL (e.g. set SBCU_PRIOH.DMAL = 0001_B).

Background

The DMA can request for SPB access with three different requests (DMAH, DMAM, DMAL) that are configured with different SPB priorities with respect to the other SPB master agents (CPUx, HSCT, ETH). The priority of the DMA requests DMAH, DMAM and DMAL on the SPB in respect to the priority of other SPB master agents can be configured via the SBCU registers SBCU_PRIOL / SBCU_PRIOH.

Each DMA channel z can be configured via DMA_CHCFGRz.DMAPRIO regarding which of three priorities (DMAH, DMAM or DMAL) it uses for SPB access.

The default configuration of DMA_CHCFGRz.DMAPRIO = 00_B. This means that the channels will request for SPB access with the DMAL priority.

The priority of a DMAL request on SPB is configured per default with the lowest priority (SBCU_PRIOH.DMAL = 1111_B).

DMA_TC.H008 Transaction Request State

The DMA Transaction Request State bit DMA_TSRz.CH is cleared when the DMA transfer starts (RROAT = 0_B) or at the end of a DMA transaction (RROAT = 1_B).

Figure “Channel Request Control” and RROAT bit field description of register DMA_MExCHCR in chapter “Register Description” of the User’s Manual are wrong.

DMA_TC.H009 Resetting Bits ICH and IPM in register CHCSRz

The Clear Interrupt from Channel bit (CICH) is accessible via the DMA channel CHCSR register.

The AURIX™ TC2xx User Manuals are incorrect with respect to the following statement:

- The DMA channel DMA_CHCSRz ICH and IPM bit field description states: “is reset by software when writing a 1 to ADICRz.CICH”.

Correction

- The text should read:
  “is reset by software when writing a 1 to **CHCSRz**.CICH”.

DMA_TC.H010 Calculation of DMA Address Checksum for DMA read moves to Cacheable Addresses

The DMA Move Engine (ME) stores the DMA read move data in eight 32-bit read registers. If a DMA read move is to a cached address (Segment 8 or 9), the ME shall translate the DMA read move access to the on chip bus into an SRI BTR4 access to a 32-byte aligned address. The DMA shall calculate the DMA address checksum from the on chip bus address i.e. the 32-byte aligned address. The DMA shall store the DMA address checksum in the SDCRCR.

Recommendation

If an expected DMA address checksum is pre-calculated to test the DMA address generation, the user shall take note of the address translation to 32-byte aligned addresses when calculating the expected DMA address checksum from a cacheable DMA source address.

Alternatively, DMA read moves should be performed to non-cacheable source addresses (segments A and B).

DMA_TC.H011 DMA_ADICRz.SHCT - Reserved Values

The DMA channel shadow control bit field DMA_ADICRz.SHCT controls the function of the shadow address register. If software programs a reserved value in DMA_ADICRz.SHCT, the DMA may deadlock the operation of the DMA.

Therefore, software shall not program DMA_ADICRz.SHCT with the following reserved values:

- 0011_B Reserved
- 0100_B Reserved
- 0111_B Reserved.

DMA_TC.H012 TCS Update in Halt State

If a DMA channel is in halt state,

- The DMA shall stop performing DMA moves to the destination location.
- Software may perform a background test on the destination location.
- Software may modify the DMA channel Transaction Control Set (TCS).

Recommendation

If software modifies the DMA channel TCS, software shall only modify the DMA channel source address (DMA_SADRz.SDAR) and the DMA channel destination address (DMA_DADRz.DADR).

DMA_TC.H013 MExSR.WS and MExSR.RS Status Bits

As documented in the User's Manual, the Move Engine (ME) status bits RS/WS in register MExSR are set when the ME is performing a read move or DMA write move. This means:

- MExSR.RS = 1_B when the ME is performing a DMA read move for the active DMA channel.
- MExSR.WS = 1_B when the ME is performing a DMA write move for the active DMA channel.

It should be noted that the setting of these bits is not restricted to DMA read move and DMA write move. Additionally the status bits may be set when the ME is performing other operations:

- MExSR.RS = 1_B when the ME is loading a new Transaction Control Set in a linked list.
- MExSR.WS = 1_B when the ME is writing a DMA timestamp.

Note: The additional setting of the ME status bits may be observed when debugging the operation of the DMA. There is no effect on the operation of the DMA.

DMA_TC.H016 DMARAM ECC Error Disable

If software disables SPB bus errors caused by DMARAM ECC errors (DMA_MEMCON.ERRDIS = 1_B), the DMA will not correctly acknowledge a Read Modify Write (RMW) access on the SPB bus.

Recommendation

The application software must always enable the reporting of SPB errors (DMA_MEMCON.ERRDIS = 0_B; default after reset).

DMA_TC.H017 DMA Channel Request Control - Documentation Update

The following text (located below figure “Channel Request Control” in section “DMA Channel Request Control” of the DMA chapter in the User’s Manual):

“If CHCFGRz.PRSEL = 1 in the current DMA channel z can bypass the ICU and trigger a DMA hardware request in the next lower DMA channel z-1. The latency to service a DMA channel z-1 request is reduced. DMA channel z interrupt service requests are disabled.”

should read as:

“If DMA_CHCFGRz.PRSEL = 1 **is selected** in the current DMA channel z, **a DMA channel trigger** can bypass the ICU and trigger a DMA hardware request in the next lower DMA channel z-1. The latency to service a DMA channel z-1 request is reduced. DMA channel z interrupt service requests are disabled.”

DTS_TC.H001 Update of Bit DTSSTAT.BUSY

The following statement in the description of bit BUSY in register DTSSTAT in the SCU chapter “Die Temperature Measurement” is incorrect:

Note: This bit is updated 2 cycles after bit DTSCON.START is set.

Correction

The correct description is as follows:

*Note: This bit is updated **7** cycles after bit DTSCON.START is set.*

ENDINIT_TC.H001 Endinit Protection for Registers KRST0, KRST1, KRSTCLR

The access protection symbol ‘E’ to indicate Endinit-protection is missing in column “Access Mode - Write” in table “Register Overview” in the User’s Manual for the following registers:

- KRST0, KRST1, KRSTCLR

of the following modules (if implemented):

- E-Ray, ETH, PSI5.

FLASH_TC.H007 Advice for using Suspend and Resume

As documented in the User’s Manual section “Operation Suspend and Resume”, an operation is suspended by writing ‘1’ to MARD.SPND. The Flash operation stops when it reaches an interruptible state. After that the flag FSR.SPND is set and BUSY is cleared.

The 1-to-0 transition of MARD.SPND alone is not indicating if the suspend request has been executed and the Flash can accept a new command. The BUSY flags have to be checked to determine if the Flash is still busy with the current operation. Only after the 1-to-0 transition of the BUSY flags the flag FSR.SPND indicates if the operation has finished or if it is in suspended state.

The following recipe describes the best practice for using suspend and resume.

Suspending an Erase Operation

In case of a request for suspending an ongoing erase operation:

As documented in the User's Manual: Please ensure that between start or resume of an erase process and the suspend request normally at least ~1 ms erase time can pass.

- Check if the corresponding BUSY flag has already cleared. If yes, no suspend is necessary.
- Request the suspend with control flag MARD.SPND = 1_B.
- Wait until the BUSY flag clears.

- After that check FSR.SPND. If this is 1_B then the operation was suspended and needs to be resumed later. If this is 0_B the operation has already finished, therefore no resume is necessary.
- Now new Flash operations are allowed with the restrictions documented in User's Manual section “Operation Suspend and Resume”.

Note for PFlash erase operations in bank x that PxBUSY and D0BUSY are set at the beginning. The D0BUSY is cleared early after updating the Erase Counters, and PxBUSY is cleared when the erase operation has finished. Therefore, for PFlash the PxBUSY flag has to be used. (Polling for PxBUSY and DxBUSY can be a generic solution for suspend sequences before checking the SPND state.) Interrupt driven software receives two interrupts!

Resuming a Suspended Erase Operation

The resume of the suspended erase operation is done in these steps:

- Resume the operation with the command sequence “Resume Prog/Erase”.
- Wait until FSR.SPND is 0_B.
- After that wait for the end of the operation signalled by BUSY going to 0_B.

Suspending a Program Operation

In case of a request for suspending an ongoing programming operation:

- Request the suspend with control flag MARD.SPND = 1_B.
- Wait until the BUSY flag clears.
- After that check FSR.SPND. If this is 1_B then the operation was suspended and needs to be resumed later. If this is 0_B the operation has already finished, therefore no resume is necessary.
- Now new Flash operations are allowed with the restrictions documented in User's Manual section “Operation Suspend and Resume”.

Resuming a Suspended Program Operation

The resume of the suspended programming operation is done in these steps:

- Resume the operation with the command sequence “Resume Prog/Erase”.
- Wait until FSR.SPND is 0_B.
- After that wait for the end of the operation signalled by BUSY going to 0_B.

FLASH_TC.H008 Understanding Flash Retention/Endurance Figures in the Data Sheet

Flash retention/endurance is documented in the Data Sheet by the following parameters

- Program Flash Retention Time t_{RET} for PFlash,
- UCB Retention Time t_{RTU} for the UCBs,
- Data Flash Endurance per EEPROMx sector N_{E_EEP10} for DFlash0,
- Data Flash Endurance per HSMx sector N_{E_HSM} for DFlash1 (if available).

Retention

To emphasize the importance of retention, the PFlash and UCB parameters are described as retention time under the condition of a maximum number of cycles.

The value “Min. x years” has to be interpreted as: the data retention is at least x years, i.e. x years or longer after the last programming data stays readable.

The condition “Max. y erase/program cycles” means: this data retention figure is valid if there were not more than y erase/program cycles.

Endurance

For the DFlash the endurance is most important, therefore as parameter the number of cycles under the condition of the retention is given.

The value “Min. x cycles” has to be interpreted as: at least x cycles can be applied.

The condition “Max. data retention time y years” means: this endurance figure is valid if the expected data retention after the last programming is maximum y years.

Note: As general remark, these figures are only valid if the parameters given in the Data Sheet are adhered to in their entirety.

FlexRay_AI.H004 Only the first message can be received in External Loop Back mode

If the loop back (TXD to RXD) will be performed via external physical transceiver, there will be a large delay between TXD and RXD.

A delay of two sample clock periods can be tolerated from TXD to RXD due to a majority voting filter operation on the sampled RXD.

Only the first message can be received, due to this delay.

To avoid that only the first message can be received, a start condition of another message (idle and sampling '0' -> low pulse) must be performed.

The following procedure can be applied at one or both channels:

- wait for no activity (TEST1.AOx=0 -> bus idle)
- set Test Multiplexer Control to I/O Test Mode (TEST1.TMC=2), simultaneously TXDx=TXENx=0
- wait for activity (TEST1.AOx=1 -> bus not idle)
- set Test Multiplexer Control back to Normal signal path (TEST1.TMC=0)
- wait for no activity (TEST1.AOx=0 -> bus idle)

Now the next transmission can be requested.

FlexRay_AI.H005 Initialization of internal RAMs requires one eray_bclk cycle more

The initialization of the E-Ray internal RAMs as started after hardware reset or by CHI command CLEAR_RAMS (SUCC1.CMD[3:0] = 1100_B) takes 2049 eray_bclk cycles instead of 2048 eray_bclk cycles as described in the E-Ray Specification.

Signalling of the end of the RAM initialization sequence by transition of MHDS.CRAM from 1_B to 0_B is correct.

FlexRay_AI.H006 Transmission in ATM/Loopback mode

When operating the E-Ray in ATM/Loopback mode there should be only one transmission active at the same time. Requesting two or more transmissions in parallel is not allowed.

To avoid problems, a new transmission request should only be issued when the previously requested transmission has finished. This can be done by checking registers TXRQ1/2/3/4 for pending transmission requests.

FlexRay_AI.H007 Reporting of coding errors via TEST1.CERA/B

When the protocol engine receives a frame that contains a frame CRC error as well as an FES decoding error, it will report the FES decoding error instead of the CRC error, which should have precedence according to the non-clocked SDL description.

This behaviour does not violate the FlexRay protocol conformance. It has to be considered only when TEST1.CERA/B is evaluated by a bus analysis tool.

FlexRay_AI.H009 Return from test mode operation

The E-Ray FlexRay IP-module offers several test mode options

- Asynchronous Transmit Mode
- Loop Back Mode
- RAM Test Mode
- I/O Test Mode

To return from test mode operation to regular FlexRay operation we strongly recommend to apply a hardware reset via input eray_reset to reset all E-Ray internal state machines to their initial state.

Note: The E-Ray test modes are mainly intended to support device testing or FlexRay bus analyzing. Switching between test modes and regular operation is not recommended.

FlexRay_TC.H002 Initialization of E-Ray RAMs

After Power-on reset the ECC codes in the E-Ray RAMs may be set to an arbitrary state. Therefore the E-Ray RAM must be cleared and the ECC codes set to a defined state to avoid unintended traps.

To achieve this the following alternative methods are proposed:

Method 1 using the MTU/MBIST:

- Clear all E-Ray RAMs and the related ECC code storage by executing writes to all RAM locations using the AURIX MBIST engine.
  The MBIST engine supports filling the E-Ray RAM with ECC-correct patterns. For this purpose the AURIX MBIST auto-initialization algorithm can be used. See section “Filling a Memory with Defined Contents” in the corresponding User’s Manual/Target Specification.
  The following E-Ray RAM blocks have to be initialized with correct data:
  – Output Buffer
  – Input Buffer
  – Message Buffers
    The MBIST function to be executed for each buffer is the same, only the function parameters have to be adapted.
- Execute one read from each E-Ray RAM block using the AURIX MBIST engine (reading from all E-Ray RAM locations is an alternative but not necessary solution). For this purpose the AURIX MBIST engine can also be used.
- Insert at the end of all MBIST function calls a status check, which makes sure that the launched MBIST tests are finished (check MSTATUS.DONE status flag).
- Clear all ECC error flags in the E-Ray module: these are flag EERR in register EIR, flags EIBF, EOBF, EMR, ETBF1, ETBF2 in register MHDS. The flags are cleared by writing a ‘1’ to the according bit position in the flag register.

After these steps the E-Ray RAM can be used for further operation, for example for initialization of the E-Ray buffer.

Method 2 using “CLEAR RAMS” Command:

Step 1 to 4: Enable the clock of the module:

- 1. Remove EINIT protection for the writing of the CLC register.
- 2. Enable the clock in the CLC register.
- 3. Read the CLC register.
- 4. Enable the EINIT protection.

Enable the test mode, check if the state of the module is according to the expected settings and start clearing the RAMs.

- 5. Take care of the unlock sequence. See description of LCK.TMK and TEST1.WRTEN in User’s Manual:
  - Test Mode Key: To set bit TEST1.WRTEN the write operation has to be directly preceded by two consecutive write accesses to the Test Mode Key.
  - If the write sequence is interrupted by other write accesses between the second write to the Test Mode Key and the write access to the TEST1 register, bit TEST1.WRTEN is not set to 1 and the sequence has to be repeated.
    First write: LCK.TMK = 75_H = 0111 0101_B
    Second write: LCK.TMK = $8A_H$ = 1000 1010_B
    Second write: TEST1.WRTEN = 1_B
- 6. Check if CCSV.POCS is either 0x0 (DEFAULT_CONFIG) or 0xF (CONFIG). If not in any of these states, perform the according command to get to CONFIG state.
- 7. Check if SUCC1.PBSY is equal 0x0. If 0x1 wait until 0x0.
- 8. Set SUCC1.CMD to 0xC meaning that the CLEAR_RAMS command is entered.
- 9. Read SUCC1.CMD. If 0x0 the command has not been accepted. Repeat up from step 7. Otherwise continue.
- 10. Wait 1024 module cycles.
- 11. Enable RAM Test mode: TEST1.TMC = 01_B. This mode enables access of all RAM blocks in E-Ray modules to the host.
- 12. CUST1.IBF1PAG := 1_B
- 13. CUST1.IBF2PAG := 1_B.
- 14. Repeat steps 7 to 10.
- 15. Read at least one address in all the RAM blocks within E-Ray module.

- 16. Switch off Test mode: TEST1.WRTEN = 0_B
- 17. Clear ECC error flags in MHDS and EIR registers
- 18. From here you can start the normal initialization process of the module.

FPI_TC.H002 Write Access to Register ACCEN1

The ACCEN1 (Access Enable Register 1) registers in the AURIX™ devices are reserved for future expansion. The bits in the ACCEN1 registers are described as “Reserved”, read-only. There is no need for software to configure (write to) the ACCEN1 registers.

Note: For a write access to the ACCEN1 registers in the following modules, a bus error will be generated: MTU, SMU, ETH, I2C, FFT, CIF.

GPT12_TC.H001 Timer T5 Run Bit T5R - Documentation Correction

In the current version of the User’s Manual, the lines for T5R=0_B and T5R=1_B in the register description of the Timer T5 Run Bit (T5R) erroneously have been swapped.

Correction

The correct behavior of bit T5R is as shown in **Table 20**: T5R=0_B (Timer T5 stops; default after reset), T5R=1_B (Timer T5 runs).

Table 20 Timer T5 Control Register T5CON, Bit T5R - Correction

Field	Bits	Type	Description
T5R	6	rw	**Timer T5 Run Bit** 0_B Timer T5 **stops** 1_B Timer T5 **runs** *Note: This bit only controls timer T5 if bit T5RC = 0.*

GTM_TC.H004 Correction to Bit Fields GTM_TIMi_IN_SRC.VAL_x

In the description of bit field VAL_0 in register GTM_TIMi_IN_SRC in the User's Manual, the encoding 01_B was erroneously repeated while 10_B and 11_B were missing.

The correct description is included in the following **Table 21**. As the description of bit fields VAL_x, x>0 refers to VAL_0, this description is valid for all VAL_x bit fields in register GTM_TIM0_IN_SRC.

Table 21 Corrected Description of Bit Field VAL_0 in Register GTM_TIM0_IN_SRC

Field	Bits	Type	Description
VAL_0	[1:0]	rw	**Value to be fed to Channel 0** 00_B Input signal 0 (ignore write access) 01_B Input signal is set to 0 10_B Input signal is set to 1 11_B Input signal 1 (ignore write access) ...

GTM_TC.H005 External Capture in TIM Pulse Integration Mode (TPIM)

In table "TIM integration Mode" in section "External Capture in TIM Pulse Integration Mode (TPIM)" of the GTM chapter in the User's Manual, the information that CNT is cleared upon external capture is missing in column "Action description".

The corrected **Table 22** is shown below:

Table 22 TIM integration Mode

Input signal F_OUTx	selected CMU clock	External capture	ISL	DSL	Action description
0	1	0	-	0	CNT++
1	1	0	-	0	no
1	1	0	-	1	CNT++

Table 22 TIM integration Mode (cont'd)

Input signal F_OUTx	selected CMU clock	External capture	ISL	DSL	Action description
0	1	0	-	1	no
-	-	rising edge	-	-	do GPRx capture; issue NEWVAL_IRQ; **CNT = 0**
-	0	0	-	-	no

GTM_TC.H007 GTM to CAN Timer Triggers

The CAN transmit trigger inputs of the individual CAN nodes are connected to GTM trigger outputs as specified in table "CAN Transmit Trigger Inputs" in the MultiCAN+ chapter of the User's Manual.

The corresponding GTM TOM/ATOM channel is selected in register GTM_CANOUTSEL as specified in tables "CAN Timer Triggers" in the GTM chapter. Note that not all specified SELx bit fields in register CANOUTSEL are used for trigger selection.

The following GTM to CAN connections are implemented:

Table 23 GTM to CAN Connections in TC23x

CAN Node	GTM Trigger Selection via Bit Field
CAN Node 0	CANOUTSEL.SEL0
CAN Node 1	CANOUTSEL.SEL1
CAN Node 2	CANOUTSEL.SEL2
CAN1 Node 0	CANOUTSEL.SEL0
CAN1 Node 1	CANOUTSEL.SEL1
CAN1 Node 2	CANOUTSEL.SEL2

GTM_TC.H009 TIM0 Channel x Input Selection - Mapping for QFP-80 and QFP-100 Packages

Basically, the mapping of TIM0 input channels to port pins follows a strict family concept: functions available in a lower pin-count package are located on the same port pin in the next higher pin-count package.

In tables “TIM 0 Mapping for QFP-80” and “TIM 0 Mapping for QFP-100” in chapter “Port to GTM Control Registers” of the GTM chapter in the User’s Manual, some rows are incorrect. The following **Table 24** and **Table 25** show the corresponding corrections.

Note: Table “TIM 0 Mapping for QFP-144/BGA-292” in the User’s Manual is correct, as well as the tables in chapter “Port Connections” of the GTM chapter, and the GTM connections listed in the Data Sheet.

Recommendation

For the correct port connections on QFP-80 and QFP-100 packages, use tables “GTM to Port Mapping for QFP-80” and “GTM to Port Mapping for QFP-100” in chapter “Port Connections” of the GTM chapter, or the Data Sheet.

Corrections

The following **Table 24** and **Table 25** show the **corrected** rows of tables “TIM 0 Mapping for QFP-80” and “TIM 0 Mapping for QFP-100”.

*Note: Connections for CHxSEL encodings not listed in **Table 24** or **Table 25** are correctly printed in the corresponding tables in the User’s Manual.*

Table 24 Corrections to Table “TIM 0 Mapping for QFP-80”

Field CHxSEL	QFP-80: Pad / Input	Name
CH0SEL		
0100_B	Reserved	-
0101_B	Reserved	-
0111_B	Reserved	TIN53
1000_B	Reserved	-

Table 24 Corrections to Table "TIM 0 Mapping for QFP-80" (cont'd)

Field CHxSEL	QFP-80: Pad / Input	Name
1011_B	P02.8	TIN8
1100_B	Reserved	-
CH1SEL		
0011_B	Reserved	-
0100_B	P14.6	TIN86
0101_B	Reserved	-
0110_B	Reserved	TIN54
1000_B	P33.5	TIN27
CH2SEL		
0001_B	Reserved	-
0011_B	Reserved	-
0100_B	P10.5	TIN107
0101_B	Reserved	-
0110_B	Reserved	-
1000_B	Reserved	-
1001_B	P33.6	TIN28
CH3SEL		
0001_B	Reserved	-
0011_B	Reserved	-
0100_B	P10.6	TIN108
0110_B	Reserved	-
1001_B	P33.7	TIN29
CH4SEL		
0010_B	Reserved	-
0100_B	Reserved	-

Table 24 Corrections to Table "TIM 0 Mapping for QFP-80" (cont'd)

Field CHxSEL	QFP-80: Pad / Input	Name
0101_B	Reserved	-
CH5SEL		
0011_B	Reserved	-
0100_B	Reserved	-
0110_B	Reserved	-
CH6SEL		
0100_B	P23.1	TIN42
0101_B	Reserved	-
0110_B	Reserved	-
CH7SEL		
0010_B	P14.4	TIN84
0011_B	P20.8	TIN64
0100_B	Reserved	-
0101_B	Reserved	-
0110_B	Reserved	-

Table 25 Corrections to Table "TIM 0 Mapping for QFP-100"

Field CHxSEL	QFP-100: Pad / Input	Name
CH0SEL		
0001_B	Reserved	-
1010_B	Reserved	-
1100_B	Reserved	-
CH2SEL		
1000_B	Reserved	-

Table 25 Corrections to Table "TIM 0 Mapping for QFP-100" (cont'd)

Field CHxSEL	QFP-100: Pad / Input	Name
CH4SEL		
1001_B	Reserved	-
1010_B	Reserved	-

GTM_TC.H011 First CM0 updates in case of SR0=1 and (A)TOM used as Triggered Channel

In case the CM0 register should be updated from the shadow register with 1, the Force Update mechanism (FUPD(x) signal) has to be enabled on the (A)TOM channel. Otherwise the first edge triggered from CM0 will not be generated after 1 appears in CM0.

GTM_TC.H014 Synchronous Bridge Mode Restrictions

The reset value for register GTM_BRIDGE_MODE is specified as 0400 1001_H, and should never be changed according to the User's Manual, i.e. the AEI bridge should always operate in async_bridge mode.

Exception

In order to improve access latency, operation in synchronous bridge mode is possible if it is ensured that the SPB frequency is identical to the GTM frequency:

- $f_{SPB} == f_{GTM}$

Sequence to configure the bridge in synchronous mode (pseudocode):

```
/* ensure that no data are read or written in the GTM */
if(fSPB == fGTM)
{
GTM_BRIDGE_MODE = 0x04011000; /* switch to sync mode, reset
bridge*/
```

```
while(GTM_BRIDGE_MODE & 0x100) /* wait till mode change
completed */
;
}
else
;
```

GTM_TC.H015 Register TIMi_CHx_CTRL - Correction to Register Image

The register image of register TIMi_CHx_CTRL (i=0) erroneously shows bit 19 as “Reserved” with type “r” (read only).

Correction

Actually, bit 19 has type “rw” and is correctly described in the register table as copied from the User’s Manual in **Table 26** below:

Table 26 Bit EXT_CAP_EN in Register TIMi_CHx_CTRL

Field	Bits	Type	Description
EXT_CAP_EN	19	**rw**	**Enables external capture mode** The selected TIM mode is only sensitive to external capture pulses, the input event changes are ignored 0_B External capture disabled 1_B External capture enabled

INT_TC.H004 Corrections to the Interrupt Router Documentation

The following corrections apply to chapter “Interrupt Router (IR)” of the TC21x/TC22x/TX23x Family User’s Manual:

Figure “Block Diagram of the TC21x/TC22x/TC23x Interrupt System” erroneously shows ICU3 related to DMA.

- **Correction**:

– Only ICU0 and ICU1 are implemented, with **ICU1** related to the DMA.

Table “Registers Overview - System, OTGM and ICU Control Registers” erroneously shows ICU1 registers INT_LWSR1, INT_LASR1, INT_ECR1 related to CPU1.

- **Correction**:
  – Registers INT_LWSR1, INT_LASR1, INT_ECR1 are related to the **DMA**.

IOM_TC.H001 How to clear the IOM_LAMEWCm register

The Logic Analyzer Module Event Window Count Status register IOM_LAMEWCm stores the window count value reached prior to being cleared in the LAM block once an event has been generated.

Writing to IOM_LAMEWCm by software will result in a bus error.

The IOM_LAMEWCm register can be reset (cleared) by software with a write to the IOM_LAMCFGm or IOM_LAMEWSm registers, e.g. by writing the same configuration data that have been read to either of these registers.

Note: The clock divider should be set to IOM_CLC.RMC = 1 when configuring the IOM (see issue IOM_TC.004 “Write to IOM register space when IOM_CLC.RMC > 1”).

IOM_TC.H002 IOM Clock Control

Contrary to the named clocks given within the subsections of the IOM chapter, the entire IOM operates at the higher of the SPB or GTM clock frequencies. This may be further divided via the RMC bit field of the IOM_CLC register, where the physical RMC value represents the divisor. For example, RMC = 00000001_B divides clock by 1, RMC = 00000010_B divides clock by 2, and so on. Note that RMC = 00000000_B disables the clock.

See also the following revised description of the IOM_CLC register.

IOM Clock Control Register (IOM_CLC)

The Clock Control Register CLC allows the programmer to adapt the functionality and power consumption of the module to the requirements of the application. The description below shows the clock control register functionality which is implemented in the BPI_FPI for the module. Where a module kernel is connected to the CLC clock control interface, CLC controls the f_{IOM} module clock signal, sleep mode and disable mode for the module.

Table 27 Description of Fields in IOM Clock Control Register (IOM_CLC)

Field	Bits	Type	Description
DISR	0	rw	**Module Disable Request Bit** Used for enable/disable control of the module. 0_B Module disable is not requested 1_B Module disable is requested
DISS	1	rh	**Module Disable Status Bit** Bit indicates the current status of the module. 0_B Module is enabled 1_B Module is disabled
0	2	rw	**Reserved** Read as 0; should be written with 0.
EDIS	3	rw	**Sleep Mode Enable Control** Used to control module's sleep mode. 0_B Sleep mode request is regarded. Module is enabled to go into Sleep Mode. 1_B Sleep mode request is disregarded. Sleep Mode cannot be entered upon a request.

Table 27 Description of Fields in IOM Clock Control Register (IOM_CLC) (cont'd)

Field	Bits	Type	Description
RMC	[15:8]	rw	**Clock Divider Value in Run Mode** 00000000_B No clock signal f_{IOM} generated (default after reset) 00000001_B Clock f_{IOM} = max (f_{SPB}, f_{GTM}) selected 00000010_B Clock f_{IOM} = max (f_{SPB}, f_{GTM})/2 selected 00000011_B Clock f_{IOM} = max (f_{SPB}, f_{GTM})/3 selected ... 11111111_B Clock f_{IOM} = max (f_{SPB}, f_{GTM})/255 selected
0	[31:16], [7:4]	r	**Reserved** Read as 0; should be written with 0.

IOM_TC.H003 Configuration of LAMCFG.IVW and LAMEWS.THR

As shown in figure "Logic Analyzer Module (LAM) block diagram" in the IOM chapter of the User's Manual, an EVENT will be generated if the required edge is detected and the XOR between the Event Window value and the invert bit (LAMCFG.IVW) is 1.

When the edge to be detected arrives at LAMEWSn.THR value of the counter, the EVENT will be generated depending on LAMCFG.IVW value:

- If LAMCFG.IVW==0 event will be generated,
- if LAMCFG.IVW==1 event will not be generated.

Taking this behavior into account, the description of the LAMCFG.IVW and/or LAMEWS.THR configuration in examples 2, 4, 5 and 6 of section "Example Monitor/Safety Measures" is misleading.

Correction

The corrected description, including the case "equal to", is as follows (only modified lines are printed):

Example 2 - Pulse or duty cycle too long

LAMCFG.IVW: 0x0 ; don't invert window, capture events when the counter is **equal or** above the threshold.

LAMEWS.THR: select appropriate threshold (maximum duty cycle length required. If duty cycle is longer than this value then an event will be triggered).

Example 4 - Period too long

LAMCFG.IVW: 0x0 ; don't invert window, capture events when the counter is **equal or** above the threshold.

LAMEWS.THR: select appropriate threshold (maximum period length required. If period is longer than this value then an event will be triggered).

Example 5 - Diagnosis of Command and Feedback - acceptable propagation window and/or signal consistency check

LAMCFG.IVW: 0x0 ; don't invert window, capture events when the counter is **equal or** above the threshold.

LAMCFG.THR: set to max delay allowed (if the delay between corresponding edges of reference and monitor signals is longer than this value, the event will be triggered).

Example 6 - Diagnosis of Set-up and Hold times

- Example settings for LAM block registers for Set-up

LAMCFG.IVW: 0x0 ; don't invert window, capture events when the counter is **equal or** above the threshold.

- Example settings for LAM block registers for Hold

LAMCFG.IVR: **0x1** ; invert reference signal (use for gating).

LAMCFG.THR: Acceptable Hold (ref Threshold 2 on waveforms shown, changes in monitor signal will generate an alarm if they occur inside the "THR" cycles after a falling edge in the reference signal).

IOM_TC.H004 Behavior of LAMEWCn.CNT when LAMEWSn.THR is 0

When LAMEWSn.THR is set to 0, no event will be sent from the Logic Analyzer Module (LAM) to the Event Combiner Module (ECM) and no ALARM towards the SMU will be generated.

The rest of the effects derived from the cause generating the event inside the LAM will be maintained, for instance copying the counter to LAMEWCn.CNT (this means LAMEWCn.CNT also may change when LAMEWSn.THR is 0).

IOM_TC.H006 ACCEN* Protection for Write Access to IOM Registers

The access protection symbol ‘P’ to indicate protection by the ACCEN* register mechanism is missing in column “Access Mode - Write” in table “Register Overview” in the User’s Manual for IOM registers with an offset address ≥ 30_H. Actually, these registers have write access attributes ‘U,SV,P’.

Exception

In this design step, a write access to register LAMEWCm will result in a bus error, as correctly reflected by symbol ‘BE’ in column “Access Mode - Write” in table “Register Overview” in the User’s Manual.

IOM_TC.H007 Write Access to FPCESR

The Filter and Prescaler Edge Status Register FPCESR stores the state of detected rising and falling edges from each of the Filter and Prescaler Channels k (k = 0..15).

The flags in this register can be selectively cleared by writing a 0 in the respective bitfield.

However, writing to register FPCESR with a sub-word granularity (e.g. byte or half-word) leads to undefined behavior.

Recommendation

Individual bits for channel k in FPCESR are cleared with a write to the control register (FPCCTRk) or timer register (FPCTIMk).

Writing to FPCESR directly shall be done always to the whole register (32-bit writes), with bits that should not be modified set to 1_B.
In particular, LDMST or SWAPMSK.W should be used only with bit mask enabled for all ´rwh´ bits in register FPCESR.

LMU_TC.H002 On-the-fly BBB:SRI clock ratio switching

Note: This problem only occurs in an ADAS or Emulation Device (ED), but may already need to be considered during software development for the target device.

When switching the clock ratio for f_{BBB} relative to f_{SRI}, make sure that no MMES (Memory Mapped Emulation System) access to EMEM is performed by an SRI master via the LMU. Otherwise, data read/written may be incorrect.

Recommendation

After a MMES read is complete, allow at least 12 SRI clock cycles before initiating a clock ratio change.

After a MMES write is complete, allow at least 20 SRI clock cycles before initiating a clock ratio change.

After a clock ratio change, allow the clock ratio change to become effective before performing any MMES transfer (e.g. read back control register that was written for the clock ratio change).

LMU_TC.H003 Function of Bit MEMCON.PMIC (Protection Bit for Memory Integrity Control Bit)

In the LMU chapter of the User's Manual, the following text (last paragraph in section "Local Memory (LMU SRAM)") is incorrect: Some bitfields of the LMU_MEMCON register are protected by LMU_MEMCON.PMIC bit. If the data written to the register has the bitfield set to 0_B, no change will be made to bits 15_D to 9_D of the register regardless of the data written to these fields.

Correct Description

For the correct description (only bit 9 (ERRDIS) is protected) see the description of bit PMIC in the LMU Memory Control Register in section “LMU Registers”, copied in **Table 28** below:

Table 28 Bit PMIC in Register LMU_MEMCON

Field	Bit	Type	Description
PMIC	8	w	**Protection Bit for Memory Integrity Control Bit** Will always return 0_B when read 0_B Bit Protection: Bit 9 remains unchanged after LMU_MEMCON write. 1_B Bit 9 will be updated by the current write to LMU_MEMCON
ERRDIS	9	rw	**ECC Error Disable** When set SRI bus errors caused by ECC errors in data read from the SRAM will be disabled. ...

MTU_TC.H003 AURIX™ Memory Tests using the MTU

The use of destructive tests such as March-U and Checkerboard etc. in conjunction with FAILDMP mode to get detailed failure information (errors, fail addresses) will cause the SRAM redundancy information to be overwritten.

Therefore, the MTU/MBIST module effectively only supports the Non-Destructive Inversion Test (NDIT).

Recommendation

To avoid overwriting the SRAM redundancy information, only use Non-Destructive Inversion Test. In this case, failure is detected by ECC and the detailed information can be obtained from ETRR and ECCD registers.

Refer to the latest version of Application Note AP32197 “AURIX™ Memory Tests using the MTU” for more details on MTU/MBIST usage and fault coverage.

MTU_TC.H004 Handling the Error Tracking Registers ETRR

CPU and on-chip peripheral SRAMs are capable of detecting errors and generating SMU alarms for correctable, uncorrectable, and address errors. The failing addresses are stored in Error Tracking Registers (ETRR), and the corresponding indicator (CERR/UERR/AERR and SERR) and valid bits (VAL) are set in the Memory ECC Detection Register (ECCD). Only new errors will be considered, i.e. errors at already stored addresses will be ignored. In case the maximum number of ETRR for a memory is used up and a new error occurs, the error overflow bit ECCD.EOV is set, and the corresponding “address buffer overflow” SMU alarm is generated. For peripheral SRAMs, the second error will cause a buffer overflow, and for CPU SRAMs, up to five errors can be registered before the buffer overflow alarm is triggered.

Bit ECCD.TRC (Tracking Clear) allows to clear the EOV and VAL bits in register ECCD and the associated ETRR registers, e.g. in response to a tolerated corrected single bit error.

Corner Case

If in an exceptional corner case software would set TRC at the same time an error overflow occurs, then the EOV bit is not set, and the SMU alarm is not generated.

Recommendation

- It is not necessary to clear the Error Tracking Registers ETRR by software as part of an SRAM error handling concept. For correctable errors, the application software should only react on the address buffer overflow alarm (e.g. with a reset). Single correctable error events may be ignored (within limits) to increase the fault tolerance of the system without impacting the safety.
- If a different concept is used requiring clearing of the ETRR registers by software via ECCD.TRC, make sure that the corresponding SRAM instance is not functionally accessed while the application software writes ECCD.TRC, so that an overflow error cannot be generated during the clear operation.

Information on using the MTU for memory diagnosis is given in Application Note AP32197 “AURIX™ Memory Tests using the MTU”.

MTU_TC.H005 Handling SRAM Alarms

Alarms are generated for CPU and on-chip peripheral SRAMs when correctable, uncorrectable, and address errors are detected.

The failing addresses are stored in Error Tracking Registers (ETRR), and information on the error type is stored in the Memory ECC Detection Register (ECCD). Only new errors will be considered, i.e. errors at already stored addresses will be ignored. In case the maximum number of ETRR for a memory is used up and a new error occurs, the error overflow bit ECCD.EOV is set, and the corresponding “address buffer overflow” SMU alarm is generated.

For peripheral SRAMs, the second error will cause a buffer overflow, and for CPU SRAMs, up to five errors can be registered before the buffer overflow alarm is triggered.

In addition, traps and bus errors are generated for uncorrectable errors, depending on the bus master and type of access.

Corner Case

If in an exceptional corner case

- two errors at different locations are present in the same SRAM
- and accesses are made to both locations within a time window of ~ 10 CPU clock cycles,

then the first access to the location with an error will correctly trigger an SMU alarm, while the second access to the other location with an error will not trigger an SMU alarm. In the worst case, a correctable error may thus mask an uncorrectable or address error.

Note: In case the second error would result in an address buffer overflow, the corresponding bit ECCD.EOV is set and the “address buffer overflow” SMU alarm is correctly generated.
*Therefore, this problem is **not** relevant for peripheral SRAMs that only have one ETRR, as the second error will always cause an SMU alarm.*

Recommendations

- As recommended in Application Hint MTU_TC.H004 (Handling the Error Tracking Registers ETRR), for correctable errors, the application software should only react on the address buffer overflow alarm (e.g. with a reset). Single correctable error events may be ignored (within limits) to increase the fault tolerance of the system without impacting the safety.
- In case an uncorrectable error for a CPU SRAM would neither generate an “address buffer overflow” nor an “uncorrectable” or “address error” SMU alarm, the error handling (typically resulting in a reset) should be performed in the corresponding trap routine.
- In particular for EMEM or FFT SRAMs used in Emulation, ADAS or Extended SRAM devices of the AURIX™ family, a workaround is possible by triggering a correctable error before application startup. This would result in the ECCD.CERR bit of the corresponding MBIST to be set. Any future correctable alarms will not be forwarded[1)] and this issue can be avoided completely.

MTU_TC.H006 Alarm Propagation to SMU via Error Flags in MCx_ECCD

Upon any correctable, un-correctable or address error alarm in an SRAM, the corresponding error flags (CERR, UERR or AERR bits) in the MCx_ECCD register are set, and the corresponding alarm is forwarded to the SMU.

However, in case these bits are set to 1_B, and a further error of the same type occurs, then the corresponding alarm is no longer forwarded to the SMU.

If in a corner case software writes to Mx_ECCD in the same cycle where an error event would set one of the CERR, UERR or AERR bits from 0_B to 1_B, the software write has priority and the status flags remain at 0_B. In this case, however, the alarm is correctly propagated to the SMU.

Note: This behavior does not endanger the concept recommended in Application Hints MTU_TC.H004 and MTU_TC.H005 (ignore correctable errors, react on first uncorrectable/address error/buffer overflow alarm).

1) see MTU_TC.H006 (Alarm Propagation to SMU via Error Flags in MCx_ECCD)

Recommendation

Upon any alarm from an SRAM/MBIST, if a further alarm of the same type is required to be sent to the SMU and processed, then the software shall clear the error flag (CERR, UERR, AERR) in the ECCD register.

The flags can be cleared by writing MCx_ECCD.CERR (or UERR or AERR, respectively) with 0_B.

MTU_TC.H008 Memory Controllers for DSPR

Due to its implementation, the Data Scratch Pad RAM (DSPR) of CPU0 has two Memory Controller instances, described as MC14 (MC_CPU0_DSPR) and MC27 (MC_CPU0_DSPR2) in the MTU chapter of the User's Manual.

Each Memory Controller covers one half of the SRAM. In order to fully test the DSPR, the test[1)] has to be executed once on each Memory Controller (i.e. only one of the two Memory Controllers is enabled at a time).

As both Memory Controllers share the same ECC decoders, any error detected by a test executed on one of the Memory Controllers will be logged in the Error Tracking Registers of both Memory Controllers.

Note that once an error status bit is set, further alarms of the same type are not forwarded to the SMU until the flag is cleared (see MTU_TC.H006 "Alarm Propagation to SMU via Error Flags in MCx_ECCD").

Recommendation

- Enable only one of the two Memory Controllers at a time.
- Before executing a test on CPUx_DSPR (respectively CPUx_DSPR2), clear the Error Tracking Registers and the error status bits of CPUx_DSPR (respectively CPUx_DSPR2), so that the test reflects the results of only the one memory which is being tested.
- It is also recommended to clear the Error Tracking Registers and the error status bits of both CPUx_DSPR and CPUx_DSPR2 after executing each test.

1) Test in this context means Non-Destructive Inversion Test (NDIT, see also MTU_TC.H003).

- Alternatively, before executing a test on CPUx_DSPR (respectively CPUx_DSPR2), disable the error notifications in CPUx_DSPR2 (respectively CPUx_DSPR) and reenable them after the test. It is also recommended to clear the Error Tracking Registers and the error status bits of CPUx_DSPR (respectively CPUx_DSPR2) after executing a test on it.

Regarding configuration and use of the two Memory Controllers, see also the latest version of Application Note AP32197 “AURIX™ Memory Tests using the MTU”.

MTU_TC.H009 Reset Value for Register ECCD

The reset value of the ECC Detection Register ECCD is documented as 7800_H in the User’s Manual. This is always the case for the SRAMs listed in **Table 29** below (if available in the corresponding product).

Table 29 TC23x SRAMs with ECCD Reset Value = 7800_H

Memory Controller No.	Associated SRAM
17	CPU0 PTAG
38	ERAY0 OBF
39	ERAY0 IBF_TBF

For other SRAMs the ECCD reset value may either be $7C00_H$ or 7800_H.

Bit ECCD.10 is marked as ‘Reserved’ in the User’s Manual:

- When writing to ECCD, bit ECCD.10 should be written as 0_B.
- When reading register ECCD, bit ECCD.10 should not be evaluated. Memory errors will be reported by the notification bits CERR, UERR, AERR and EOV in register ECCD.

MTU_TC.H010 Register MCONTROL - Bit Field Res4

The position of the 3-bit field Res4 within register MCONTROL is incorrectly described as [14:10] in the register description of the User's Manual.

The correct position of the 3-bit field Res4 is MCONTROL.[14:12], as shown in the register image in the User's Manual, and in the following **Table 30**:

Table 30 Register MCONTROL - Position of Bit Field Res4

Field	Bits	Type	Description
Res	15	r	**Reserved** Read returns 0_B, should be written with 0_B
Res4	14:12	**rw**	**Reserved** Read returns 0x4 Must always be written with 0x4
Res	11:10	r	**Reserved** Read returns 00_B, should be written with 00_B

MTU_TC.H011 Access Protection for Memory Control Registers

The access protection symbol 'P' to indicate Access Enable Register protection is missing in column "Access Mode - Write" in table "Register Overview of each MTU Memory Control register block" of the MTU chapter in the User's Manual.

The MTU Memory Control register block actually has protection via the Access Enable registers (ACCEN0/1).

MTU_TC.H012 Kernel Reset triggers Reset of MBIST Registers

When a kernel reset is executed (via bit RST in registers KRST0/1) for a module equipped with Memory Controllers (MC) for its internal RAMs, also the corresponding MTU Memory Control (MBIST) registers are reset.

Recommendation

If required, analyze/save the contents of the MBIST registers before executing a kernel reset.

After a kernel reset, reconfigure the MBIST registers.

MTU_TC.H014 Access to SRAM while MTU operations are underway

When MTU operations on the SRAM are underway, the memories cannot be accessed. MTU operations in this context include:

1. Running an MBIST test (e.g. Non-destructive test).
2. Performing an SRAM initialization using the MTU.
3. When an Auto-data-initialization is underway.

During these operations, the SRAM shall not be accessed. If the SRAM is accessed during this time, unexpected behavior may occur (e.g. access timeout).

Cases 1. and 2. are easily identified, i.e. whenever the application has triggered an MBIST test or SRAM initialization.

Case 3. occurs whenever bit field PROCOND.RAMIN is not equal to 0x3. Whenever this is the case in specific MBIST controllers, the SRAM is fully or partially cleared under certain conditions:

- When MTU_MEMTEST.*EN bit is enabled or disabled.
- When MTU_MEMMAP.*MAP bit is set or cleared (applicable only to cache memories).

This means, when the above mentioned bits are set or cleared, it takes some time (~hundreds of clock cycles) for the associated SRAMs to be (fully or partially) initialized. During this time the SRAM is not accessible.

Affected SRAMs are:

- CPUx DMEM (DSPR+DCACHE)
- CPUx PMEM (PSPR + PCACHE)

Recommendation

- For all memories, ensure that the SRAM is not accessed when any MTU operation is underway.

- For the specific memories listed above, ensure that the SRAM is not accessed:
  - When setting MTU_MEMTEST.*EN bit: as long as MEMSTAT.*AIU bit is set or as long as the MEMTEST.*EN bit is not yet set.
  - When clearing MTU_MEMTEST.*EN bit: as long as MEMSTAT.*AIU bit is set or as long as the MEMTEST.*EN bit is not yet cleared.
  - When setting or clearing MTU_MEMMAP.*MAP bit for DMEM/PMEM: as long as MEMSTAT.*AIU bit is set.

MultiCAN_AI.H005 TxD Pulse upon short disable request

If a CAN disable request is set and then canceled in a very short time (one bit time or less) then a dominant transmit pulse may be generated by MultiCAN module, even if the CAN bus is in the idle state.

Example for setup of the CAN disable request:

`CAN_CLC.DISR` = 1 and then `CAN_CLC.DISR` = 0

Workaround

Set all INIT bits to 1 before requesting module disable.

MultiCAN_AI.H006 Time stamp influenced by resynchronization

The time stamp measurement feature is not based on an absolute time measurement, but on actual CAN bit times which are subject to the CAN resynchronization during CAN bus operation.The time stamp value merely indicates the number of elapsed actual bit times. Those actual bit times can be shorter or longer than nominal bit time length due to the CAN resynchronization events.

Workaround

None.

MultiCAN_AI.H007 Alert Interrupt Behavior in case of Bus-Off

The MultiCAN module shows the following behavior in case of a bus-off status:

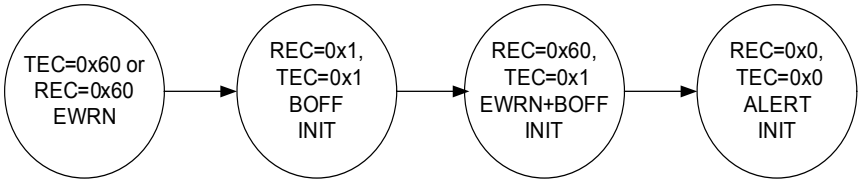

Figure 8 Alert Interrupt Behavior in case of Bus-Off

When the threshold for error warning (EWRN) is reached (default value of Error Warning Level EWRN = 0x60), then the EWRN interrupt is issued. The bus-off (BOFF) status is reached if TEC > 255 according to CAN specification, changing the MultiCAN module with REC and TEC to the same value 0x1, setting the INIT bit to 1_B, and issuing the BOFF interrupt. The bus-off recovery phase starts automatically. Every time an idle time is seen, REC is incremented. If REC = 0x60, a combined status EWRN+BOFF is reached. The corresponding interrupt can also be seen as a pre-warning interrupt, that the bus-off recovery phase will be finished soon. When the bus-off recovery phase has finished (128 times idle time have been seen on the bus), EWRN and BOFF are cleared, the ALERT interrupt bit is set and the INIT bit is still set.

MultiCAN_TC.H003 Message may be discarded before transmission in STT mode

If `MOFCRn.STT=1` (Single Transmit Trial enabled), bit TXRQ is cleared (TXRQ=0) as soon as the message object has been selected for transmission and, in case of error, no retransmission takes places.

Therefore, if the error occurs between the selection for transmission and the real start of frame transmission, the message is actually never sent.

Workaround

In case the transmission shall be guaranteed, it is not suitable to use the STT mode. In this case, `MOFCRn.STT` shall be 0.

MultiCAN_TC.H004 Double remote request

Assume the following scenario: A first remote frame (dedicated to a message object) has been received. It performs a transmit setup (TXRQ is set) with clearing NEWDAT. MultiCAN starts to send the receiver message object (data frame), but loses arbitration against a second remote request received by the same message object as the first one (NEWDAT will be set).

When the appropriate message object (data frame) triggered by the first remote frame wins the arbitration, it will be sent out and NEWDAT is not reset. This leads to an additional data frame, that will be sent by this message object (clearing NEWDAT).

There will, however, not be more data frames than there are corresponding remote requests.

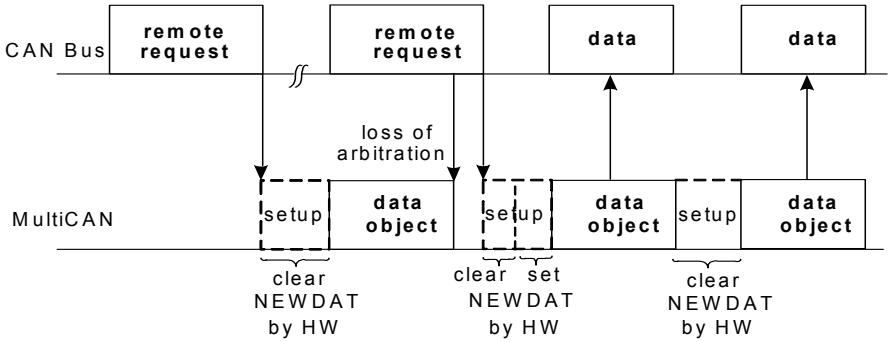

Figure 9 Loss of Arbitration

MultiCAN_TC.H007 Oscillating CAN Bus may Disable the CAN Interface

If the connected CAN network is in an unspecified oscillating state for more than 512 cycles this can result in disabling the CAN interface of the device. Enabling the CAN interface again requires then a Power-on Reset.

Recommendation

Please refer to application note AP32264 “DXCPL DAP over CAN Physical Layer” for further information and how this situation can be prevented.

MultiCAN_TC.H008 Changes due to CAN FD protocol ISO 11898-1:2015

Note: This Application Hint might affect the SFR C Header Definitions. In such cases, SFR usage in the software shall be analyzed within the applications for their correct handling.

Introduction

Specific variants of this device step support the CAN FD frame format according to standard version ISO 11898-1:2015. These variants are identified by the feature type code **`N`** as last letter in the device name, e.g.

- SAK-TC234LP-32F200**N**

*Note: In TC23x variants with feature type code `N`, nodes 0 and 1 in MultiCAN and MultiCAN1 support this feature, while nodes 2 don’t; see **Table 34** at the end of this text module.*

For availability of the variants with this feature see the corresponding “AURIX™ TC2xx Variants / Data Sheet Addendum”.

Detailed Description

ISO 11898-1:2015 improves the failure detection capabilities of the ISO11898-1 DIS version 2014. Information about the number of stuff bits in the data field is added to the CRC field. These added bits are called **‘Stuff Count’**.

The Stuff Count contains 4 bits, including

- 3 bits gray code to represent the modulo-8 of number of stuff bits in the data field,
- and 1 bit for the parity.

Since the Stuff Count bits are part of the CRC field, fixed stuff bits will be added before and after the Stuff Count bits. **Figure 10** and **Figure 11** show the frame format of the ISO 11898-1:2015 CAN FD protocol. There is no change in the classical CAN frame format.

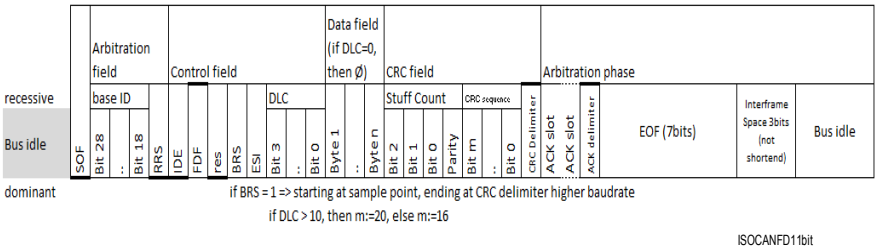

Figure 10 ISO CAN FD 11-bit ID Data Frames

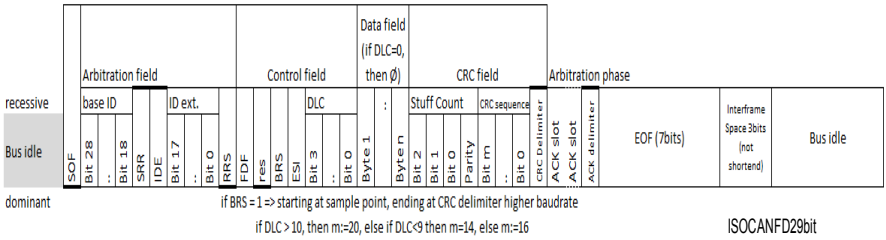

Figure 11 ISO CAN FD 29-bit ID Data Frames

From here on,

- the ISO 11898-1:2015 frame format will be referred to as **ISO** CAN FD format,
- the previous frame format will be referred to as **Non-ISO** CAN FD format.

Note: The ISO CAN FD frame format is incompatible with Non-ISO CAN FD frame format.

AURIX™ devices (with feature type code `N`) support both ISO and Non-ISO CAN FD formats. The format can be selected by modified functionality of bits NBTR0.15 and NBTR1.15:

Functionality of Bit NBTR0.15

NBTR0.15 is changed from NBTR0.DIV8 (Divide Prescaler Clock by 8) to **NBTR0.NISO**[1)] (Non-ISO operation) as shown in **Table 31**:

Table 31 Functionality of Bit NBTR0.15

Field	Bit	Type	Description
NISO	15	rw	**Non-ISO Operation** If this bit is set, the MultiCAN+ uses the non-ISO CAN FD frame format. This bit is CCE protected. 0_B CAN FD frame format according to ISO 11898-1:2015 (default after reset) 1_B CAN FD frame format non-ISO.

Functionality of Bit NBTR1.15

NBTR1.15 is changed from NBTR1.DIV8 (Divide Prescaler Clock by 8) to **NBTR1.PED**[1] (Protocol Exception Disable) as shown in **Table 32**:

Table 32 Functionality of Bit NBTR1.15

Field	Bit	Type	Description
PED	15	rw	**Protocol Exception Disable** The protocol exception event is described in the ISO 11898-1:2015 as option. The error frame on the res bit can be controlled with this option. This bit is CCE protected. 0_B Protocol Exception Event is enabled (default after reset). 1_B Protocol Exception Event is disabled.

Note: Both NBTR0.NISO and NBTR1.PED are global register bits. This means they affect all the ISO 11898-1:2015 compliant CAN FD nodes in the respective MultiCAN+ module.
The former DIV8 function of nodes 0 and 1 is hard-wired to 0_B (i.e. a time quantum lasts (BRP+1) clock cycles).

1) The symbolic names NISO and PED are only used for explanation in this context. If desired, the register definition file could be modified.

The DIV8 function (Divide Prescaler Clock by 8) for all other nodes x (x>1) remains the same, irrespective of the setting of NBTR0.NISO and NBTR1.PED.

Table 33 describes the CAN FD behavior for different configurations of the NBTR0.NISO and NBTR1.PED bits. By default, the CAN FD behaves in compliance with ISO 11898-1:2015 if CAN FD is enabled (bit FDEN = 1_B for corresponding node).

Table 33 Configurations of PED and NISO

PED	NISO	CAN FD Enabled
0	0	Default values - ISO 11898-1:2015 CAN FD compliant
0	1	Non-ISO CAN FD format - same behavior as previous AURIX™ devices
1	0	CAN FD with protocol exception event disabled - ISO 11898-1:2015 CAN FD compliant
1	1	Reserved

Note: Nodes where FDEN = 0_B will operate using the classical CAN frame format.

Summary of Devices and Nodes supporting ISO CAN FD

The following table summarizes the nodes of devices with feature type code `N` which have the ISO 11898-1:2015 CAN FD functionality.

Table 34 AURIX™ TC23x Devices/Nodes supporting ISO CAN FD

Device / Step	ISO CAN FD supporting nodes	Non-ISO CAN FD supporting nodes
TC23x[1] ≥ AC	MultiCAN - Nodes 0,1 MultiCAN1 - Nodes 0,1	MultiCAN - Node 2 MultiCAN1 - Node 2

1) Emulation (ED) and ADAS Devices only support Non-ISO CAN FD

MultiCAN_TC.H009 Limitation on Secondary Sample Point (SSP) Position (ISO CAN FD nodes only)

Note: This Application Hint only applies to ISO CAN FD nodes. For devices and nodes supporting the ISO CAN FD format, see MultiCAN_TC.H008.

The MultiCAN+ of AURIX™ TC2xx has passed the ISO/DIS 16845-1(E), 2015 CAN Conformance test performed by an external test house C&S group GmbH and the test reports are available. The limitation on the range of SSP position is described in the Conformance test report.

In AURIX™ TC2xx devices, there are two limitations with the Secondary Sample Point (SSP) position for CAN FD with respect to ISO 11898-1, 2015 specification:

1. Granularity of the Transmitter loop delay measurement (only when CAN_FNBTEVRx.FBRP = 1)

Limitation

The Transmitter loop delay measurement is based on data-phase time quantum ($t_{q(D)}$) and not by minimum time quanta (mtq) or CAN clock period as specified in ISO 11898-1 2015. Hence the granularity of the transmitter loop delay measurement is +1 $t_{q(D)}$ in worst case scenario.

Note: According to ISO 11898-1 – 2015, when Transmitter Delay Compensation is enabled (CAN_NTDCR.TDC = 1), then the CAN_FNBTEVRx.FBRP shall be either 0 or 1.

Effect

In worst case scenario, the SSP could be delayed by +1 $t_{q(D)}$.

Recommendation

It has to be taken care that the SSP offset (CAN_NTDCR.TDCO) is configured accordingly by including the granularity of the transmitter loop delay measurement of +1 $t_{q(D)}$ in worst case scenario.

2. Range of SSP position (only when CAN_FNBTEVRx.FBRP = 0)

Limitation

The Secondary Sample Point Position is limited to 31 t_q or 31 mtq (bit field CAN_NTDCRx.TDCV), when compared to 63 mtq as required by ISO 11898-1, 2015.

Note: When CAN_FNBTEVRx.FBRP = 0, then
1 time-quantum (t_q) = 1 minimum time-quantum (mtq).

CAN FD applications with fast data baud rate greater than 2 Mbit/s require Fast Baud Rate Prescaler setting CAN_FNBTEVRx.FBRP = 0 and f_{CAN} at 80 MHz to ensure reliable CAN communication in long networks. In such a scenario, the max SSP position achievable by the TDC is limited to 31 t_q, i.e. 388 ns (31 * 12.5 ns).

Effect

In scenarios where the sum of transmitter loop delay and SSP offset (CAN_NTDCRx.TDCO) is more than 31 time quanta, the SSP value saturates at 31 time quanta, leading to SSP placed (at 31 time quanta) earlier than required.

Recommendation

It has to be taken care to ensure that the sum of transmitter loop delay and SSP offset (CAN_NTDCRx.TDCO) is within the limit of 31 time quanta.

MultiCAN_TC.H010 Limitation on maximum SJW Range for CAN FD Data Phase (ISO CAN FD nodes only)

Note: This Application Hint only applies to ISO CAN FD nodes. For devices and nodes supporting the ISO CAN FD format, see MultiCAN_TC.H008.

The MultiCAN+ of AURIX™ TC2xx has passed the ISO/DIS 16845-1(E), 2015 CAN Conformance test performed by an external test house C&S group GmbH and the test reports are available.

ISO 11898-1, 2015 specifies the configuration range of the CAN FD Data phase (re-)synchronization jump width (SJW) as 1-8 $t_{q(D)}$.

In AURIX™ TC23x devices, the CAN FD Data phase SJW is limited to 1-4 $t_{q(D)}$, as bit fields CAN_FNBTRx.FSJW and CAN1_FNBTRy.FSJW are 2 bits wide.

Effect

Configuring a MultiCAN+ node for CAN FD communication with CAN FD Data Phase SJW less than required, could result in wrong sampling of the received bit of CAN FD Data Phase, thus causing a Receive Error.

Recommendation

Choose the CAN FD configuration in such a way that

- The period of time-quanta in Arbitration phase is equal to the period of time-quanta in data phase. This can be achieved by configuring CAN_NBTEVRx.BRP = CAN_FNBTRx.FBRP.
- CAN_FNBTRx.FSJW = min(CAN_FNBTRx.TSEG2, 3)

By this configuration the effect of limited Data SJW range offered by MultiCAN+ on maximum oscillator tolerance required (as given by conditions described in ISO 11898-1) is minimized.

OCDS_TC.H010 JTAG requires two initial clock cycles after $\overline{\text{PORST}}$

For a proper selection of the chip internal TCK clock path, two TCK clock cycles are needed after $\overline{\text{PORST}}$ release. They can be executed with TMS Low or High. A following TCK clock cycle with TMS High will always bring the JTAG TAP state to Run-Test/Idle. This sequence is compliant to standard JTAG and can be used for all TriCore devices.

OCDS_TC.H012 Minimum Hold Time for Inputs OCDS_TGIx

Inputs OCDS_TGIx (x=0..7, depending on device/package type) may be used to trigger the On-Chip Debug System (OCDS) e.g. for break or interrupt from an external source.

To ensure the external trigger is sampled correctly and not missed, the trigger should be asserted for a minimum of two SPB clock cycles.

PLL_ERAY_TC.H002 Correction in Figure "PLL_ERAY Block Diagram"

The signal originating from block "K2-Divider" in figure "PLL_ERAY Block Diagram" in chapter "ERAY Phase-Locked Loop" of the User's Manual is incorrectly labeled as PLLERAYSTAT.K**1**RDY.

Correction

The correct name of the signal originating from block "K2-Divider" is PLLERAYSTAT.K**2**RDY.

PMC_TC.H001 Check for permanent Overvoltage during Power-up

After an initial power-on with a permanent overvoltage condition on either V_{EXT}, V_{DDP3} or V_{DD} supply rails, no overvoltage alarm may be generated by the SMU after configuration of the alarms, as the threshold transition condition has already happened.

However, in case an overvoltage condition was present, it will be indicated by flags OV13, OV33, and OVSWD, respectively, in register EVRSTAT.

Recommendation

Check the OV13, OV33, and OVSWD flags in register EVRSTAT by software at start-up to identify an overvoltage condition.

PMC_TC.H004 Selecting the WUT Clock Divider

Wake-up timer usage with PMSWCR3.WUTDIV = 1_B (10 ms count) for PMSWCR3.WUTREL values up to 20 ms is exposed to synchronization issues. The WUT counter PMSWUTCNT.WUTCNT is counted down to 0 every 10 ms, and reloading of WUTREL happens 10 ms later. If Standby request is sent before reloading PMSWCR3.WUTREL, regardless of

PMSWSTATCLR.WUTWKPCLR, wake-up request is issued without counting down. This leads to immediate wake-up.

Recommendation

Use WUT with setting PMSWCR3.WUTDIV = 1_B only for longer time periods (more than 20 ms).

For shorter periods the 10 µs clock should be used with setting PMSWCR3.WUTDIV = 0_B (default after reset).

PMS_TC.H002 Sensitivity to supply voltage ripple at VDDP3 during start-up

The internal back-up clock is sensitive to specific power supply voltage disturbance/ripple caused by a voltage ripple intrinsic to DC-DC converters. Specific conditions such as insufficient filtering of the ripple may lead to improper behavior of the start-up scheme of the back-up clock, and thus stuck-at state during the start-up of the microcontroller until this condition is removed.

The acceptable voltage vs. frequency characteristic is portrayed below on the chart:

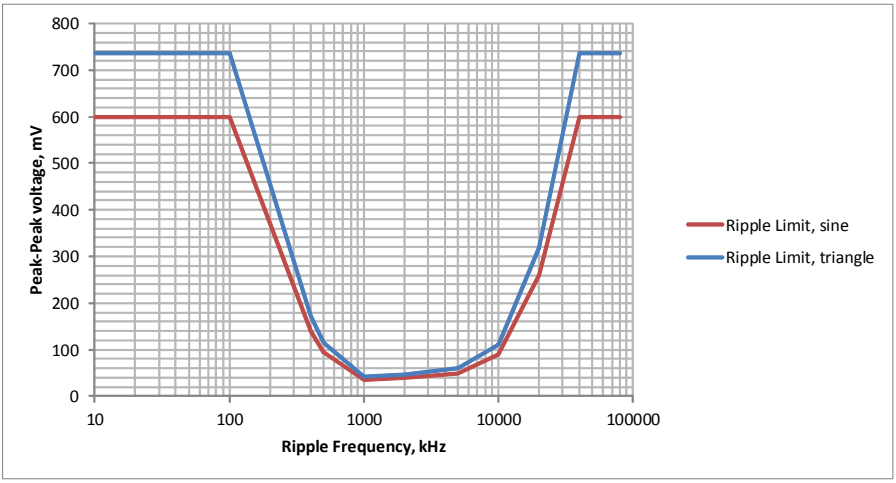

Figure 12 Ripple Voltage vs. Frequency Characteristic

The diagram reflects acceptable ripple level during the cold start of the microcontroller at the VDDP3 supply of the PMS subsystem. For devices in QFP-144, QFP-100 and QFP-80 packages the ripple is reflected for pin 69, pin 47, and pin 37, respectively.

Recommendation 1

Apply an additional ceramic capacitor at the VDDP3 supply input (at pins specified above) to attenuate the residual ripple of the buck converter. The resonant frequency of the additional filter capacitor shall be chosen in accordance with the amplitude-frequency characteristic given above and the switching frequency of the DC-DC converter in order to provide a proper attenuation in the range of interest.

The amount of ripple voltage can be approximated by $V_{pk-pk} = I_{load} / (f*C)$ and therefore the necessary nominal value of the blocking capacitance can be estimated as $C = I_{load} / (f*V_{pk-pk})$

It is recommended to take the I_{load} value as approximately 10 mA for the start-up load at the VDDP3 domain before the internal regulator starts.

The frequency shall be taken same as the switching frequency of the external DC-DC voltage regulator. For example:

C = (0.010 A) / (10^6 Hz * 0.040 V) = 0.25 * 10^{-6} F

Recommendation 2

Dimension the output LC filter of the external DC-DC converter to meet the limit of the ripple below the specified limit at the switching frequency. The effective value of ripple current flowing in and out of the buffer capacitor is calculated in accordance with standard formulas for the DC-DC buck converters. Selection of the low-ESR buffer capacitor is crucial in such applications, as the ESR value is directly proportional to the voltage drop caused by inductor current ripple.

Recommendation 3

Supply VDDP3 rail by an external post LDO power stage.

PORTS_TC.H006 Using P33.8 while SMU is disabled

Per default, the SMU is enabled (SMU_CLC = 0x0) and collects the alarms from the safety mechanisms defined by the safety concept. The SMU may optionally use P33.8 to output the Fault Signaling Protocol (FSP), selectable via register SMU_PCTL. To satisfy safety requirements, it is ensured that the pad configuration of this pin is not affected by an application or system reset after the first 0-to-1 transition of bit SMU_PCTL.PCS.

If the SMU is enabled, but is not using P33.8 for the FSP function, this pin may be used as general purpose input/output (GPIO) or alternate function input/output, controlled via the corresponding P33 registers.

However, if the SMU is disabled by software (SMU_CLC.DISR = 1_B, i.e. not clocked), configuration of P33.8 (pull devices, driver settings, selection of alternate function, etc.) requires special considerations as described in the following, otherwise the configuration change may not become effective.

Recommendations

- If P33.8 shall be used as GPIO or alternate function input/output, do not disable the SMU, i.e. keep SMU_CLC = 0x0 (default after reset). In this case, the configuration of P33.8 may be changed by software at any time.
- Alternatively, configure P33.8 before the SMU is disabled by software (SMU_CLC.DISR = 1_B). After the SMU is disabled, the configuration of P33.8 can no longer be modified by software.
- Alternatively, if the SMU is disabled by software (SMU_CLC.DISR = 1_B, i.e. not clocked), clear bit position 8 at address 0xF003 D364 in the P33 address space once after any reset (Application, System Reset, PORST) before configuring P33.8. Controlling P33.8 as FSP by SMU is possible only once after a reset.

Note: Write access to address 0xF003 D364 is Safety ENDINIT protected.

QSPI_TC.H005 Stopping Transmission in Continuous Mode

The QSPI module supports the following mechanisms to (temporarily) suspend its operation:

- Pause by setting bit GLOBALCON.EN = 0_B via software
- Disable by setting bit CLC.DISR = 1_B via software
- Sleep Mode (enabled with CLC.EDIS = 0) requested by hardware
- Suspend Mode requested by hardware (debugger)

These modes and their handling is described in detail in section “Operation Modes” of the QSPI chapter in the User’s Manual.

In **Continuous Mode**, the following specific behavior of QSPI module has to be considered:

- In case the QSPI module is put into **Pause** state by setting bit GLOBALCON.EN = 0_B via software, it continues transmission until the end of the TRAIL phase of the frame with BACON.LAST = 1_B.
- In case the QSPI module is put into **Disable**, **Sleep**, or **Suspend** mode, the frame is stopped after the next trailing delay (character n). In case BACON.LAST was not =1_B at that time, transmission continues with character n+2 when operation from Disable/Sleep/Suspend state is resumed, i.e. data loss (character n+1) will occur.

Recommendation

Ensure that software does not put the QSPI module into Pause or Disable state (via GLOBALCON.EN or CLC.DISR) while a transmission in Continuous Mode is ongoing.

If Sleep Mode is used in the system, disable acceptance of sleep requests (set CLC.EDIS = 1_B) before starting data transmission in Continuous Mode.

During debugging, ensure that the QSPI is not suspended while it is transmitting in Continuous Mode.

QSPI_TC.H006 Corrections to Figures "QSPI - Frequency Domains" and "Phase Duration Control, Overview"

In the current version of the User's Manual,

- Figure "QSPI - Frequency Domains" erroneously uses the term "f_{PER}" instead of "f_{BAUD2}", and
- Figure "Phase Duration Control, Overview" erroneously uses the term "T_{PER}" instead of T_{BAUD2}".

Correction

- $f_{SCLK} = 1/f_{BAUD2}$ in Figure "QSPI - Frequency Domains", and
- $T_{BAUD2} = 1/f_{BAUD2}$ in Figure "Phase Duration Control, Overview".

QSPI_TC.H007 RXFIFO Overflow Bit Behavior in Slave Mode

In slave mode, if no data word has been written to TXFIFO during initialization before the master starts sending data, the error flag corresponding to an RXFIFO overflow (bit STATUS.5) is set to 1_B.

Recommendation

To avoid this RXFIFO overflow event, write (at least) one word to TXFIFO during initialization and after each reset in slave mode. For following transmissions, no data need to be written to TXFIFO to avoid this effect.

RESET_TC.H002 Unexpected SMU Reset Indication in SCU_RSTSTAT

Under certain conditions the Reset Status Register SCU_RSTSTAT can show an SMU reset indication in addition to the real reset trigger (e.g. a SW reset).

The explanation of this behavior refers to section “Reset Generation” and following pages in chapter “RCU” of the User’s Manual.

Figure “Reset Overview” shows that all warm resets are executed in a defined sequence. This sequence ensures that first the active CPUs are ramped down, then at 80µs the Flash receives an idle request and at 180µs the reset is executed.

The idle request to the Flash makes it immediately busy, all read requests after this point fail with a bus error. All non-CPU masters (HSM, Ethernet, HSSL, DMA and DAM) however continue operation from 80µs to 180µs. When one of these masters reads the busy Flash, a bus error is signaled to the SMU as alarm ALM3[30] (SRI) and/or ALM3[31] (SPB).

If the SMU is configured to react on this by a reset request, this will be noted in the SCU_RSTSTAT register in addition to the original warm reset.

This applies mainly to the master HSM which fetches its code from PFlash.

Recommendations

- Generally a different alarm handling can be configured in the SMU for the mentioned alarms, e.g. trigger an NMI trap but not a reset.
- When the application detects after reset that SCU_RSTSTAT has an additional SMU reset indication it might ignore it and proceed based on the other reset indication.
- In case of SW resets the application can prepare the system just before activating the reset:
  - The non-CPU masters can be disabled or in case of HSM it can be informed about the imminent SW reset and continue execution from RAM.
  - The mentioned alarms can be disabled or the alarm reaction can be changed to trigger an NMI trap.
  - The SMU module reset can be used to reconfigure the SMU into its initial state in which only watchdog timeout alarms are handled.

RESET_TC.H003 Usage of the Prolongation Feature for ESR0 as Reset Indicator Output

The ESR0 pin can be used as reset indicator output and in such a case its active low state can be prolonged upon user-configurable selection as described in section “ESRx as Reset Output” of chapter “Reset Control Unit (RCU) in the User’s Manual.

According to this description, an ESR0CNT value of 0 defines “as soon as possible after start of Boot Code execution”, where “as soon as possible” means:

- about 500 µs after cold power-on,
- not less than 20 µs after other types of reset.

Warning

In case of ESR0CNT = 2, the ESR0 pin will never be released by the device and the user code will never start.

Note: On the other hand - as explained before - configuring an ESR0CNT value of 1 or 2 would anyhow not be effective as a prolongation time below 20 µs is conceptually unachievable.

Recommendation

Do not configure ESR0CNT = 2.

If prolongation of about 20 µs or below is needed, configure ESR0CNT = 3 or 0 instead.

RESET_TC.H004 Effect of Power-on and System Reset on DSPR

The following part of footnote [2)] on Table “Effect of Reset on Device Functions” in the RCU chapter “Module Reset Behavior” regarding the effect of startup firmware on Data Scratchpad RAM (DSPR): “DSPR is partially used as a scratchpad by the startup firmware. Previous data stored in the upper 32kB will be overwritten on start-up” is incorrect.

The correct effect is described in the Boot ROM chapter “RAM overwrite during start-up“:

Start-up procedure upon power-on and system reset can overwrite up to 8 Kbyte at the beginning of CPU0 DSPR.

SCU_TC.H009 LBIST Influence on Pad Behavior

The behavior of the GPIO and ESR0/1 pads during LBIST execution is as follows:

- ESR0 is switched to input direction during LBIST with weak pull-up and pull-down driver disabled (i.e. pad is tri-stated).
- ESR1 is switched to input direction during LBIST with weak pull-down driver enabled.
- Other GPIO pins are switched to input direction with weak pull-up devices either stable active or inactive (depending on LBIST user configuration).

SCU_TC.H010 LBIST Signature Depends on Debug Interface Configuration

The following three cases generate different sets of LBIST MISR signatures:

1. Pin $\overline{\text{TRST}}$ is held high during $\overline{\text{PORST}}$ rising edge (DAP operation): In this case the further values of $\overline{\text{TRST}}$ will have no influence on the MISR signature
2. Pin $\overline{\text{TRST}}$ is held low during $\overline{\text{PORST}}$ rising edge (JTAG operation): $\overline{\text{TRST}}$ is held continuously low also during LBIST operation
3. Pin $\overline{\text{TRST}}$ is held low during $\overline{\text{PORST}}$ rising edge (JTAG operation): $\overline{\text{TRST}}$ is switched to high after $\overline{\text{PORST}}$ has been released and at least one pulse occurred at TCK before LBIST starts.

If DXCM/DXCPL (Debug over CAN) is not needed it is recommended to keep pin $\overline{\text{TRST}}$ always at a high level during $\overline{\text{PORST}}$ rising-edge in the application environment (also in final application). This makes the MISR signature independent from further $\overline{\text{TRST}}$ behavior and still allows debug access via DAP or to completely disable the debug IF via software (by setting OIFM.DAPMODE = 111_B).

In the DXCM/DXCPL enabled case it is recommended to keep pin $\overline{\text{TRST}}$ always at a low level (also after $\overline{\text{PORST}}$ has been released). In this operation case a

different set of MISR signatures will be received (case 2 in above list). Consequently the application software needs to be prepared to accept LBIST MISR signature results from case 1 or from case 2 as pass criteria.

SCU_TC.H013 Correction to Register References in Chapter "Watchdog Timers"

Some references to register names in chapter "Watchdog Timers" of the User's Manual are incorrect.

The corrected references and their section headers are listed in **bold** below.

Section Password Access to WDTxCON0

.. To ensure that a CPU fault could not allow a fault to be ignored an option is provided to prevent watchdog unlocking if the Safety Management Unit (SMU) is not in the RUN state. This option may be enabled by bit **WDTxCON1**.UR.If the password is valid and the SMU state meets the requirements of the **WDTxSR**.US bit then WDTxCON0 will be unlocked as soon as the Password Access is completed. ..

Section Timer Operation

.. The parameter divider represents the user-programmable source clock division selected by **WDTxCON1**.IRx, which can be 64, 256 or 16384.

Section Watchdog Timer Registers

- **WDTSCON1** - Safety WDT Control Register 1:
  - References to WDTxCON0 and WDTxSR should be consequently to **WDTSCON0** and **WDTSSR** in the context of WDTSCON1.
- **WDTCPUxCON1** - CPUx WDT Control Register 1:
  - References to WDTSCON0 and WDTSSR should be consequently to **WDTCPUxCON0** and **WDTCPUxSR** in the context of WDTCPUxCON1.

SCU_TC.H014 Reset Value of Bit Field IOCR.PC1 - Control for Pin $\overline{\text{ESR1}}$

The reset value of register SCU_IOCR is documented as 0000 $20E0_H$ in chapter “Reset Control Units” of the User’s Manual, i.e. the reset value of bit field PC1 = 2_H.

This is not always correct under all circumstances:

The actual SCU_IOCR reset value should be considered as 0000 $X0E0_H$ with the explanations given in the following **Documentation Update**.

Documentation Update

The reset value of bit field SCU_IOCR.PC1 is influenced by pin HWCFG6 and bit PMSWCR0.TRISTREQ:

- When a cold reset is activated and HWCFG6=1 then PC1 is reset to 2_H and pin $\overline{\text{ESR1}}$ will have input pull-up mode.
- If HWCFG6=0 then PC1 is reset to 0_H and $\overline{\text{ESR1}}$ will have tri-state mode.

PC1 and the $\overline{\text{ESR1}}$ reset state can also be configured by software with the PMSWCR0.TRISTREQ bit. PMSWCR0.TRISTREQ is not affected by warm reset or wake-up from standby so the IOCR.PC1 reset value is configured as per the state of the TRISTREQ bit prior to the warm reset.

SENT_TC.H003 First Write Access to Registers FDR and TPD after ENDINIT Status Change

Due to an extra registering stage of the ENDINIT signal from the SCU inside the SENT kernel, the behavior of the first write access to SENT registers FDR and TPD protected by the Endinit write protection scheme after an ENDINIT status change is as follows:

- After unlocking protection (ENDINIT change from 1 to 0), if the first access to the SENT module is a write to FDR or TPD, it will still view ENDINIT as locked (value 1). The contents of FDR or TPD is not changed, but no BCU alarm will be generated, as the ENDINIT does not indicate a protected status in case of the access.
- By setting protection again (ENDINIT change from 0 to 1), if the first access to the SENT module is a write to FDR or TPD, it will still be effective, i.e., the

value will be written. Nevertheless a SMU alarm through BCU will be generated as the protection status is ENDINIT.

Note: After the first read of any SENT register, or first write to any SENT register, the ENDINIT change will be correctly considered for all following accesses. The CLC, KRST0/1 and KRSTCLR registers (that also have Endinit protection) are not affected at all. An initial value of 0 for ENDINIT is seen by SENT after reset before the first access.

Recommendation

After a change of the ENDINIT protection status, first perform a read of any SENT register or a write to a non-Endinit-protected SENT register. The second access is then always equipped with correct information of ENDINIT.

SENT_TC.H004 Short Serial Message - Figure Correction

In Figure “Short Serial Message, Serial Data Encoding over 16 messages” of the SENT chapter, the arrows originating from bits 2 and 3 of the Status & Comm Nibble are routed incorrectly and must be swapped.

Correction

Figure 13 shows a corrected version of this figure.

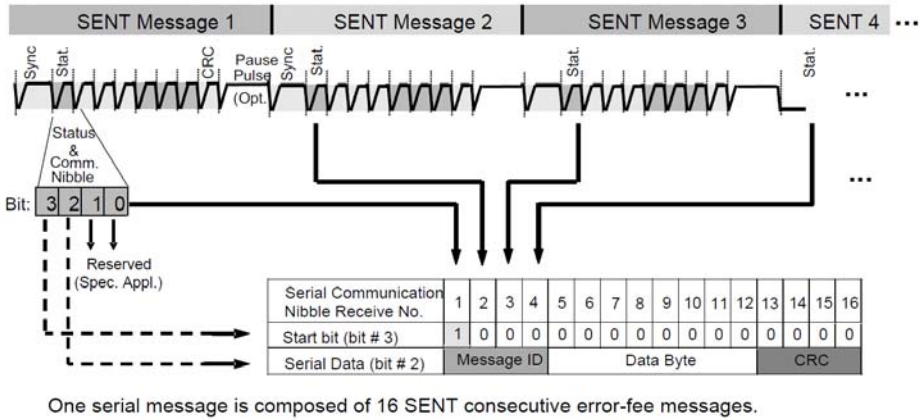

Figure 13 Short Serial Message, Serial Data Encoding over 16 messages

SENT_TC.H005 Interface Connections of the SENT Module - Documentation Correction

The following corrections apply to chapter “Interface Connections of the SENT Module” in the SENT chapter of the User’s Manual:

Figure “SENT Module Implementation and Interconnections”

- In TC23x/TC22x/TC21x, no TRIGOn signals are connected from the SENT module to the Interrupt Router (IR). All references to TRIGOn should be ignored in this figure.
- The range of index n for connected trigger inputs TRIGn in TC23x/TC22x/TC21x is n = 0..3.

Interrupt and DMA Controller Service Requests

In TC23x/TC22x/TC21x, request lines SR0..3 of the SENT module are connected via the Interrupt Router and can be selected in register INPx accordingly. Values ≥ 0100_B are reserved and should not be used for the bit fields in register INPx.

SMU_TC.H001 Write all bit fields of SMU_PCTL with one write access

When configuring the FSP pin (e.g. P33.8), all bit fields (HWDIR, HWEN and PCS) of register SMU_PCTL must be written with the same write access.

Otherwise, when first writing a 1_B to HWEN before writing a 1_B to PCS, the pad configuration will be modified to push/pull configuration before it is latched into field PCFG.

Note: When PCS = 1_B, the bit fields PCFG and PCS are protected against any changes until the next power on reset. HWEN and HWDIR may still be modified by SW, unless locked via register SMU_KEYS.

SMU_TC.H005 Correction to Figure "SMU Register Map"

The start address "@SMU + 0x0E0" for the SMU System Registers shown in the lower part of figure "SMU Register Map" in the SMU chapter of the User's Manual is incorrect.

The correct start address is "@SMU + 0x**7E0**".

Addresses listed in table "Registers Overview" of the SMU chapter are correct.

SMU_TC.H006 Description of Bit EFRST in Register SMU_AGC

In the SMU chapter of the User's Manual, the description of the encoding of bit EFRST (Enable FAULT to RUN State Transition) in register SMU_AGC (Alarm Global Configuration) is missing.

The complete description should be as shown in **Table 35**:

Table 35 Bit EFRST in Register SMU_AGC

Field	Bits	Type	Description
EFRST	29	rw	**Enable FAULT to RUN State Transition** 0_B FAULT to RUN State Transition disabled 1_B FAULT to RUN State Transition enabled See section "**FSP Fault State**" for the usage of this field.

SMU_TC.H007 SPB Bus Control Unit (SBCU) Alarm Signalling to SMU

ALM3[31] is dedicated to System Peripheral Bus (SPB) alarms. As described in table “Alarm Mapping related to ALM3 group” in the SMU chapter of the User’s Manual, an SPB bus error can result from multiple root causes, including protocol violation, incorrect address, register access protection violation.

More details on the SPB related error conditions can be found in the “On-Chip Bus System” chapter:

The SBCU signals an alarm to the SMU whenever it detects

- a SPB transaction that was finished with a Bus Error (Error Acknowledge)
- an un-implemented Address (no slave responds to a transaction request)
- a SPB transaction that was finished by a Time-out.

The alarm signaling to the SMU is independent of the BCU configuration (e.g. BCU interrupt configuration, BCU debug status).

SMU_TC.H009 Alarm Table Corrections

Some alarm tables were unintentionally changed between User's Manual (UM) version V1.0 and V1.1.

In the following, the issues are described and the correct table parts are included.

- **Table 10-2 HwAlarmOut[3:0]: CPU0 DCACHE/DSPR SRAM**

The PreAlarms 1, 3, 5, 7 of the DSPR2 part (TC23x only) were accidentally removed in UM V1.1.

The following **Table 36** copied from UM V1.0 is correct:

Table 36 Table 10-2 HwAlarmOut[3:0]: CPU0 DCACHE/DSPR SRAM

Function
HwAlarmOut[0]= PreAlarm[0=CPU0.DMI.DSPR.(ECC single bit correction)] or PreAlarm[1=CPU0.DMI.DSPR2.(ECC single bit correction)]
HwAlarmOut[1]= PreAlarm[2=CPU0.DMI.DSPR.(ECC uncorrectable error)] or PreAlarm[3=CPU0.DMI.DSPR2.(ECC uncorrectable error)]
HwAlarmOut[3]= PreAlarm[4=CPU0.DMI.DSPR.(Address error)] or PreAlarm[5=CPU0.DMI.DSPR2.(Address error)]
HwAlarmOut[4]= PreAlarm[6=CPU0.DMI.DSPR.(Address buffer overflow)] or PreAlarm[7=CPU0.DMI.DSPR2.(Address buffer overflow)]

- **Table 10-3 HwAlarmOut[7:4]: CPU1 DCACHE/DSPR SRAM**

HwAlarmOut[7:4] are reserved. The following **Table 37** copied from UM V1.0 is correct:

Table 37 Table 10-3 HwAlarmOut[7:4]: CPU1 DCACHE/DSPR SRAM

Function
HwAlarmOut[7:4] are reserved

- **Table 10-4 HwAlarmOut[15:8]: CPU2 SRAMs**

HwAlarmOut[15:8] are reserved. The following **Table 38** copied from UM V1.0 is correct:

Table 38 Table 10-4 HwAlarmOut[15:8]: CPU2 SRAMs

Function
HwAlarmOut[15:8] are reserved

- **Table 10-5 HwAlarmOut[19:16]: GTM SRAMs**

HwAlarmOut[19:16] are reserved. The following **Table 39** copied from UM V1.0 is correct:

Table 39 Table 10-5 HwAlarmOut[19:16]: GTM SRAMs

Function
HwAlarmOut[19:16] are reserved

- **Table 10-7 HwAlarmOut[27:24]: CAN SRAM**

The PreAlarms of the second CAN module RAMs (TC23x only) were accidentally removed in UM V1.1; these are: 81, 83, 85, 87.

The following **Table 40** copied from UM V1.0 is correct:

Table 40 Table 10-7 HwAlarmOut[27:24]: CAN SRAM

Function
HwAlarmOut[24]= PreAlarm[80=CAN.SRAM.MCAN0.(ECC single bit correction)] or PreAlarm[81=CAN.SRAM.MCAN1.(ECC single bit correction)]
HwAlarmOut[25]= PreAlarm[82=CAN.SRAM.MCAN0.(ECC uncorrectable error)] or PreAlarm[83=CAN.SRAM.MCAN1.(ECC uncorrectable error)]
HwAlarmOut[26]= PreAlarm[84=CAN.SRAM.MCAN0.(Address error)] or PreAlarm[85=CAN.SRAM.MCAN1.(Address error)]
HwAlarmOut[27]= PreAlarm[86=CAN.SRAM.MCAN0.(Address buffer overflow)] or PreAlarm[87=CAN.SRAM.MCAN1.(Address buffer overflow)]

- **Table 10-8 HwAlarmOut[31:28]: LMU sub-system SRAMs**

The PreAlarms of the FFT RAMs (TC23x ADAS only) were accidentally removed in UM V1.1; these are: 230, 231, 233, 234, 236, 237, 239, 240.

The following **Table 41** copied from UM V1.0 is correct:

Table 41 Table 10-8 HwAlarmOut[31:28]: LMU sub-system SRAMs

Function
HwAlarmOut[28]= PreAlarm[88=LMU.DAM.SRAM(ECC single bit correction)] or PreAlarm[230=LMU.FFT0.SRAM(ECC single bit correction)] or PreAlarm[231=LMU.FFT1.SRAM(ECC single bit correction)] or
HwAlarmOut[29]= PreAlarm[90=LMU.DAM.SRAM(ECC uncorrectable error)] or PreAlarm[233=LMU.FFT0.SRAM(ECC uncorrectable error))] or PreAlarm[234=LMU.FFT1.SRAM(ECC uncorrectable error))] or
HwAlarmOut[30]= PreAlarm[92=LMU.DAM.SRAM(Address error)] or PreAlarm[236=LMU.FFT0.SRAM(Address error)] or PreAlarm[237=LMU.FFT1.SRAM(Address error)] or
HwAlarmOut[31]= PreAlarm[94=LMU.DAM.SRAM(Address buffer overflow)] or PreAlarm[239=LMU.FFT0.SRAM(Address buffer overflow)] or PreAlarm[240=LMU.FFT1.SRAM(Address buffer overflow)] or

- **Table 10-9 HwAlarmOut[34:32]: SRI Agents**

PreAlarm[116] is accidentally listed as HSSL.SRI_MASTER(SRI Read Data Phase Error) in UM V1.1.

Actually PreAlarm[116] is reserved.

- **Table 9-11 HwAlarmOut[44:41]: Misc. SRAMs**

The PreAlarms accidentally listed as assigned to PSI5 and CIF are actually reserved; these are 145, 147-149, 153, 155-157, 161, 163-165, 169, 171-173.

- **Table 10-12 HwAlarmOut[45]: Watchdogs Timeout**

The PreAlarms accidentally listed as assigned to WDTCPU1 and WDTCPU2 in UM V1.1 are actually reserved; these are 175, 176.

- **Table 10-13 HwAlarmOut[50:46]: PMU Alarms**

The PreAlarms accidentally listed as assigned to PFLASH1 in UM V1.1 are actually reserved; these are: 179, 187, 195, 203, 211.

- **Table 10-18 TC21x/TC22x/TC23x Alarm Mapping related to ALM1 Group**

This table incorrectly shows alarms for CPU1 in UM V1.1.

These alarms actually are reserved, as shown in the following **Table 42** copied from UM V1.0:

Table 42 Table 10-18 Alarm Mapping related to ALM1 Group

Alarm Index	Module	Description
ALM1[31:0]	Reserved	Reserved

- **Table 10-20 TC21x/TC22x/TC23x Alarm Mapping related to ALM3 Group**

The rows in the following **Table 43** replace the corresponding rows of the table in UM V1.1:

Table 43 Part of Table 10-20 with corrected ALM3 Group Mapping

Alarm Index	Module	Description
ALM3[9]	Reserved	Reserved
ALM3[13]	Reserved	Reserved
ALM3[14]	Reserved	Reserved
ALM3[19]	Reserved	Reserved
ALM3[20]	Reserved	Reserved

Table 43 Part of Table 10-20 with corrected ALM3 Group Mapping

Alarm Index	Module	Description
ALM3[27]	**Registers**	**Safety Mechanism: Register Monitor Alarm: register error detection**
ALM3[28]	SCU/LSCU	Safety Mechanism: Lockstep Dual Rail Monitor Alarm: dual rail error Note: monitors the dual-rail property (inverted signals) from the lockstep comparator unit (LSCU) alarms.

- **Table 10-21 TC21x/TC22x/TC23x Alarm Mapping related to ALM4 Group**

There are no GTM SRAMs in this device. The rows in the following **Table 44** replace the corresponding rows of the table in UM V1.1:

Table 44 Part of Table 10-21 with corrected ALM4 Group Mapping

Alarm Index	Module	Description
ALM4[3:0]	Reserved	Reserved
ALM4[7:4] connects to pre-alarms specified by table “HwAlarmOut[27:24]: CAN SRAM”		

- **Table 10-23 TC21x/TC22x/TC23x Alarm Mapping related to ALM6 Group**

This table incorrectly shows alarms for CPU2 in UM V1.1.

These alarms actually are reserved, as shown in the following **Table 45** copied from UM V1.0:

Table 45 Table 10-23 Alarm Mapping related to ALM6 Group

Alarm Index	Module	Description
ALM6[31:0]	Reserved	Reserved

SMU_TC.H010 Clearing individual SMU flags: use only 32-bit writes

The SMU registers shall only be written via 32-bit word accesses (i.e. ST.W instruction), as mentioned in table “Registers Overview” of the SMU chapter in the User’s Manual.

If any other instruction such as LDMST or SWAPMSK.W is used to modify only a few bits in the 32-bit register, then this may have the effect of modifying/clearing unintended bits.

Recommendation (Examples in C Language)

- **Example 1**: To clear status flag SF2 in register AG0, use:
  - SMU_AG0.U = 0x0000 0004;
- **Example 2**: To clear status flags EF2 in register RMEF and RMSTS, use:
  - SMU_RMEF.U = 0xFFFF FFFB;
  - SMU_RMSTS.U = 0xFFFF FFFB;

Here the <REGISTER>.U implies writing to the register as an unsigned integer, which normally results in a compiler translation into an ST.W instruction.

Safety Considerations

As long as software uses only 32-bit writes to the SMU registers, there is no risk of malfunction.

In case the software does not use 32-bit writes (and for example uses bit-wise operations such as LDMST instructions instead) – then potentially unintended flags may be written and modified in the SMU registers. Depending on the application, this may potentially have an impact on safety and/or diagnostics.

Note: The SMU reaction itself (e.g. alarm action triggering) is not affected even if the software unintentionally clears additional bits by not using a 32-bit write as recommended.

SRI_TC.H001 Using LDMST and SWAPMSK.W instructions on SRI mapped Peripheral Registers (range 0xF800 0000-0xFFFF FFFF)

The LDMST and SWAPMSK.W instructions in the AURIX™ microcontrollers are intended to provide atomicity as well as bit-wise operations to a targeted

memory location or peripheral register. They are also referred to as Read-Modify-Write (RMW) instructions.

The bit-manipulation functionality is intended to provide software a mechanism to write to individual bits in a register, without affecting other bits. The bits to be written can be selected via a mask in the instruction. Please refer to the TriCore Architecture Manual for further information about these instructions and their formats.

Restrictions for SRI mapped Peripherals

The bit-manipulation functionality is supported only on registers accessed via the SPB bus, and is not supported on the SRI mapped peripheral range (i.e. address range 0xF800 0000 to 0xFFFF FFFF, including (if available) EBU, PMU0, SRI Crossbar, LMU, DAM, FFT, CPUx SFRs and CSFRs, MCDS, miniMCDS); see table “On Chip Bus Address Map of Segment 15” in chapter “Memory Map”).

On the SRI mapped peripherals, usage of these instructions always results in all the bits of a register being written, and not just specific individual bits.

Note: The instructions are still executed atomically on the bus – i.e the SRI is locked between the READ and the WRITE transaction.

STM_TC.H001 Effect of kernel reset on interrupt outputs STMIR0/1

The clock ratio $f_{STM} : f_{SPB}$ is determined by the settings of bit fields STMDIV and SPBDIV in registers CCUCON1 and CCUCON0, respectively.

If $f_{STM} \leq f_{SPB}$, and a kernel reset of the STM module is performed in the same clock cycle where a compare match of the STM with the CMP0 or CMP1 registers occurs, a transition on the interrupt outputs STMIR0 or STMIR1 may occur. This may e.g. trigger the External Request Unit (ERU), or set the corresponding Service Request flags SRC_STMmSR0.SRR or SRC_STMmSR1.SRR in the Interrupt Router (m = 0, 1, 2, depending on number of CPUs).

Note: For $f_{STM} > f_{SPB}$, this effect will not occur.

Recommendation

If $f_{STM} \leq f_{SPB}$, set bits ICR.CMP0EN = 0_B and ICR.CMP1EN = 0_B to disable the compare match interrupts before performing the STM kernel reset.

STM_TC.H002 Access Protection for STM Control Registers

The access protection symbol ‘P’ to indicate Access Enable Register protection is missing in table “Registers Overview - STM Control Registers” of the STM chapter in the User’s Manual for the STM registers CMP0, CMP1, CMCON, ICR, ISCR.

The STM registers CMP0, CMP1, CMCON, ICR, ISCR actually have protection via the Access Enable registers (ACCEN0/1), as shown in the following Table 46.

Table 46 Correction to Table Registers Overview - STM Control Registers

Short Name	Description	Offset Addr.	Access Mode		Reset
			Read	Write	
CMP0	Compare Register 0	30_H	U, SV	U, SV, P	Application
CMP1	Compare Register 1	34_H	U, SV	U, SV, P	Application
CMCON	Compare Match Control Register	38_H	U, SV	U, SV, P	Application
ICR	Interrupt Control Register	$3C_H$	U, SV	U, SV, P	Application
ISCR	Interrupt Set/Clear Register	40_H	U, SV	U, SV, P	Application