1321TH
13 GHz Bandwidth 2 GS/s THA
Datasheet

Applications

- Test instrumentation equipment, ATE
- RF demodulation systems
- Radar
- Software radio
- Digital receiver systems
- High-speed DAC deglitching
- THA for differential ADCs
- Digital sampling oscilloscopes

Features

- Supports 2 GS/s sampling rate
- 13 GHz input bandwidth (small-signal)
- 10 GHz input bandwidth (0.5 Vpp)
- 8 GHz input bandwidth (1 Vpp)
- THD < -60 dB (1 GHz 1 Vpp input)
- THD < -35 dB (10 GHz 0.5 Vpp input)
- Ultralow aperture jitter: < 50 fs
- 0 dB Gain with up to 1 Vpp out
- Differential master-slave architecture
- Multiple clock modes
- Fast rise time: < 25 ps (10 – 90%)
- Adjustable input termination voltage
- Single -5.2 V power supply
- Low power consumption: 1400 mW
- Available in 4 mm square QFN package
- Evaluation kit available

Description

The 1321TH track-and-hold amplifier is designed for high-precision sampling of wideband signals with multi-GHz frequency content. The master-slave architecture integrates two track-and-hold (T/H) circuits, clock mode selection logic, and a 50-ohm, differential, output buffer.

Sample rates up to 2 GS/s are supported. Clock modes include out-of-phase master-slave (M/S) clocking based on a single clock signal and independent M/S clocking based on two clock signals. The output is settled for nearly a complete clock cycle of the slave T/H.

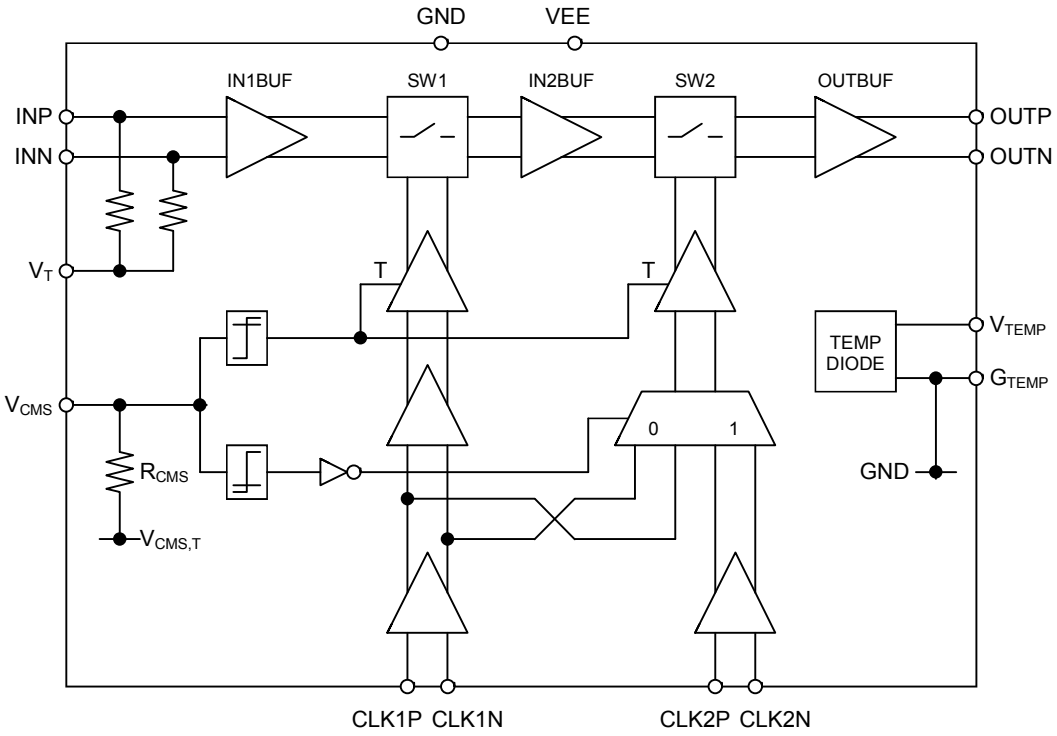
Analog inputs are dc-coupled and terminated on chip with 50 ohms to a user-adjustable voltage. The 1321TH can be driven single-ended or differentially and provides differential outputs.

An output buffer provides 0 dB overall THA gain and up to 1 Vpp differential output swing into a 50 ohm load. The differential clock inputs are dc-coupled and terminated through 50 ohms to ground.

Because of its low power dissipation and low thermal resistance, the 1321TH does not normally require a heatsink when operated at a case temperature up to the maximum case temperature of 85 °C.

The 1321TH operates from a single -5.2 V power supply. It is available in a 4 mm square QFN package. It is also available on an evaluation board with SMA connectors.

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min	Max	Unit
Power Supply Voltage	V_{EE}		-6	0.5	V
RF Input Signals[1]		Terminated to V_T on-Chip	max(-2, -2.5+V_T)	min(1, 2.5+V_T)	V
RF Output Signals			-2	1	V
Input Termination Voltage[2]	V_T		max(-4 –2$V_{IN,MIN}$, -5 +2$V_{IN,MAX}$)	min(2 –2$V_{IN,MAX}$, 5 +2$V_{IN,MIN}$)	V
Clock Mode Select Voltage	V_{CMS}		V_{EE} – 0.3	0.3	V
Junction Temperature - Die	T_J		-5	+175	°C
Case Temperature – Package paddle	T_C		-15	+125	°C
Shipping/Storage Temperature	T_{STORE}		-40	+125	°C
Humidity	R_H		0	100	%
ESD Protection (HBM)	ESD	All, Except Analog Inputs	500	---	V
		Analog Inputs	100	---	V

Notes:

[1] RF input signals, INp and INn, are terminated on-chip with 50 Ω to V_T. The stated min and max values ensure INp and INn between -2 and +1 V, and limit their pin currents to 50 mA.

[2] The V_T min and max values depend on the RF input signal levels, which should be driven from a 50 Ω source. $V_{IN,MIN}$ ($V_{IN,MAX}$) is the minimum (maximum) expected INp or INn voltage, assuming 50 Ω to GND termination. The stated V_T voltage min and max values ensure INp and INn between -2 and +1 V and limit their pin currents to 50 mA.

Test Levels

Test Level (TL)	Test Procedure
1	100% Production tested at V_{EE} = -5.2 V, T_C = 25 °C. Characterization sample tested over V_{EE}, T_C operating conditions
2	Characterization sample tested over V_{EE}, T_C operating conditions
3	Guaranteed by design and/or characterization testing
4	Typical value only, based on simulations.

Operating Conditions

Parameter	Symbol	Conditions	TL	Min	Typ	Max	Unit
Power Supply Voltage	V_{EE}	± 5% Tolerance	---	-5.45	-5.2	-4.95	V
Supply Current	I_{EE}		1	---	275	---	mA
On-Chip Power Dissipation	P_D		1	---	1.4	---	W
Operating Temperature (Junction) - Die	T_J		---	15	---	+125	°C
Operating Temperature (Case) - Package	T_C	package paddle	---	-5	---	+85	°C
Thermal Resistance	R_{JC} (θ_{JC})		---	---	20	---	°C/W

Electrical Specifications: RF I/O

WARNING – To prevent damage to the part:

- DC power must be turned off prior to connecting or disconnecting any cables.

Electrical specifications guaranteed when the part is operated within the specified operating conditions							
Parameter	**Symbol**	**Conditions**	**TL**	**Min**	**Typ**	**Max**	**Unit**
Full Scale Range	FSR	Single-Ended	4	---	500	---	mVpp
		Differential	4	---	1000	---	mVpp
Input High Level[1]	V_{IH}		2	0.5	---	---	V
Input Low Level[1]	V_{IL}		2	---	---	-0.5	V
Input Return Loss	RL_{IN}	Up to 8 GHz	2	10	---	---	dB
Clock Amplitude		Single-Ended	2	300	---	600	mVpp
		Differential	2	300	---	1200	mVpp
Clock Input High Level	V_{CH}		2	0.5	---	---	V
Clock Input Low Level	V_{CL}		2	---	---	-1	V
Clock Input Return Loss	RL_{CLK}	Up to 5 GHz	2	15	---	---	dB
Output Termination Voltage	$V_{OUT,T}$		2	0	0	1	V
Output Common Mode Voltage[2]	$V_{OUT,CM}$	Into 50 Ω to $V_{OUT,T}$	3	---	-0.55 + 0.58 $V_{OUT,T}$	---	V
Output Return Loss	RL_{OUT}	Up to 5 GHz	2	15	---	---	dB
Gain	A_V	50-Ω I/O Environment	1	0.95	1	1.05	
Gain Drift	$\partial A_V/\partial T$		2	---	240	---	ppm/°C
Offset	V_O	Differential, Input Referred	2	---	---	±10	mV
Offset Drift	$\partial V_O/\partial T$	Differential, Input Referred	2	---	10	---	uV/°C

Notes:

[1] For inputs that are not centered (common mode level) close to GND, set V_T so that the input voltages are within the V_{IL}, V_{IH} range. The V_T input must be connected to GND or a DC supply that is well bypassed to GND. For GND-centered inputs, connect V_T to GND.

[2] Outputs are resistively terminated to GND on chip. $V_{OUT,T}$ is the voltage used to terminate the outputs at the far end of the transmission line. The $V_{OUT,T}$ range allows adjustment of $V_{OUT,CM}$ (output common mode level) from -550 mV to about +30 mV.

Electrical Specifications: DC I/O

WARNING – To prevent damage to the part:

- DC power must be turned off prior to connecting or disconnecting any cables.

Electrical specifications guaranteed when the part is operated within the specified operating conditions							
Parameter	**Symbol**	**Conditions**	**TL**	**Min**	**Typ**	**Max**	**Unit**
Clock Mode Select Voltage[1]	V_{CMS}	**Full Track Mode**: TH1 and TH2 in Track Mode; CLK1 and CLK2 Ignored	3	-0.5	---	0	V
		CLK1 Mode: CLK1 clocks TH1 and TH2, out-of-phase; CLK2 Ignored	3	V_{EE} + 2	---	-2	V
		CLK1&2 Mode: CLK1 clocks TH1, CLK2 clocks TH2	3	V_{EE}	---	V_{EE} + 0.5	V
Clock Select Termination Voltage[2]	$V_{CMS,T}$		3	---	$0.5V_{EE}$	---	V
Clock Select Input Resistance	R_{CMS}	To $V_{CMS,T}$. V_{EE}-0.5 < V_{CMS} < 0.5 V	3	---	3	---	kΩ

Notes:

[1] V_{CMS} selects one of three clock modes. Full track mode is useful for test purposes. CLK1 mode is the easiest to use since only one clock signal is required. CLK1&2 mode allows sub-sampling by N of the TH1 output by choosing $f_{CLK2} = f_{CLK1} / N$. A high CLK1 frequency may be optimal for lowest clock jitter while a low CLK2 frequency may allow reduced speed requirements on subsequent circuitry, such as an ADC.

[2] Internally generated voltage. For V_{EE} = -5.2V, $V_{CMS,T}$ = -2.6V. If the CMS pin is open, V_{CMS} defaults to $V_{CMS,T}$. This results in the CLK1 mode being selected.

Electrical Specifications: Dynamic

WARNING – To prevent damage to the part:

- DC power must be turned off prior to connecting or disconnecting any cables.

Electrical specifications guaranteed when the part is operated within the specified operating conditions							
Parameter	**Symbol**	**Conditions**	**TL**	**Min**	**Typ**	**Max**	**Unit**
Bandwidth, Small-Signal	bw	-3dB Gain, 0.1 Vpp Input	2	---	13	---	GHz
Bandwidth, Half-Scale Signal		-3dB Gain 0.5 Vpp Input	2	---	10	---	GHz
Bandwidth, Large-Signal	BW	-3dB Gain 1 Vpp Input	2	---	8	---	GHz
Gain Flatness Deviation		Up to 10 GHz	2	---	---	±0.5	dB
Master T/H Hold Feedthrough[1]	$A_{TH1,HOLD}$	1 GHz 1 Vpp Input	2	---	-65	---	dB
Total Harmonic Distortion[2]	THD	1 GHz 1 Vpp Input	1	---	-60	---	dB
		2 GHz 1 Vpp Input	2	---	-55	---	dB
		3 GHz 1 Vpp Input	2	---	-50	---	dB
		5 GHz 1 Vpp Input	2	---	-40	---	dB
		10 GHz 1 Vpp Input	2	---	-25	---	dB
		1 GHz 0.5 Vpp Input	2	---	-70	---	dB
		2 GHz 0.5 Vpp Input	1	---	-60	---	dB
		3 GHz 0.5 Vpp Input	2	---	-55	---	dB
		5 GHz 0.5 Vpp Input	2	---	-45	---	dB
		10 GHz 0.5 Vpp Input	2	---	-35	---	dB
		5 GHz 0.25 Vpp Input	2	---	-50	---	dB
		10 GHz 0.25 Vpp Input	1	---	-45	---	dB
		5 GHz 0.1 Vpp Input	2	---	-55	---	dB
		10 GHz 0.1 Vpp Input	1	---	-50	---	dB

Notes:

[1] In dB: $A_{TH1,HOLD}$ = -(TH1 isolation). Since the TH1 track mode gain is close to unity, $A_{TH1,HOLD}$ can be measured and is the ratio of the TH gain with TH1 in hold mode to the TH gain with TH1 in track mode (TH2 is in track mode).

[2] This is the THD for a single-ended output with a differential input. Both outputs are terminated with 50 □ to $V_{OUT,T}$. The THD for a differential output is lower than the THD for a single-ended output.

Electrical Specifications: TH1 Switching

WARNING – To prevent damage to the part:

- DC power must be turned off prior to connecting or disconnecting any cables.

Electrical specifications guaranteed when the part is operated within the specified operating conditions							
Parameter	**Symbol**	**Conditions**	**TL**	**Min**	**Typ**	**Max**	**Unit**
Aperture Delay[1]	t_A	After $V_{CLK1P} - V_{CLK1N}$ goes positive	4	---	55	---	ps
Aperture Delay Drift	$\partial t_A/\partial T$		4	---	+25	---	fs/°C
Aperture Jitter	Δt	Jitter Free 2 GHz 0.5 Vpp CLK1 Signal	3	---	50	---	fs
Settling Time[1,2]	t_S	After $V_{CLK1P} - V_{CLK1N}$ goes positive to 1 mV at Hold Capacitors, $t_{TRACK1,MIN}$, Observed	4	---	50	---	ps
Differential Pedestal/ V_{IN}			4	---	±0.25	---	%
Differential Droop Rate/ V_{IN}[3]		Hold Mode	4	---	-0.2	---	%/ns
Differential Drift Rate[3]		Hold Mode	4	---	±0. 5	---	mV/ns
Maximum Hold Time[4,5]	$t_{HOLD1,MAX}$		3	25	---	---	ns
Minimum CLK1 Frequency[4]	$f_{CLK1,MAX}$	50% Duty Cycle Clock	2	---	---	20	MHz
Maximum CLK1 Frequency[4]	$f_{CLK1,MAX}$	50% Duty Cycle Clock	2	2000	---	---	MHz
Acquisition Time[1]	t_{ACQ}	After $V_{CLK1P} - V_{CLK1N}$ goes negative to 1 mV at Hold Capacitors, FSR Input Step	4	---	100	---	ps
Maximum Acquisition Slew Rate	$(\partial V/\partial t)_{MAX}$	At Hold Capacitors, FSR Input Step	4	---	25	---	V/ns
Rise Time[6]	t_R	10 – 90%, 0 to FSR/2 Input Step	3	---	15	25	ps
Minimum Track Time	$t_{TRACK1,MIN}$		4	---	200	---	ps

Notes:

[1] The $V_{CLK1P} - V_{CLK1N}$ positive (rising) edge is the TH1 hold command. It causes the TH1 circuit to transition from the track mode to the hold mode. The $V_{CLK1P} - V_{CLK1N}$ negative (falling) edge is the TH1 track command. It causes the TH1 circuit to transition from the hold mode to the track mode.

[2] For a 0.5Vpp input step with a 25ps (10-90%) rise time. Measured from the time at which the mid-level slope line of the hold capacitor voltage signal crosses the final value to the time at which the hold capacitor voltage signal is within 1mV of its final value. Observed in the time-reconstructed output signal of a sampled, repetitive step signal.

[3] The time variation of the differential output voltage, V_{OUT}, with TH1 in hold mode and TH2 in track mode, is:

dV_{OUT}/dt = TH1 Drift Rate + V_{OUT} x TH1 Droop Rate.

[4] The slew rate of the track-to-hold clock transition should be 1 V/ns or higher for best performance.

[5] The hold time is limited by differential droop, which causes an exponential decay of the differential signal. No recovery time is required after any hold duration. The maximum hold time is defined here as the time at which the differential signal loss is 5% of its initial held value.

[6] Measured as $\sqrt{(t_{rise,cap}^2 - t_{rise,input}^2)}$, where $t_{rise,input}$ is the 10-90% rise time of the input signal and $t_{rise,cap}$ is the 10-90% rise time of the hold capacitor signal. The rise time $t_{rise,cap}$ is equal to that of the time-reconstructed output signal of a sampled repetitive step signal with rise time $t_{rise,input}$.

Electrical Specifications: TH2 Switching

WARNING – To prevent damage to the part:

- DC power must be turned off prior to connecting or disconnecting any cables.

Electrical specifications guaranteed when the part is operated within the specified operating conditions							
Parameter	**Symbol**	**Conditions**	**TL**	**Min**	**Typ**	**Max**	**Unit**
Aperture Delay	t_{A2}	After $V_{CLK2P} - V_{CLK2N}$ goes positive in CLK1&2 Mode. After $V_{CLK1P} - V_{CLK1N}$ goes negative in CLK1 Mode	4	---	45	---	ps
Aperture Delay Drift	$\partial t_{A2}/\partial T$		4	---	+25	---	fs/°C
Settling Time[1]	t_{S2}	After $V_{CLK2P} - V_{CLK2N}$ goes positive in CLK1&2 Mode. After $V_{CLK1P} - V_{CLK1N}$ goes negative in CLK1 Mode. To 1 mV at Hold Capacitors, $t_{TRACK2,MIN}$, Observed	4	---	60	---	ps
Differential Pedestal / V_{IN}			4	---	±0.25	---	%
Differential Droop Rate / V_{IN}[2]			4	---	-0.1	---	%/ns
Differential Drift Rate[2]		Hold Mode	4	---	±0. 5	---	mV/ns
Maximum Hold Time[3]	$t_{HOLD2,MAX}$		3	50	---	---	ns
Minimum CLK2 Frequency	$f_{CLK2,MAX}$	50% Duty Cycle Clock	2	---	---	10	MHz
Maximum CLK2 Frequency	$f_{CLK2,MAX}$	50% Duty Cycle Clock	2	2000	---	---	MHz
Minimum Track Time	$t_{TRACK2,MIN}$	After TH1 in Hold Mode	4	---	200	---	ps

Notes:

[1] For a 0.5 Vpp step between subsequent TH1 output levels. Measured from the time at which the mid-level slope line of the hold capacitor voltage signal crosses its final value to the time at which the hold capacitor voltage signal is within 1 mV of its final value.

[2] The time variation of the differential output voltage, V_{OUT}, with TH1 in any mode and TH2 in hold mode, is:

dV_{OUT}/dt = TH2 Drift Rate + V_{OUT} x TH2 Droop Rate.

[3] The hold time is limited by differential droop, which causes an exponential decay of the differential signal. No recovery time is required after any hold duration. The maximum hold time is defined here as the time at which the differential signal loss is 5% relative to its initial held value.

Typical DC Operating Characteristics

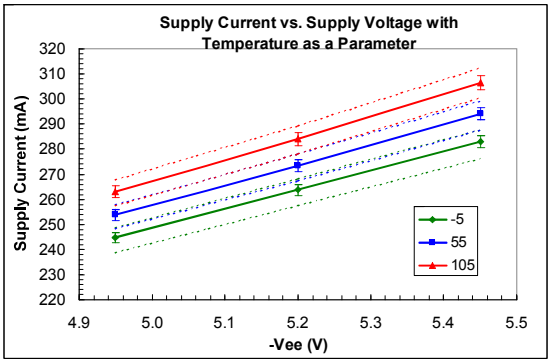


Figure 1. Measured power supply current vs. power supply voltage for 23 devices.

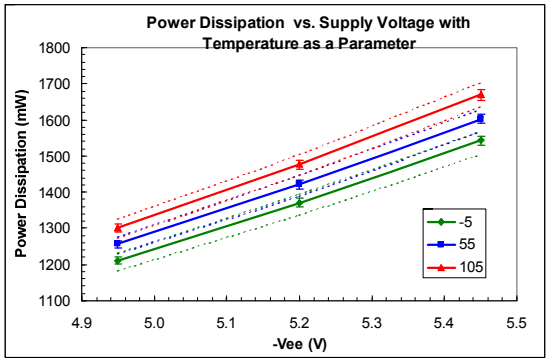


Figure 2. Measured power dissipation vs. power supply voltage for 23 devices.

V_T Pin Description

The voltage V_T sets the analog input termination voltage. This increases the range of signals that can be accurately sampled by adjusting their common-mode level at the THA inputs. Consider a differential input signal that has a 50 Ω source impedance and a non-zero common-mode level (V_{COM}) when terminated into 50 Ω to ground. By setting V_T to -2 X V_{COM}, the common-mode level at the THA input pins is made zero. This feature can be used to adjust the input signal range to be within the specified input signal range for the THA. This can also be used for single-ended input signals, as illustrated by the following examples.

Consider first a differential signal with negative, CML signal levels of -400 mV and 0 V on each side when terminated into 0 V (V_T=GND). The V_{COM} level of this differential signal is -200 mV. Adjusting V_T from 0 V to +400 mV results in a 0 V V_{COM} level at the THA, analog input pins. Although the -200 mV original V_{COM} level would be acceptable for the THA, this example shows the principle that can be applied to signals with larger positive or negative, V_{COM} levels.

Consider a single-ended, negative CML signal connected to INp with a V_{COM} level of -200 mV when terminated to GND. For optimal differential operation, the INn input should also be forced to -200 mV DC. If we set V_T to +400 mV, the INp V_{COM} level becomes 0 V. In this case, since INn is terminated to V_T through 50 Ω, the INn V_{COM} level will be at +400 mV (V_T) if left disconnected. INn should be forced to 0 V either by connecting it through 50 Ω to -400 mV or by shorting it to GND.

The V_T is well by-passed to GND on the die and in the package. Therefore, the analog inputs are AC terminated to GND. For proper DC termination V_T must be connected to either a DC supply or to GND. In general, V_T may be forced to any value between 0 and +1 V. Please see Maximum Ratings section.

V_{CMS} Pin Description

V_{CMS} is the clock mode select voltage. V_{CMS} digitally selects one of three clock modes for the two internal track-and-holds, TH1 and TH2. If left open, V_{CMS} by default assumes a level $V_{CMS,M}$ and CLK1 clocks both TH1 and TH2, out-of-phase. If forced low (V_{EE}), CLK1 clocks TH1 and CLK2 clocks TH2. If forced high (GND), both TH1 and TH2 are put into track mode and both CLK1 and CLK2 are ignored. For the voltage level ranges corresponding to the three states, see the I/O Electrical Specifications.

V_{TEMP} and G_{TEMP} Pins Description

The V_{TEMP} and G_{TEMP} pins can be used to measure the chip temperature. The G_{TEMP} pin connects to GND on the chip and may serve as an extra GND connection when not used for temperature measurement. The V_{TEMP} pin connects to G_{TEMP} through a parallel combination of two circuits. Circuit 1 is a series combination of two diodes, connected in the forward direction. Circuit 2 is a series combination of two similar diodes, connected in the reverse direction. V_{TEMP} does not connect to the rest of the IC in any other way. Although the GTEMP pin connects to GND on the chip, the connecting metal from G_{TEMP} to the diode combinations is routed so that it conducts only the diode currents and no current for the rest of the IC. Therefore, the G_{TEMP} voltage accurately reflects the voltage at the diode terminals that connect to G_{TEMP}. Since V_{TEMP} only connects to the diode circuits, it is routed such that the voltage drop along the V_{TEMP}, on-chip, routing is very small. These techniques are similar to the ones used in Kelvin probing.

When forcing a positive current of 0.5 mA, from GTEMP to VTEMP, the voltage difference VTEMP – GTEMP will be about 1.2 V at room temperature and will depend on the temperature of the two forward series diodes that conduct the current. The reverse biased series diodes conduct negligible current. Both sets of diodes are located near the output buffer's active circuitry. The reverse diodes allow the same type of temperature measurement to be performed. For a current of -0.5 mA, from GTEMP to VTEMP, the voltage difference VTEMP – GTEMP will be -1.2 V. The user thus has the option of measuring a positive or a negative voltage relative to GND.

A calibration voltage vs. temperature curve for a fixed current may be obtained by measuring the voltage while changing the IC temperature in a controlled manner with the IC powered off.

I/O Equivalent Circuits

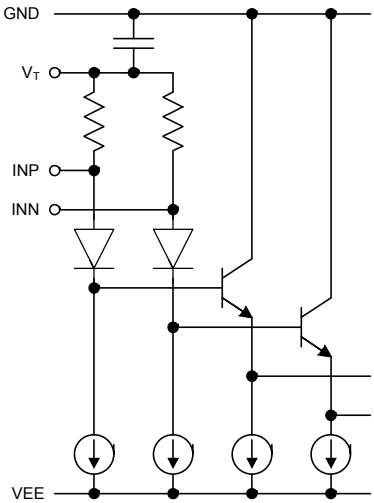


Figure 3. Simplified analog input structure.

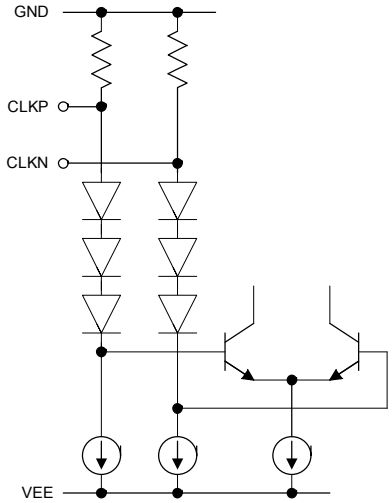


Figure 4. Simplified Clock1 and Clock2 input structure.

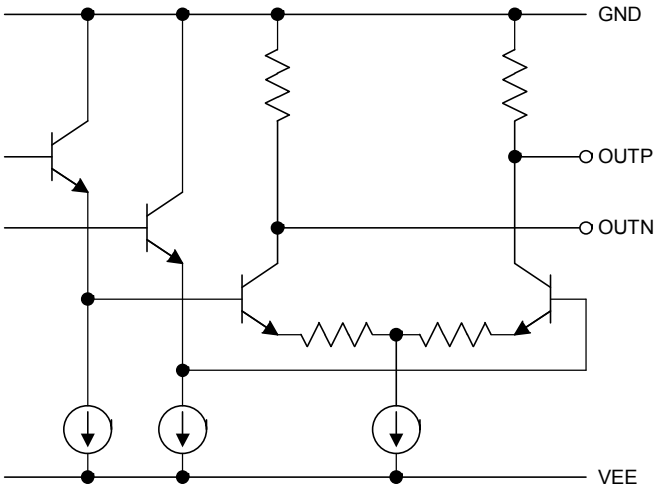
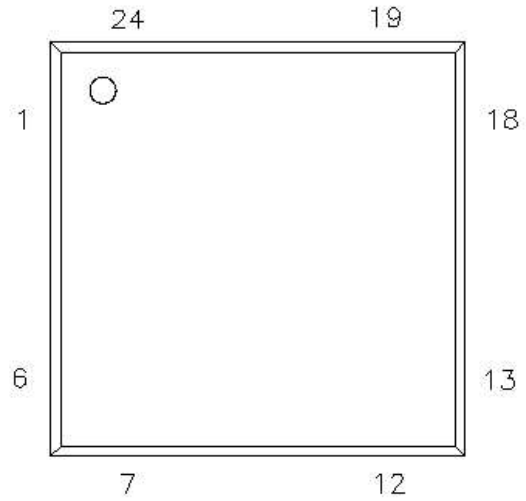
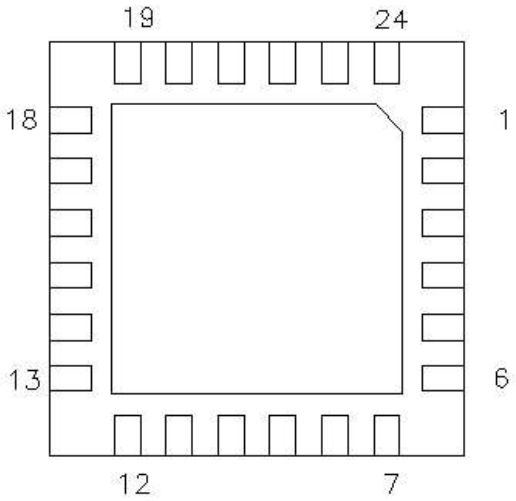


Figure 5. Simplified analog output structure.

4 mm QFN Pinout Information



Top View



Bottom View

Name	Pin	Description	Function
INp, INn	3, 5	Analog Inputs	Input
OUTp, OUTn	16, 14	Analog Outputs	Output
CLK1p, CLK1n	8, 9	Clock 1 Inputs	Input
CLK2p, CLK2n	11, 12	Clock 2 Inputs	Input
V_T	24	Termination Voltage for Analog Inputs	Input
V_{CMS}	23	Clocking Mode Select	Digital Input
V_{TEMP}	19	Temperature Diode Voltage	Input
G_{TEMP}	18	Ground Sense Voltage for Temperature Diode	Output
V_{EE}	20, 22	Power Supply: Connect to –5.2 V	Supply
GND	2, 4, 6, 7, 10, 13, 15, 17, 21, paddle	Ground	Supply
NC	1	No Internal Connection	NC

4 mm QFN Package Outline Drawing

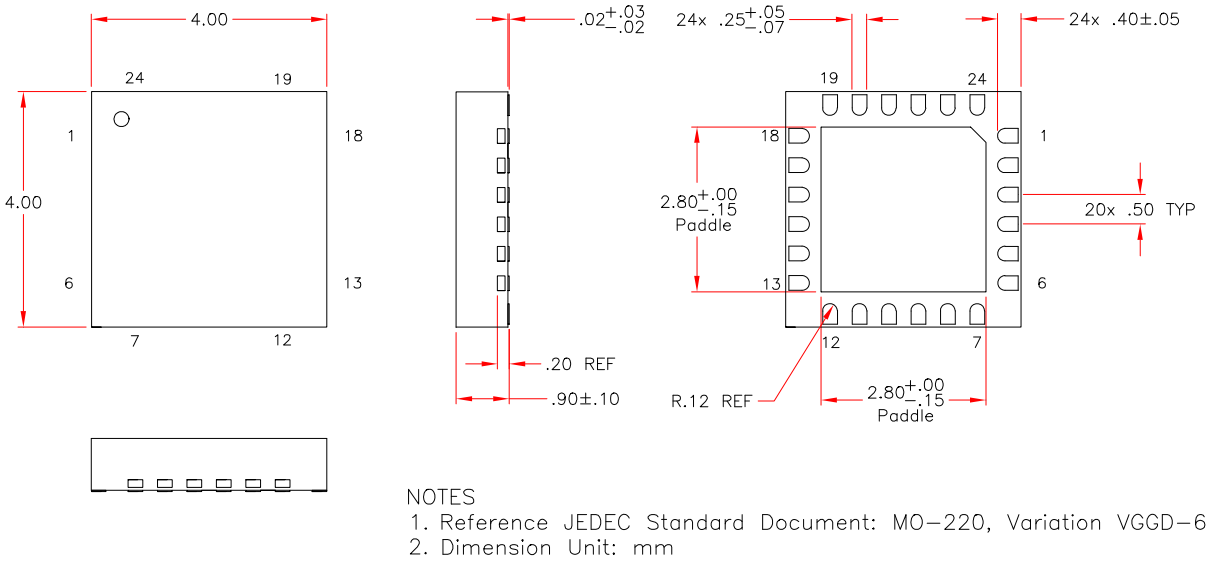


Figure 6. 4x4 mm QFN package.

Order Information

Part No.	Description
1321TH-S01QFN	2 GS/s Track and Hold Amplifier in a 24 pin QFN package
1321TH -S01QFNEVB	2 GS/s Track and Hold Amplifier in a 24 pin QFN package on an Evaluation Board with SMA Connectors

Contact Information

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Qualification Notification

The 1321TH is fully qualified. Please contact Inphi for the qualification report.

Inphi Corporation will honor the full warranty as outlined in Section 5 of Inphi's Standard Customer Purchase Order Terms and Conditions.

Version Updates

Version 1.0 (dated 4/20/06)

Initial Release

From Version 1.0 to 1.1 (dated 2009-12-16)

1. Removed "Preliminary" watermark throughout document.
2. Added 1321TH product photo (page 1).
3. Deleted the Temperature Diode Voltage parameter in the Absolute Maximum Ratings section (page 3).
4. Changes to Operating Conditions table (page 3):
    a. IEE typical spec from 250 mA to 275 mA.
    b. Power Dissipation typical spec from 1.3 to 1.4 W.
    c. Changed the Thermal Resistance (θ_{JC}) typical spec from "TBD" to 20 °C/W.
5. Removed the Input and Clock Resistance specs from Electrical Specifications: RF I/O table (page 4). Deleted the Noise Figure and Noise Power Floor specs from the Electrical Specifications: Dynamic table (page 6).
6. Changes to Electrical Specifications: TH1 Switching table (page 7):
    a. Changed Test Level from 2 to 4 on the following specs:
    - Aperture Delay Drift
    - Differential Droop Rate
    - Differential Drift Rate
    b. Deleted the Hold Noise Spec.
7. Changes to Electrical Specifications: TH2 Switching table (page 8):
    a. Changed Test Level from 2 to 4 on the following specs:
    - Differential Droop Rate
    - Differential Drift Rate
    b. Deleted the Hold Noise Spec.
8. Replaced the 4mm QFN Package Outline Drawing with the current version (no dimensions changed).
9. Updated Qualification Notification section to indicate that the 1321TH is fully qualified and added warranty information (page 14).