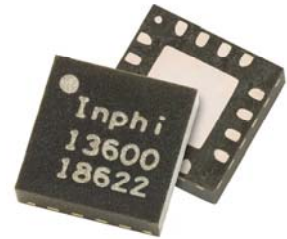


13600DF

13 Gbps D Flip-Flop in QFN Package

Data Sheet



Applications

- High-speed (up to 13 GHz) digital logic
- High-speed (up to 13 Gbps) serial data transmission systems
- Broadband test and measurement equipment

Features

- Supports data rates up to 13 Gbps
- Very low random jitter: 37 fs rms typical
- Fast rise and fall times: 16 ps typical
- Low power consumption: 300 mW typical
- Supports single-ended and differential operation
- Output signal swing 1200 mVpp differential
- Low Added Deterministic Jitter: 2 ps pp typical
- Single -3.3 V power supply
- Available in QFN package
- Evaluation board available

Description

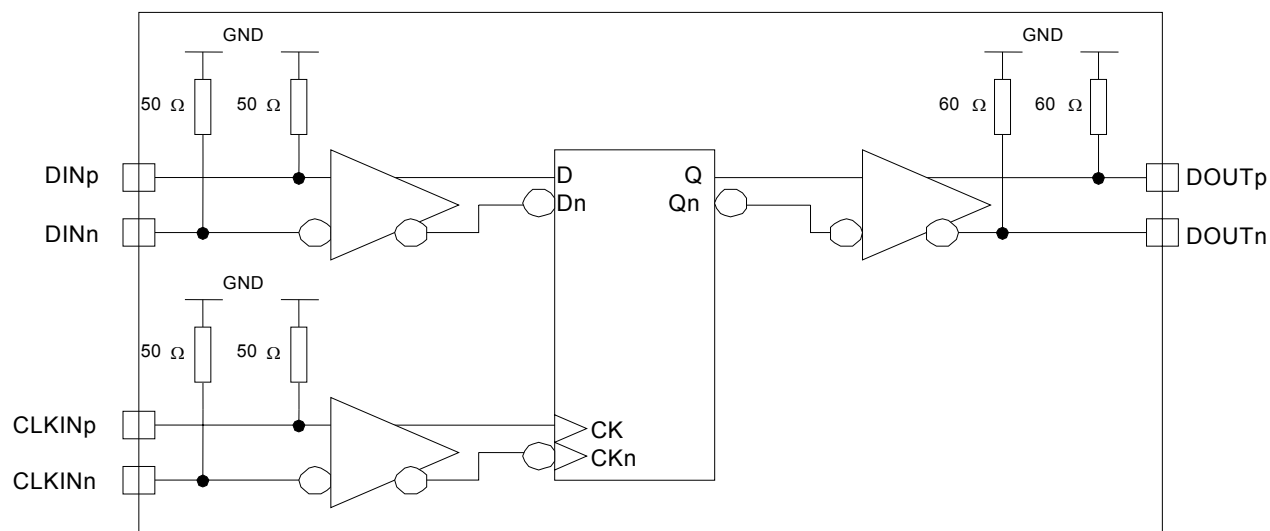
The 13600DF static D flip-flop (DFF) is designed to support data rates up to 13 Gbps. The part is nominally positive-edge triggered; however, by reversing the positive and negative clock connections, a negative-edge triggered application can be accommodated.

All differential data and differential clock inputs are on-chip DC coupled and terminated with 50 Ω resistors to ground (GND). For direct-coupled applications, the differential data outputs should

be terminated off chip with 50 Ω resistors to GND. For applications requiring termination to DC levels other than GND, external AC coupling to a good RF ground is required. See the application note for various termination examples.

The 13600DF operates from a single -3.3 V power supply and is available in a 3 x 3 mm² quad flat no-lead (QFN) package. The QFN part is also available on an evaluation board with SMA connectors.

Block Diagram



Absolute Maximum Ratings

- Stresses beyond those listed here may cause permanent damage to the device.
- These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the "Operating Conditions" and "Electrical Specifications" of this datasheet is not implied.
- Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Conditions	Min	Max	Unit
Power Supply Voltage	V_{EE}		-3.6	+0.5	V
Input Signals (Data & Clock)			-2	+1	V
Output Signals			-2	+1	V
Junction Temperature – Die	T_J		-5	+175	°C
Case Temperature – Package	T_C		-15	+125	°C
Shipping/Storage Temperature	T_{STORE}		-40	+125	°C
Humidity	RH		0	100	%
ESD Protection (Human Body Model)	ESD	Clock and Data inputs	500	---	V
		Data outputs	250	---	V
		Power Supply	500	---	V

Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply Voltage	V_{EE}	± 5% Tolerance	-3.465	-3.300	-3.135	V
On-Chip Power Dissipation	P_D		---	300	410	mW
Power Supply Current	I_{EE}		70	91	115	mA
Operating Temperature (Junction) – Die	T_J		+15	---	+125	°C
Operating Temperature (Case) – Package	T_C	Bottom of paddle	-5	---	+85	°C
Thermal Resistance – junction to paddle	$R_{JC} (\theta_{JC})$	Bottom of paddle	---	51	---	°C/W

Electrical Specifications



WARNING – To prevent damage to the part:

- DC power must be turned off prior to connecting or disconnecting any cables.

Electrical specifications guaranteed when the part is operated within the specified operating conditions.						
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Maximum Data Rate		10 ⁻¹² BER (NRZ format)	13			Gbps
Maximum Clock Frequency	f _{MAX}		13	---	---	GHz
Minimum Clock Slew Rate	S _{MIN}	At crossing of CLKIN _p and CLKIN _n	---	---	1	V/ns
Input High Level (Data & Clock)	V _{IH}		-0.5	---	0.5	V
Input Low Level (Data & Clock)	V _{IL}		-1.0	---	0	V
Input Amplitude (Data & Clock)	V _{INpp} , V _{CLKpp}	Differential peak-to-peak	300	---	2000	mVpp
		Single-ended peak-to-peak	300	---	1000	mVpp
Input Return Loss (Data & Clock) ¹	RL _{IN}	Freq. < 13 GHz and Input Common Mode (V _{ICM}) ≤ 0 V	10	---	---	dB
Clock Phase Margin	CPM	V _{IH} ≤ 0.3 V	280	300	---	deg
		V _{IH} > 0.3 V	260	300	---	deg
Data Output Amplitude ²	D _{OUT}	Differential peak-to-peak	900	1200	1400	mVpp
Output High Voltage	V _{OH}	DC coupled, GND referenced	-50	-4	0	mV
Output Common Mode	V _{OCM}	DC coupled, GND referenced	---	-300	---	mV
Output Rise/Fall Time	t _r /t _f	20–80%	---	16	25	ps
Output Return Loss ³	RL _{OUT}	Freq. < 13 GHz	10	---	---	dB
Added Deterministic Jitter ^{4, 5}	J _D	Peak-to-peak at 12.5 Gbps	---	2	4	ps
Added Random Jitter ^{4, 6}	J _R	RMS at 10 GHz	---	37	80	fs
Clock to Data Output Delay ⁴	t _Q	QFN Package	50	65	80	ps

Notes:

¹ Inputs are designed to be a broadband match to 50 Ω impedance and are terminated with a 50 Ω resistor to GND.

² Outputs are CML. Values are based on DC measurements.

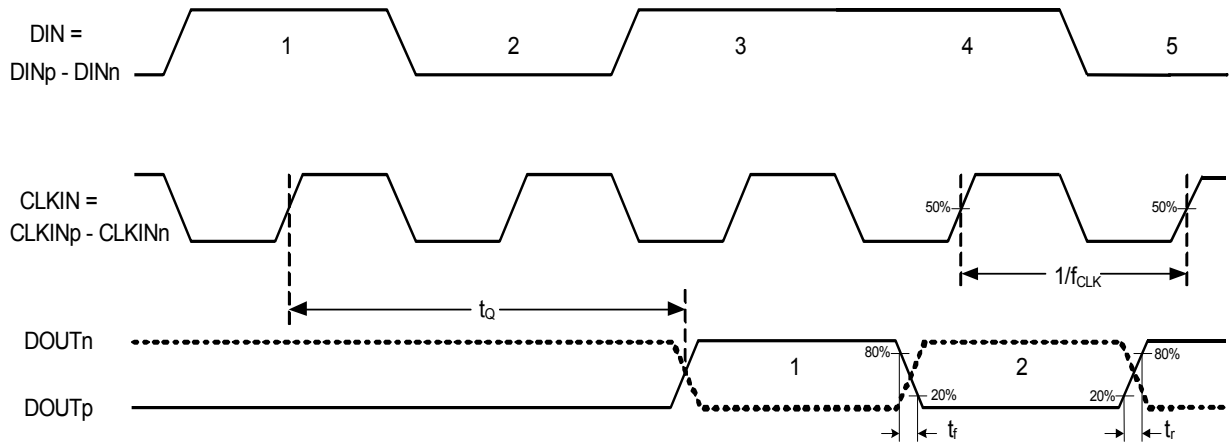
³ Outputs are designed to be a broadband match to 50 Ω impedance and are terminated with a 60 Ω resistor to GND.

⁴ Valid when clock to data phase is near center of CPM window. Propagation delay is based on simulations.

⁵ The added deterministic jitter (J_D) specified is the total peak-to-peak jitter measured using a 2³¹-1 PRBS data pattern less the measured peak-to-peak jitter of the input clock source.

⁶ The added random jitter (J_R) is the calculated RMS jitter based on residual phase noise measurements.

Timing Diagram



Note: Not drawn to scale

D-Flip Flop Truth Table

Inputs				Outputs	
$DINp_{k-1}$	$DINn_{k-1}^1$	CLKINp	CLKINn ¹	DOUTp _k	DOUTn _{k}^1}
L	H	↑	↓	L	H
H	L	↑	↓	H	L

¹ $DIN1n$, $CLKINn$ and $DOUTn$ are complementary signals to $DIN1p$, $CLKINp$ and $DOUTp$, respectively.

H Denotes a HIGH voltage level
 L Denotes a LOW voltage level
 ↑ Denotes a rising clock transition
 ↓ Denotes a falling clock transition

Typical DC Operating Characteristics

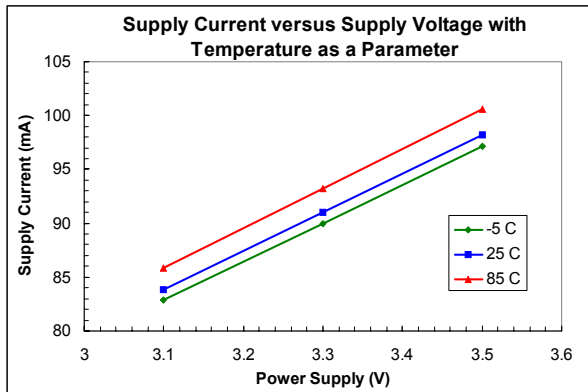


Figure 1. Power supply current vs. power supply voltage

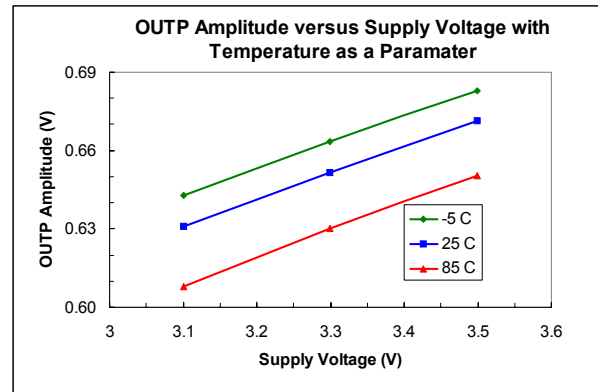


Figure 2. Single-ended, peak-to-peak output amplitude (on wafer) vs. power supply

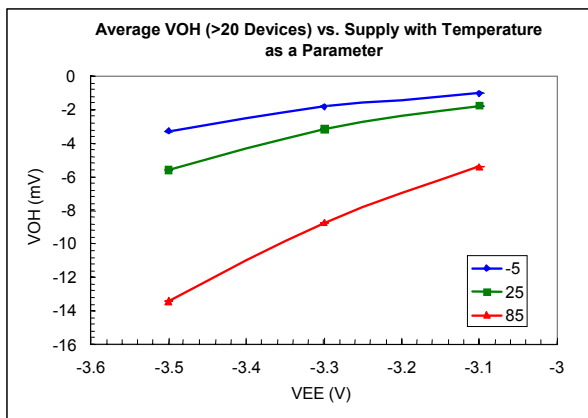


Figure 3. Single-ended, output high level (on wafer) vs. power supply

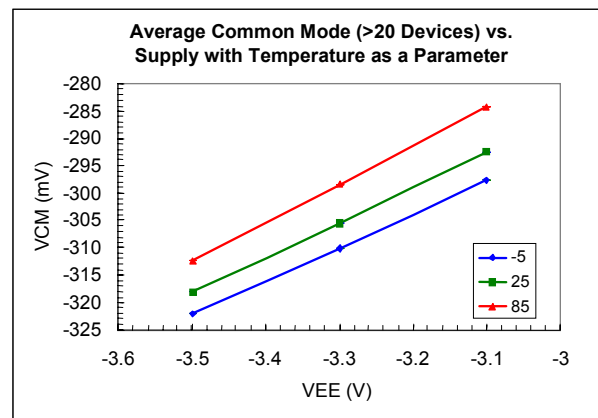


Figure 4. Output common mode (on wafer) vs. power supply

Time Domain Operating Characteristics

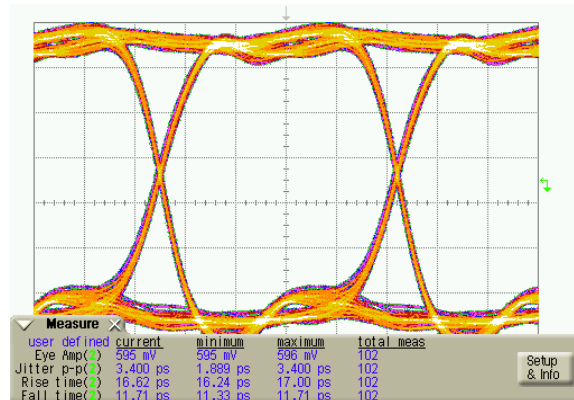


Figure 5. Output DOUTp (QFN package) at 10 Gbps, $2^{31}-1$ PRBS data input; 100 mV/div, 20 ps/div.

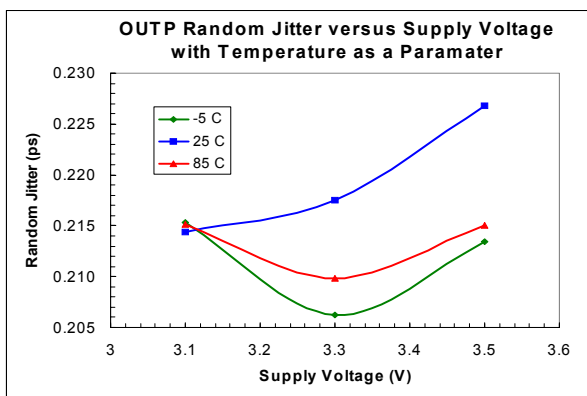


Figure 6. Output Random Jitter (on wafer) vs. Power Supply; Refer to note #3 under Electrical Specifications.

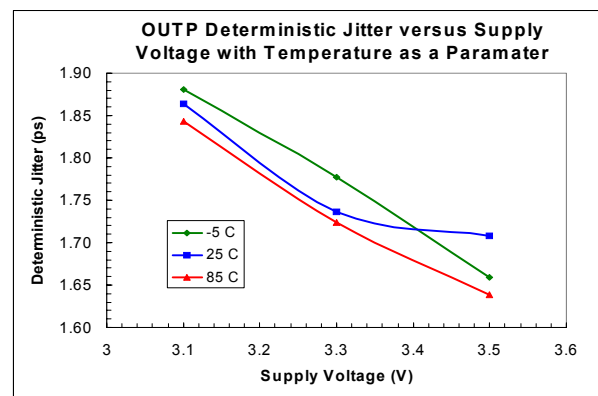


Figure 7. Output Deterministic Jitter (on wafer) vs. Power Supply; Refer to note #3 under Electrical Specifications.

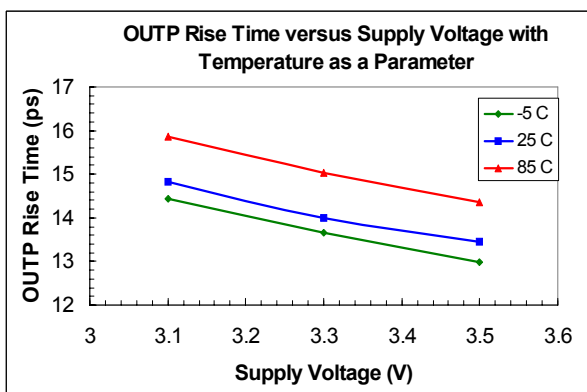


Figure 8. Output Rise Time (on wafer) vs. power supply

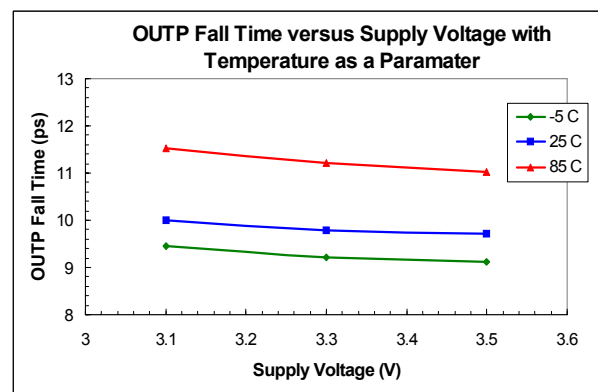


Figure 9. Output Fall Time (on wafer) vs. power supply

Typical Return Losses

All S-parameter measurements were made single-ended. S-parameters for the packaged part are not given here due to the unavailability of calibration standards for the evaluation board.

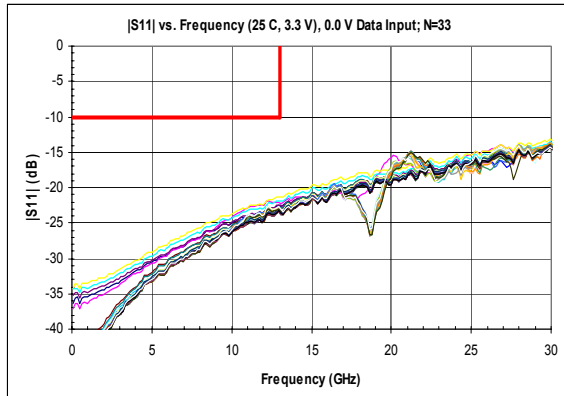


Figure 10. Data Input $|S_{11}|$ versus frequency of 33 die on wafer at $V_{EE} = -3.3$ V and 25° C; Input common mode = 0 V.

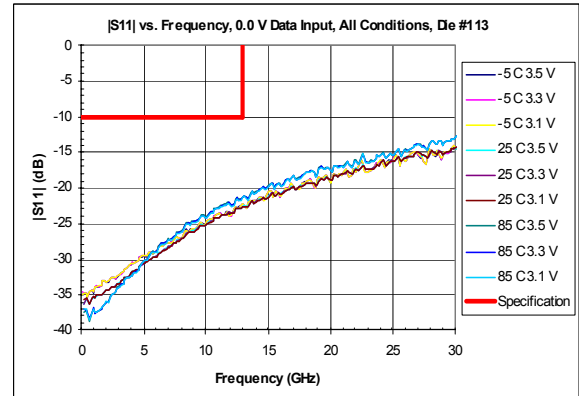


Figure 11. Data Input $|S_{11}|$ versus frequency of one dice on wafer at $V_{EE} = -3.3$ V and 25° C; Input common mode = 0 V.

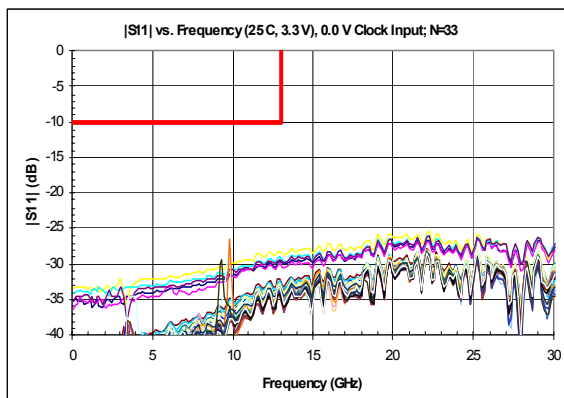


Figure 12. Clock Input $|S_{11}|$ versus frequency of 33 die on wafer at $V_{EE} = -3.3$ V and 25° C; Input common mode = 0 V.

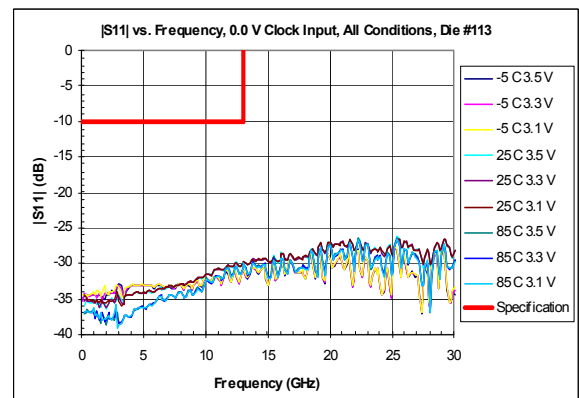


Figure 13. Clock Input $|S_{11}|$ versus frequency of one dice on wafer at $V_{EE} = -3.3$ V and 25° C; Input common mode = 0 V.

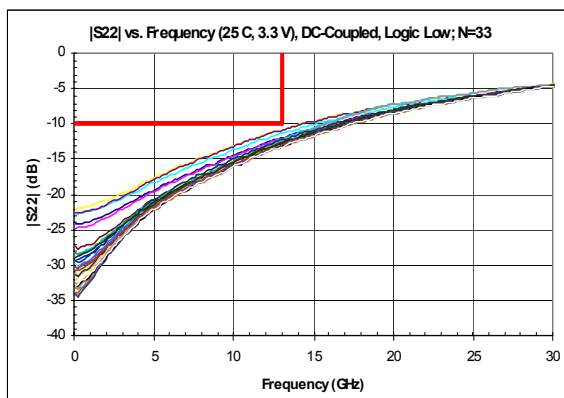


Figure 14. Data Output $|S_{22}|$ versus frequency of 33 die on wafer at $V_{EE} = -3.3$ V and 25° C; Output in logic low state. Add 3dB margin for logic high state.

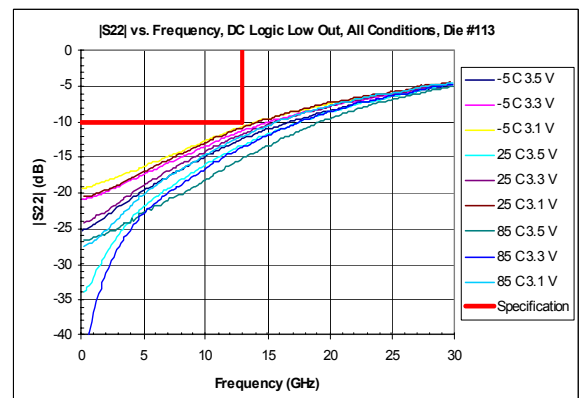
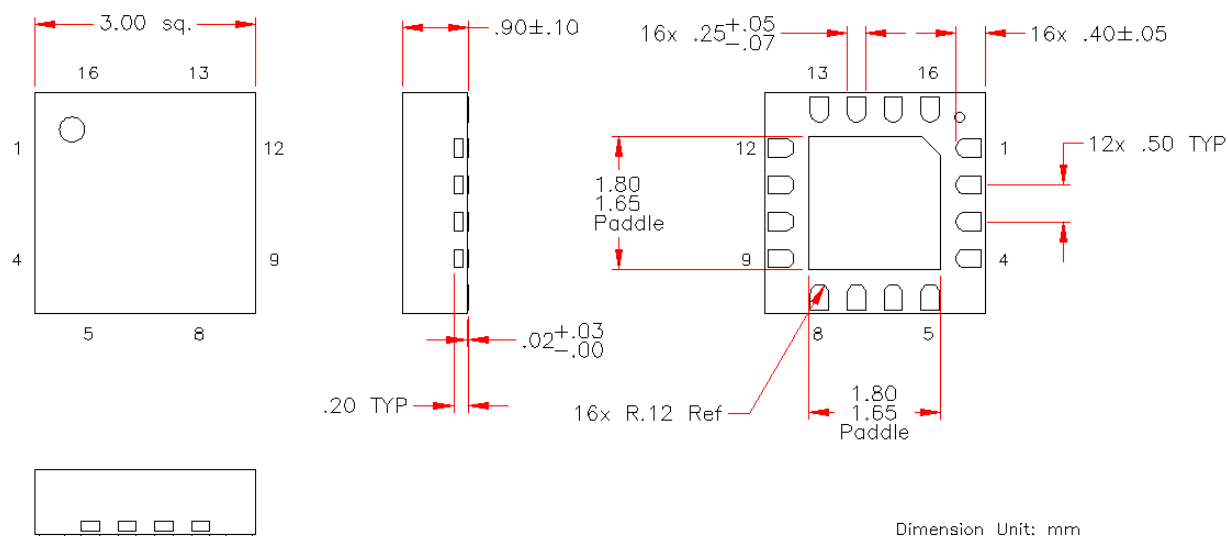


Figure 15. Data Output $|S_{22}|$ versus frequency of one dice on wafer at $V_{EE} = -3.3$ V and 25° C; Output in logic low state. Add 3dB margin for logic high state.

QFN Package Outline Drawing and Pin Assignment



Name	Pin	Description	Function
DIN _p	3	Non-inverting Data Input	Input
DIN _n	2	Inverting Data Input	Input
CLKIN _p	6	Non-inverting Clock Input	Input
CLKIN _n	7	Inverting Clock Input	Input
DOU _{Tp}	11	Non-inverting Data Output	Output
DOU _{Tn}	10	Inverting Data Output	Output
GND	1, 4, 5, 8, 9, 12, 14, paddle	Ground	Supply
V _{EE}	13, 15, 16	Power Supply: Connect to -3.3 V	Supply

Note:

The paddle is the heat dissipation path and must be tied to the PCB ground planes by means of thermal vias.


Order Information

Part No.	Description
13600DF-S02QFN	13 Gbps D Flip-Flop (-3.3 V Supply) in QFN Package
13600DF-S02QFN-EVB	13 Gbps D Flip-Flop (-3.3 V Supply) in QFN Package on an Evaluation Board with SMA Connectors

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Qualification Notification

The 13600DF-S02 is fully qualified. Please contact Inphi for the qualification report.

Inphi Corporation will honor the full warranty as outlined in Section 5 of Inphi's Standard Customer Purchase Order Terms and Conditions.

Version Updates

From Version 2.2 to 2.3 (dated 2008-03-28)

1. Added the typical random and deterministic jitter numbers to the Features section (page 1).
2. Changed the jitter specifications in the Electrical Specifications table (page 3):
 - a. Changed "Deterministic Jitter" parameter name to "Added Deterministic Jitter".
 - i. Added "at 12.5 Gbps" to the Test Conditions.
 - ii. Changed typical spec from 3 ps to 2 ps.
 - iii. Changed Max spec from 6 ps to 4 ps.
 - iv. Modified note #5.
 - b. Changed "Random Jitter" parameter name to "Added Random Jitter".
 - i. Added Test Conditions "at 10 GHz".
 - ii. Changed typical spec from 0.3 ps to 37 fs.
 - iii. Changed Max spec from 0.6 ps to 80 fs.
 - iv. Added note #6.
3. Added the requirement to use thermal vias from the package paddle to the PCB in the notes of the QFN Package Outline Drawing and Pin Assignment section (page 8).