

Description

The 5PB11xx is a high-performance LVCMOS Clock Buffer Family. It has best-in-class Additive Phase Jitter of 50fsec RMS.

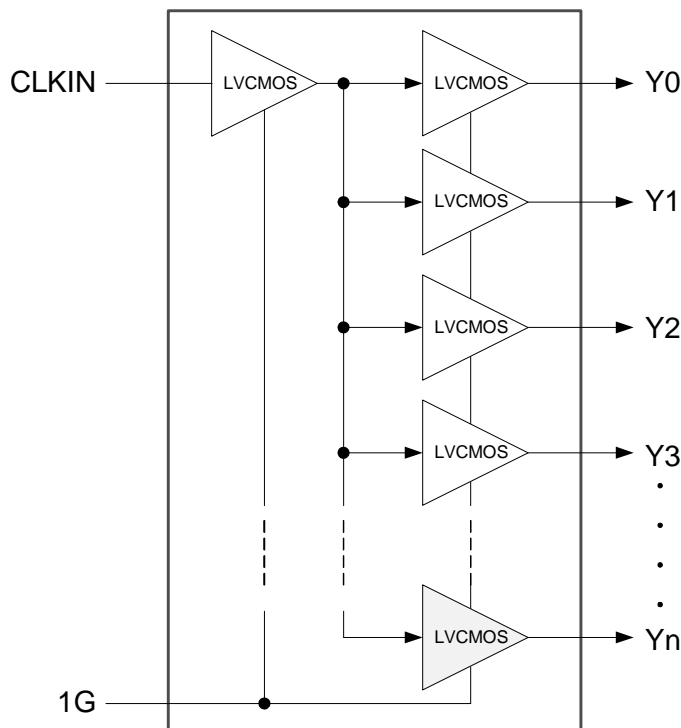
There are five different fan-out variations, 1:2 to 1:10, available.

The IDT5PB11xx also supports a synchronous glitch-free Output Enable function to eliminate any potential intermediate incorrect output clock cycles when enabling or disabling outputs. It comes in various packages and can operate from a 1.8V to 3.3V supply.

Features

- High performance 1:2, 1:4, 1:6, 1:8, 1:10 LVCMOS clock buffer
- Very low pin-to-pin skew <50 ps
- Very low additive jitter <50 fs
- Supply voltage: 1.8V to 3.3V
- fMAX = 200MHz
- Integrated serial termination for 50ohm channel
- Packaged in 8-, 14-, 16-, 20-pin TSSOP and small DFN and QFN packages
- Extended (-40°C to +105°C) temperature range

Block Diagram



Pin Assignments for TSSOP Packages

CLKIN	1	8	Y1
1G	2	7	NC
Y0	3	6	VDD
GND	4	5	NC

5PB1102PGGI

CLKIN	1	8	Y1
1G	2	7	Y3
Y0	3	6	VDD
GND	4	5	Y2

5PB1104PGGI

CLKIN	1	14	Y1
1G	2	13	Y3
Y0	3	12	VDD
GND	4	11	Y2
VDD	5	10	GND
Y4	6	9	Y5
GND	7	8	VDD

5PB1106PGGI

CLKIN	1	16	Y1
1G	2	15	Y3
Y0	3	14	VDD
GND	4	13	Y2
VDD	5	12	GND
Y4	6	11	Y5
GND	7	10	VDD
Y6	8	9	Y7

5PB1108PGGI

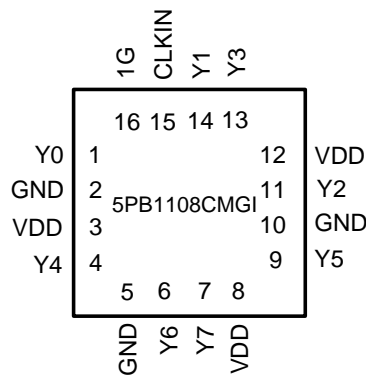
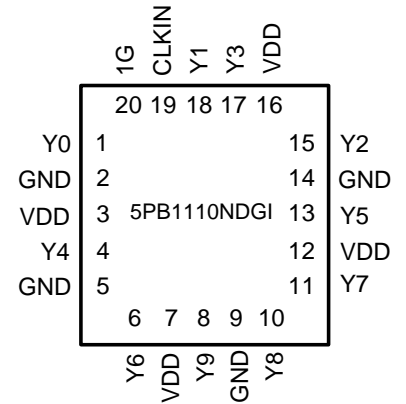
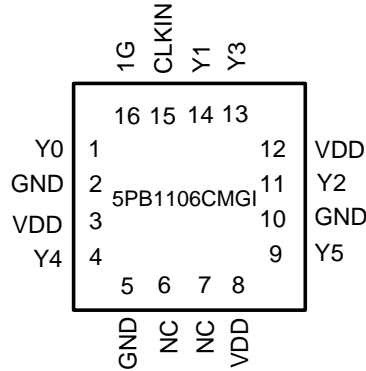
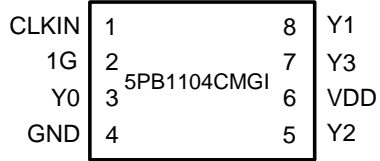
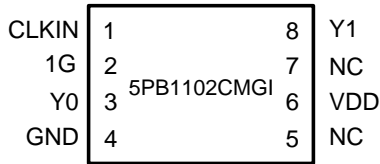
CLKIN	1	20	Y1
1G	2	19	Y3
Y0	3	18	VDD
GND	4	17	Y2
VDD	5	16	GND
Y4	6	15	Y5
GND	7	14	VDD
Y6	8	13	Y7
VDD	9	12	Y8
Y9	10	11	GND

5PB1110PGGI

Pin Descriptions for TSSOP Packages

Device Number	LVC MOS Clock Input	Clock Output Enable	LVC MOS Clock Output	Supply Voltage	Ground
	CLKIN	1G	Y0, Y1, . . . Y9	VDD	GND
5PB1102PGGI	1	2	3, 8	6	4
5PB1104PGGI	1	2	3, 8, 5, 7	6	4
5PB1106PGGI	1	2	3, 14, 11, 13, 6, 9	5, 8, 12	4, 7, 10
5PB1108PGGI	1	2	3, 16, 13, 15, 6, 11, 8, 9	5, 10, 14	4, 7, 12
5PB1110PGGI	1	2	3, 20, 17, 19, 6, 15, 8, 13, 12, 10	5, 9, 14, 18	4, 7, 11, 16

Pin Assignments for DFN/QFN Packages



Pin Descriptions for DFN/QFN Packages

Device Number	LVC MOS Clock Input	Clock Output Enable	LVC MOS Clock Output	Supply Voltage	Ground
	CLKIN	1G	Y0, Y1, . . . Y9	VDD	GND
5PB1102CMGI	1	2	3, 8	6	4
5PB1104CMGI	1	2	3, 5, 7, 8	6	4
5PB1106CMGI	15	16	1, 4, 9, 11, 13, 14	3, 8, 12	2, 5, 10
5PB1108CMGI	15	16	1, 4, 6, 7, 9, 11, 13, 14	3, 8, 12	2, 5, 10
5PB1110NDGI	19	20	1, 4, 6, 8, 10, 11, 13, 15, 17, 18	3, 7, 12, 16	2, 5, 9, 14

Output Logic Table

Inputs		Output
CLKIN	1G	Yn
X	L	L
L	H	L
H	H	H

After at least three cycles of input clock toggling, Output Enable function is asynchronous to eliminate any intermediate incorrect output clock cycles during transition which may cause frequency peaking to the downstream device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 5PB11xx. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	3.465V
Output Enable and All Outputs	-0.4 V to VDD+0.5 V
CLKIN	-0.4 V to 3.465V
Ambient Operating Temperature (extended)	-40 to +105°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (extended)	-40		+105	°C
Power Supply Voltage (measured in respect to GND)	+1.71		+3.465	V

DC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD=1.8V ±5% , Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		1.71		1.89	V
Input High Voltage, CLKIN	V _{IH}	Note 1	0.7xVDD		VDD	V
Input Low Voltage, CLKIN	V _{IL}	Note 1			0.3xVDD	V
Input High Voltage, 1G	V _{IH}		1.6		VDD	V
Input Low Voltage, 1G	V _{IL}				0.6	V
Output High Voltage	V _{OH}	I _{OH} = -5 mA	1.4			V
Output Low Voltage	V _{OL}	I _{OL} = 5 mA			0.4	V
Nominal Output Impedance	Z _O			50		Ω
Input Capacitance	C _{IN}	CLKIN, 1G pin		5		pF
Operating Supply Current						
5PB1102	IDD	100MHz, No load, 25°C		8		mA
5PB1104		100MHz, No load, 25°C		12		
5PB1106		100MHz, No load, 25°C		16		
5PB1108		100MHz, No load, 25°C		21		
5PB1110		100MHz, No load, 25°C		25		

Notes: 1. Nominal switching threshold is VDD/2

VDD=2.5 V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.375		2.625	V
Input High Voltage, CLKIN	V _{IH}	Note 1	0.7xVDD		VDD	V
Input Low Voltage, CLKIN	V _{IL}	Note 1			0.3xVDD	V
Input High Voltage, 1G	V _{IH}		1.8		VDD	V
Input Low Voltage, 1G	V _{IL}				0.7	V
Output High Voltage	V _{OH}	I _{OH} = -8 mA	1.9			V
Output Low Voltage	V _{OL}	I _{OL} = 8 mA			0.5	V
Nominal Output Impedance	Z _O			50		Ω
Input Capacitance	C _{IN}	CLKIN, 1G pin		5		pF
Operating Supply Current						
5PB1102	IDD	100MHz, No load, 25°C		10		mA
5PB1104		100MHz, No load, 25°C		15		
5PB1106		100MHz, No load, 25°C		22		
5PB1108		100MHz, No load, 25°C		28		
5PB1110		100MHz, No load, 25°C		33		

VDD=3.3 V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135		3.465	V
Input High Voltage, CLKIN	V _{IH}	Note 1	0.7xVDD		VDD	V
Input Low Voltage, CLKIN	V _{IL}	Note 1			0.3xVDD	V
Input High Voltage, 1G	V _{IH}		2		VDD	V
Input Low Voltage, 1G	V _{IL}				0.8	V
Output High Voltage	V _{OH}	I _{OH} = -12 mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 12 mA			0.7	V
Nominal Output Impedance	Z _O			50		Ω
Input Capacitance	C _{IN}	CLKIN, 1G pin		5		pF
Operating Supply Current						
5PB1102	IDD	100MHz, No load, 25°C		12		mA
5PB1104		100MHz, No load, 25°C		20		
5PB1106		100MHz, No load, 25°C		25		
5PB1108		100MHz, No load, 25°C		35		
5PB1110		100MHz, No load, 25°C		40		

AC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD = 1.8V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time (2 pF load)	t _{OR}	0.36V to 1.44V, C _L =2 pF		0.5	0.75	ns
Output Fall Time (2 pF load)	t _{OF}	1.44V to 0.36V, C _L =2 pF		0.5	0.75	ns
Output Rise Time (5 pF load)	t _{OR}	0.36V to 1.44V, C _L =5 pF		0.8	1.0	ns
Output Fall Time (5 pF load)	t _{OF}	1.44V to 0.36V, C _L =5 pF		0.8	1.0	ns
Start-up Time	t _{START-UP}	Part start-up time for valid outputs after VDD ramp-up			3	ms
Propagation Delay		Note 1		1.9	2.2	ns
Buffer Additive Phase Jitter, RMS		156.25MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew (5PB1102/04/06)		Rising edges at VDD/2, Note 2		35	50	ps
Output to Output Skew (5PB1108/10)		Rising edges at VDD/2, Note 2		45	65	ps
Device to Device Skew		Rising edges at VDD/2			200	ps
Output Enable Time	t _{EN}	C _L ≤ 5 pF			3	cycles
Output Disable Time	t _{DIS}	C _L ≤ 5 pF			3	cycles

VDD = 2.5 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time (2 pF load)	t _{OR}	0.5V to 2.0V, C _L =2 pF		0.4	0.7	ns
Output Fall Time (2 pF load)	t _{OF}	2.0V to 0.5V, C _L =2 pF		0.4	0.7	ns
Output Rise Time (5 pF load)	t _{OR}	0.5V to 2.0V, C _L =5 pF		0.75	1.0	ns
Output Fall Time (5 pF load)	t _{OF}	2.0V to 0.5V, C _L =5 pF		0.75	1.0	ns
Start-up Time	t _{START-UP}	Part start-up time for valid outputs after VDD ramp-up			3	ms
Propagation Delay		Note 1		2.4	2.9	ns
Buffer Additive Phase Jitter, RMS		156.25MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew (5PB1102/04/06)		Rising edges at VDD/2, Note 2		35	50	ps
Output to Output Skew (5PB1108/10)		Rising edges at VDD/2, Note 2		45	65	ps
Device to Device Skew		Rising edges at VDD/2			200	ps
Output Enable Time	t _{EN}	C _L ≤ 5 pF			3	cycles
Output Disable Time	t _{DIS}	C _L ≤ 5 pF			3	cycles

VDD = 3.3 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time (2 pF load)	t _{OR}	0.66V to 2.64V, C _L =2 pF		0.45	0.6	ns
Output Fall Time (2 pF load)	t _{OF}	2.64V to 0.66V, C _L =2 pF		0.45	0.6	ns
Output Rise Time (5 pF load)	t _{OR}	0.66V to 2.64V, C _L = 5pF		0.7	1.0	ns
Output Fall Time (5 pF load)	t _{OF}	2.64V to 0.66V, C _L =5 pF		0.7	1.0	ns
Start-up Time	t _{START-UP}	Part start-up time for valid outputs after VDD ramp-up			3	ms
Propagation Delay		Note 1		2	2.4	ns
Buffer Additive Phase Jitter, RMS		156.25MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew (5PB1102/04/06)		Rising edges at VDD/2, Note 2		35	50	ps

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output to Output Skew (5PB1108/10)		Rising edges at VDD/2, Note 2		45	65	ps
Device to Device Skew		Rising edges at VDD/2			200	ps
Output Enable Time	t_{EN}	$C_L \leq 5$ pF			3	cycles
Output Disable Time	t_{DIS}	$C_L \leq 5$ pF			3	cycles

Notes:

1. With rail to rail input clock
2. Between any 2 outputs with equal loading.
3. Duty cycle on outputs will match incoming clock duty cycle. Consult IDT for tight duty cycle clock generators.

Phase Noise Plots

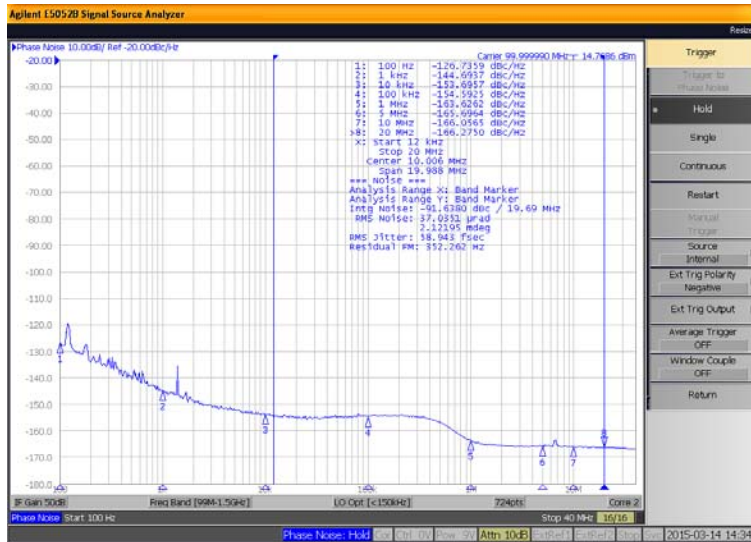


Figure 1. 5PB11xx Reference Phase Noise 58.9fs (12kHz to 20MHz)

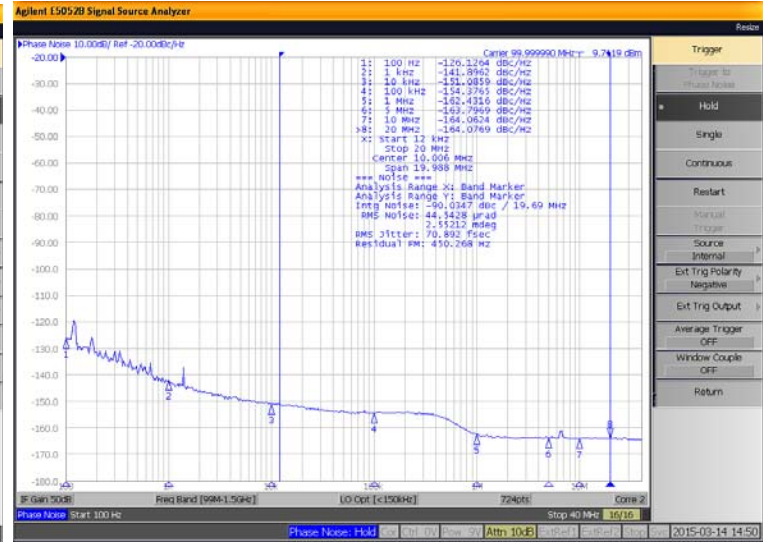
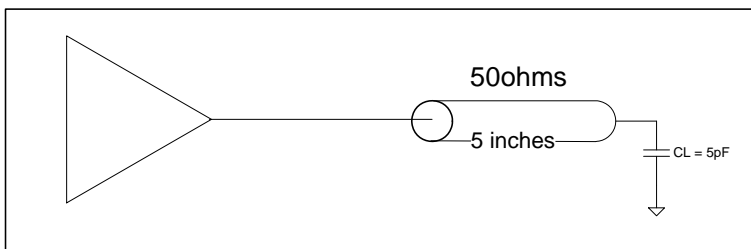


Figure 2. 5PB11xx Output Phase Noise 70.9fs (12kHz to 20MHz)

The phase noise plots above show the low Additive Jitter of the 5PB11xx high-performance buffer. With an integration range of 12kHz to 20MHz, the reference input has about 58.9fs of RMS phase jitter while the output of 5PB11xx has about 70.9fs of RMS phase jitter. This results in a low Additive Phase Jitter of only 39fs.

Test Load and Circuit



Marking Diagrams



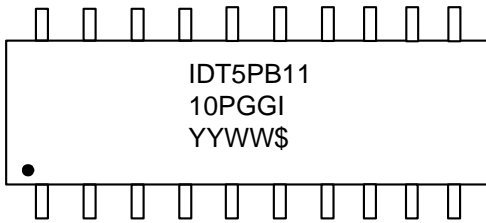
8-pin TSSOP



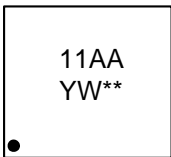
14-pin TSSOP



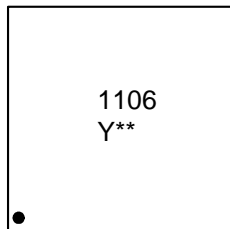
16-pin TSSOP



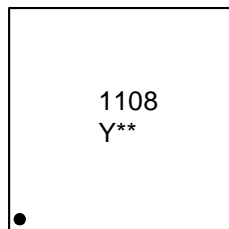
20-pin TSSOP



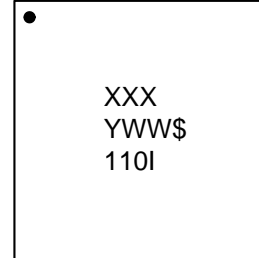
8-pin DFN



16-pin QFN



16-pin QFN

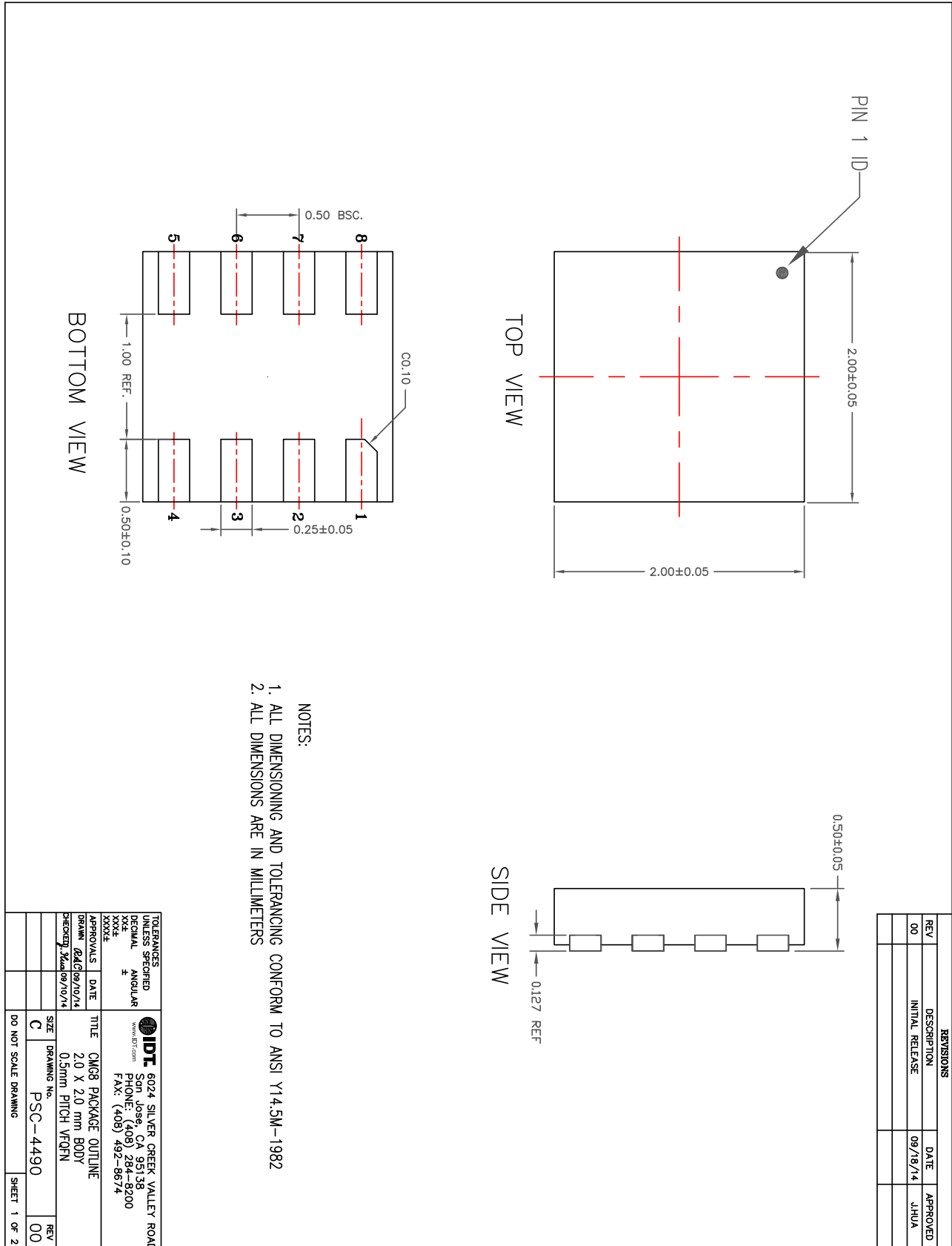


20-pin QFN

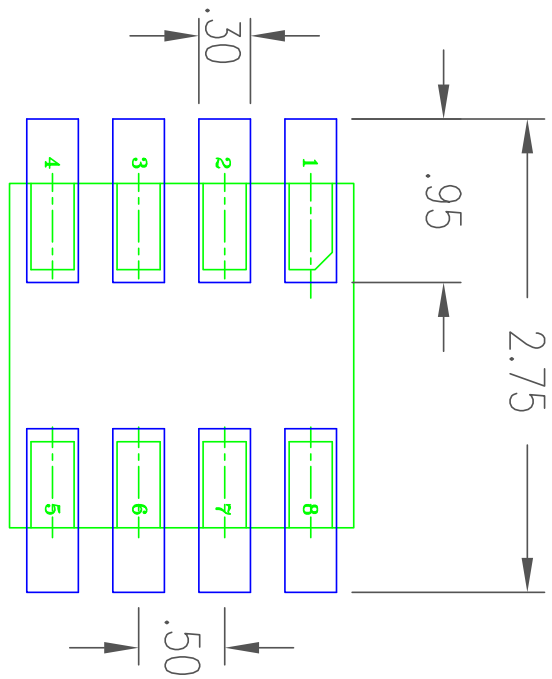
Notes:

1. "AA" denotes the last two digits of the part number for 8-pin TSSOP and DFN (e.g. 02, 04).
2. "**" is the lot sequence.
3. "XXX" denotes the last three characters of the Asm lot (20-pin QFN only).
4. "YYWW", "YWW", "YW", or "Y" is the last digit(s) of the year and week that the part was assembled.
5. "\$" denotes the mark code.
6. "G" after the two-letter package code denotes RoHS compliant package.
7. "I" denotes extended temperature range device.
8. Bottom marking: country of origin (TSSOP only).

Package Outline and Package Dimensions (8-pin DFN, 2mm x 2mm Body, 0.5mm pitch)



Package Outline and Package Dimensions, cont. (8-pin DFN, 2mm x 2mm Body, 0.5mm pitch)



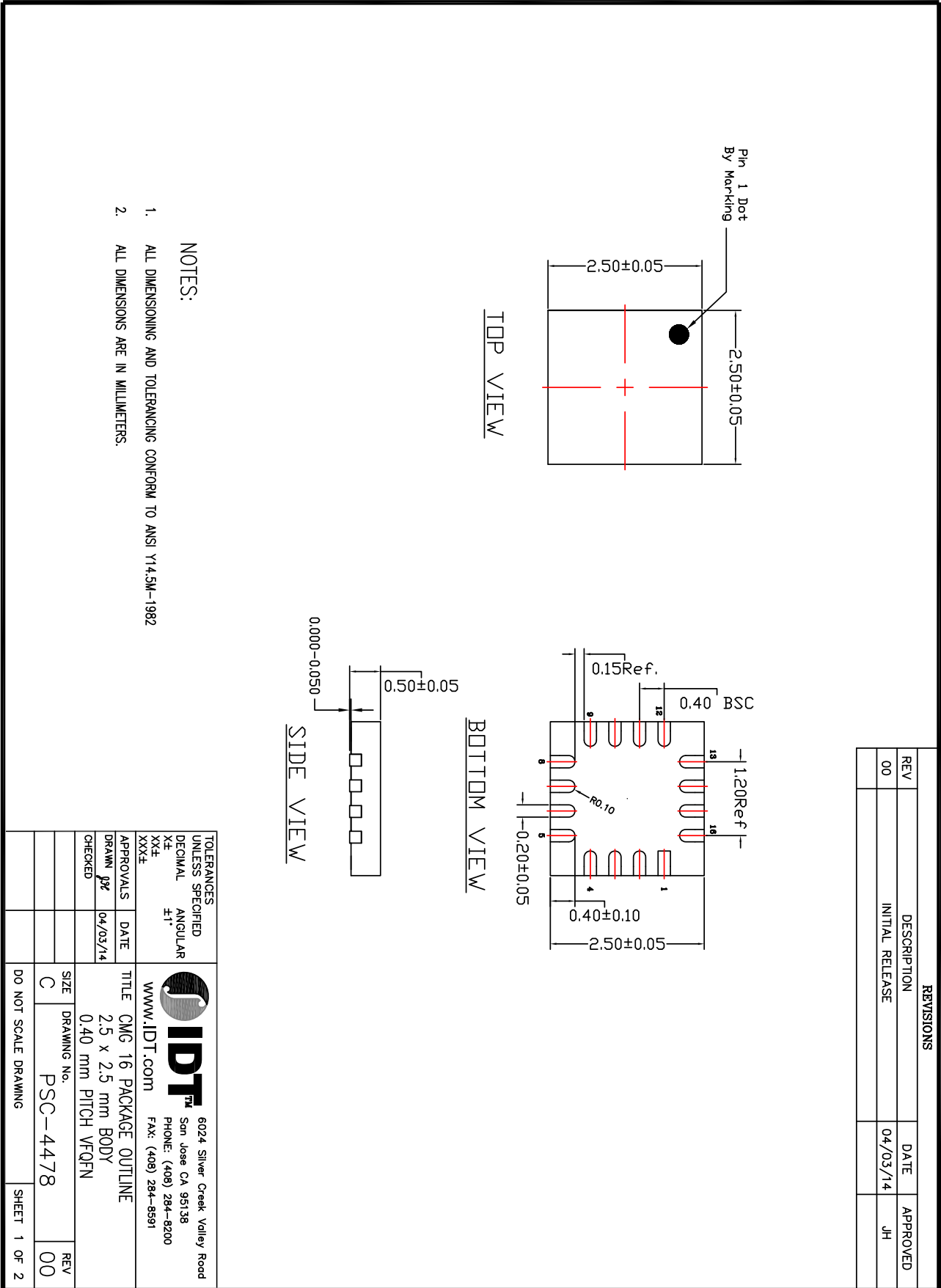
RECOMMENDED LAND PATTERN DIMENSION

- NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
 2. TOP DOWN VIEW, AS VIEWED.
 3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
 4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
 5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR MOUNT DESIGN AND LAND PATTERN.

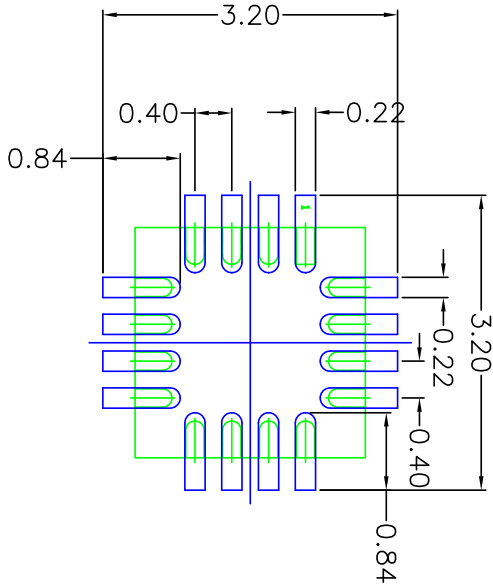
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	09/18/14	JHVA

TOLERANCES UNLESS SPECIFIED		6024 SILVER CREEK VALLEY ROAD SIMI VALLEY, CA 91382 PHONE: (409) 264-8200 FAX: (409) 492-8674
DECIMAL	ANGULAR	
XXX	#	
XXXX		
APPROVALS	DATE	TITLE
DRAWN <i>2/2/09/10/14</i>		CM08 PACKAGE OUTLINE
CHECKED		2.0 X 2.0 mm BODY 0.5 mm PITCH VFOFN
		SIZE DRAWING No. PSC-4490
		REV 00
DO NOT SCALE DRAWING		SHEET 2 OF 2

Package Outline and Package Dimensions (16-pin QFN, 2.5mm x 2.5mm Body, 0.4mm pitch)



Package Outline and Package Dimensions, cont. (16-pin QFN, 2.5mm x 2.5mm Body, 0.4mm pitch)



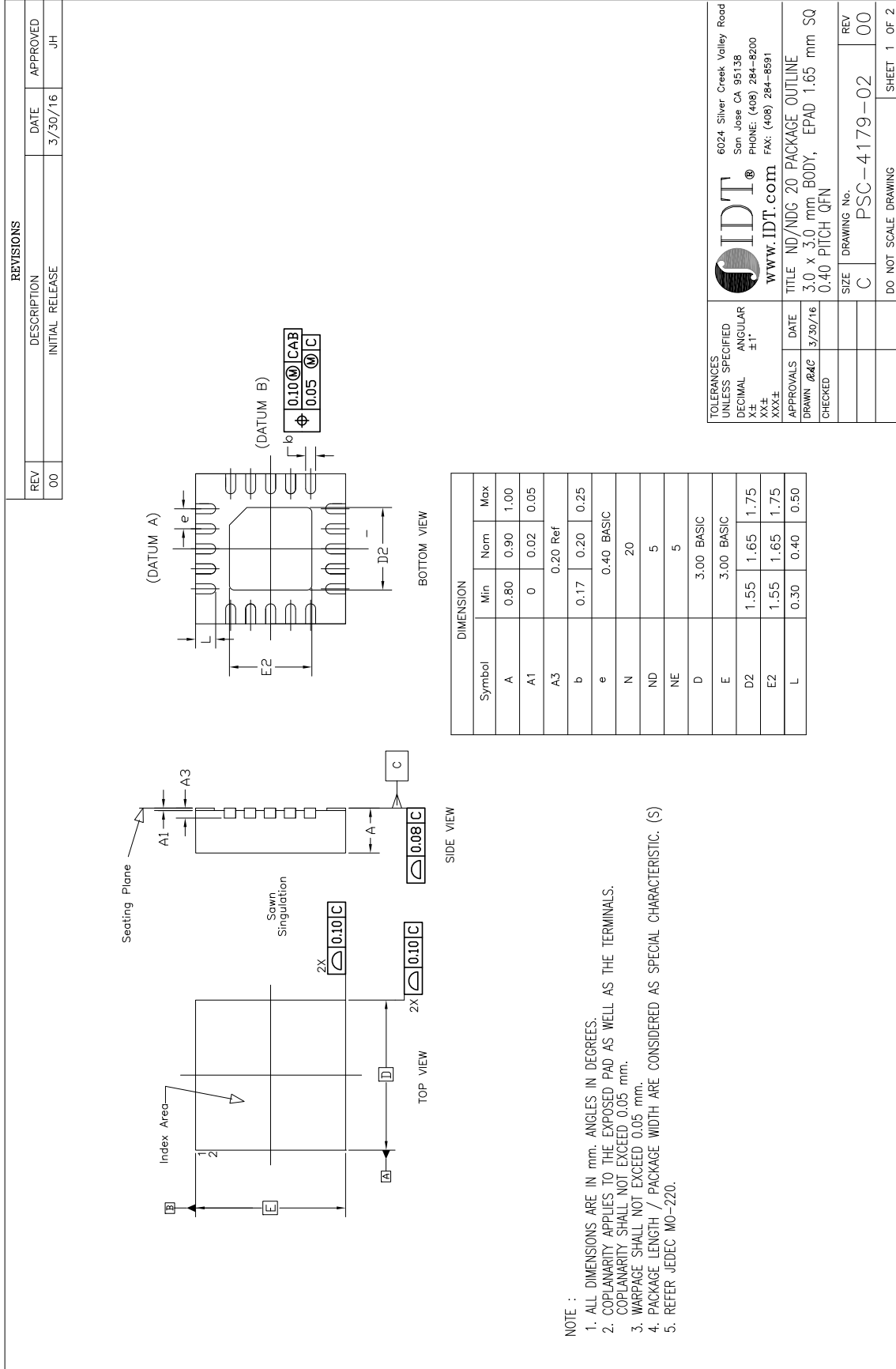
RECOMMENDED LAND PATTERN DIMENSION

- NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
 2. TOP DOWN VIEW. AS VIEWED ON PCB.
 3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
 4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
 5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
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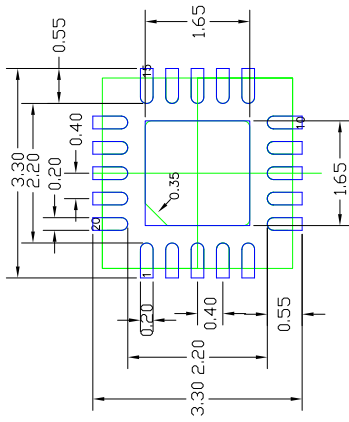
TOLERANCES UNLESS SPECIFIED		6024 Silver Creek Valley Road	
DECIMAL	ANGULAR	San Jose CA 95138	
XX±	1°	PHONE: (408) 284-8200	
XXX±		FAX: (408) 284-8591	
XXXX±		www.IDT.com	
APPROVALS	DATE	TITLE	
DRAWN <i>gk</i>	04/03/14	CMG 16 PACKAGE OUTLINE	
CHECKED		2.5 x 2.5 mm BODY	
		0.40 mm PITCH VQFN	
		SIZE	REV
		C	00
		DRAWING No.	
		PSC-4478	
		DO NOT SCALE DRAWING	SHEET 2 OF 2

Package Outline and Package Dimensions (20-pin QFN, 3mm x 3mm Body, 0.4mm pitch)



Package Outline and Package Dimensions, cont. (20-pin QFN, 3mm x 3mm Body, 0.4mm pitch)

REVISIONS			
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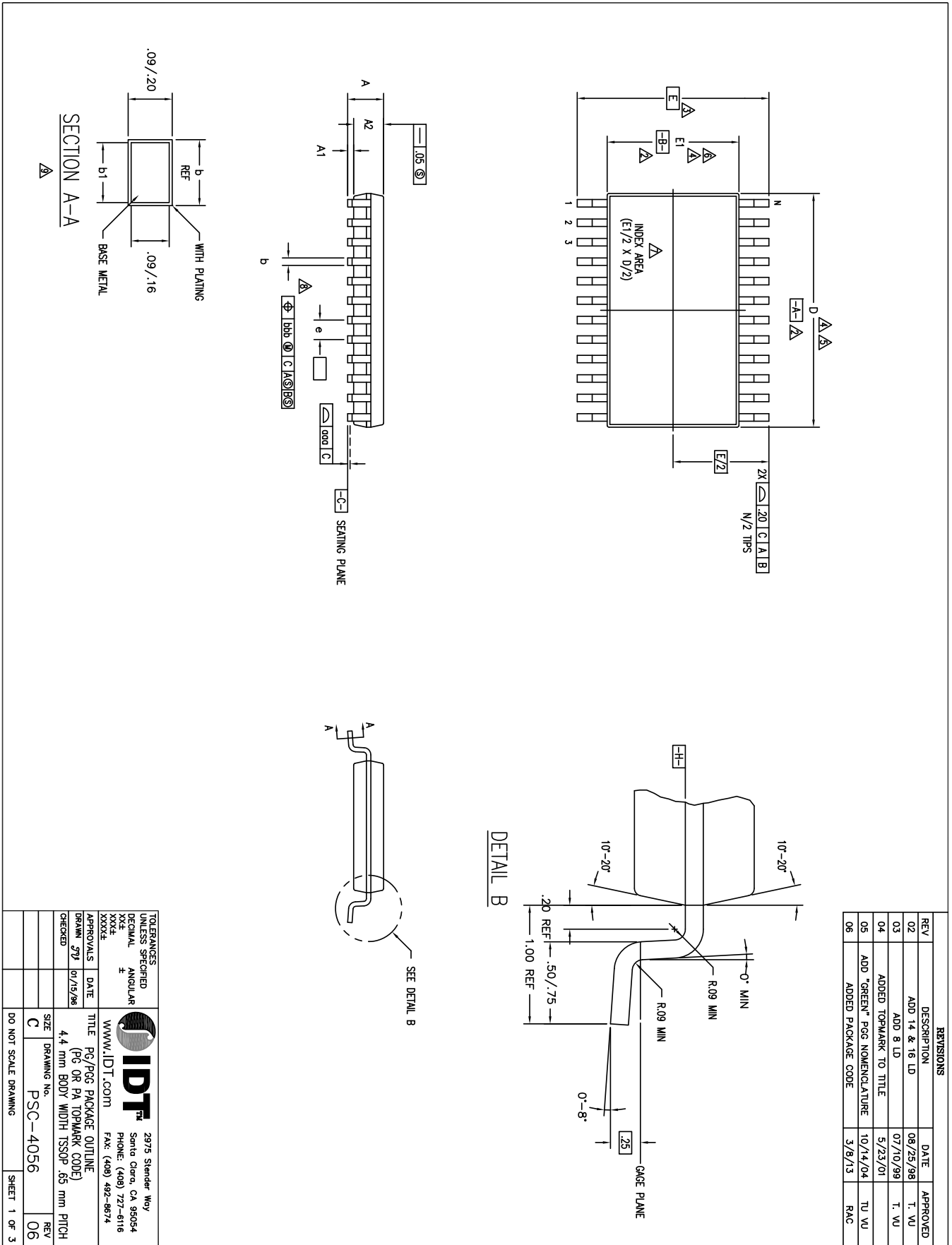


RECOMMENDED LAND PATTERN DIMENSION

- NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
 2. TOP DOWN VIEW, AS VIEWED ON PCB.
 3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
 4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
 5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED	6024 Silver Creek Valley Road
DECIMAL	San Jose CA 95138
X±	PHONE: (408) 284-8200
XX±	FAX: (408) 284-8591
XXX±	WWW: IDT.COM
APPROVALS	TITLE
DRAWN	DATE
CHECKED	3/30/16
	ND/NDG 20 PACKAGE OUTLINE
	3.0 x 3.0 mm BODY, EPAD 1.65 mm SQ
	0.40 PITCH QFN
SIZE	DRAWING No.
C	PSC-4179-02
DO NOT SCALE DRAWING	REV
	00
	SHEET 2 OF 2

Package Outline and Package Dimensions (8-, 14-, 16-, 20-pin TSSOP)



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
02	ADD 14 & 16 LD	08/25/98	T. VU
03	ADD 8 LD	07/10/99	T. VU
04	ADDED TOPMARK TO TITLE	5/23/01	TU VU
05	ADD "GREEN" Pkg NOMENCLATURE	10/14/04	TU VU
06	ADDED PACKAGE CODE	3/8/13	RAC

TOLERANCES UNLESS SPECIFIED			2975 Stender Way Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 482-8674	
DECIMAL	ANGULAR		WWW.IDT.COM TITLE PG/PKG PACKAGE OUTLINE (PG OR PA TOPMARK CODE) 4.4 mm BODY WIDTH TSSOP .65 mm PITCH	
XXXX	±	DATE	APPROVALS	DRWN
XXXX		01/15/98	STY	STY
CHECKED				
SIZE	DRAWING No.	PSC-4056	REV	06
DO NOT SCALE DRAWING			SHEET	1 OF 3

Package Outline and Package Dimensions, cont. (8-, 14-, 16-, 20-pin TSSOP)

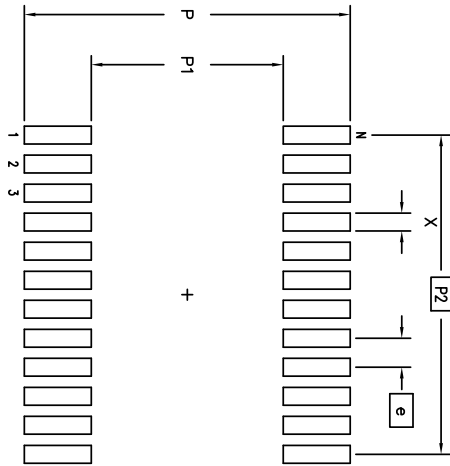
S M B D L	Pg/Pg68			Pg/Pg614			Pg/Pg616			Pg/Pg620		
	JEDEC VARIATION			JEDEC VARIATION			JEDEC VARIATION			JEDEC VARIATION		
	AA	NOM	MAX	AB-1	NOM	MAX	AB	NOM	MAX	AC	NOM	MAX
A	–	–	1.20	–	–	1.20	–	–	1.20	–	–	1.20
A1	.05	–	.15	.05	–	.15	.05	–	.15	.05	–	.15
A2	.80	1.00	1.05	.80	1.00	1.05	.80	1.00	1.05	.80	1.00	1.05
D	2.90	3.00	3.10	4.90	5.00	5.10	4.90	5.00	5.10	6.40	6.50	6.60
E	6.40	6.40	4.50	6.40	6.40	4.50	6.40	6.40	4.50	6.40	6.40	4.50
E1	4.30	4.40	4.50	4.30	4.40	4.50	4.30	4.40	4.50	4.30	4.40	4.50
e	.65 BSC			.65 BSC			.65 BSC			.65 BSC		
b	.19	–	.30	.19	–	.30	.19	–	.30	.19	–	.30
b1	.19	.22	.25	.19	.22	.25	.19	.22	.25	.19	.22	.25
ooo	–	–	.10	–	–	.10	–	–	.10	–	–	.10
bbb	–	–	.10	–	–	.10	–	–	.10	–	–	.10
N	8			14			16			20		

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
- DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION E TO BE DETERMINED AT SEATING PLANE **-C-**
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
- DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADII OR THE FOOT
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- ALL DIMENSIONS ARE IN MILLIMETERS
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-153, VARIATION AA, AB-1, AB, AC, AD & AE

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
02	ADD 14 & 16 LD	09/25/98	T. VU
03	ADD 8 LD	07/10/99	T. VU
04	ADDED TOPMARK TO TITLE	5/23/01	TU VU
05	ADD "GREEN" Pkg NOMENCLATURE	10/14/04	TU VU
06	ADDED PACKAGE CODE	3/8/13	RAC

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XXXX ± XXXXX		2975 Stander Way Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8874	
APPROVALS	DATE	TITLE	PC/Pg68 PACKAGE OUTLINE
DRAWN	07/15/98	(Pg OR PA TOPMARK CODE)	4.4 mm BODY WIDTH TSSOP .65 mm PITCH
CHECKED		SIZE	DRAWING No. PSC-4056
		DO NOT SCALE DRAWING	SHEET 2 OF 3

Package Outline and Package Dimensions, cont. (8-, 14-, 16-, 20-pin TSSOP)
LAND PATTERN DIMENSIONS


	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	7.20	7.40	7.20	7.40	7.20	7.40	7.20	7.40
P1	4.20	4.40	4.20	4.40	4.20	4.40	4.20	4.40
P2	1.95 BSC		3.90 BSC		4.55 BSC		5.85 BSC	
X	.30	.50	.30	.50	.30	.50	.30	.50
e	.65 BSC		.65 BSC		.65 BSC		.65 BSC	
N	8		14		16		20	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
02	ADD 14 & 16 LD	08/25/98	T. VU
03	ADD 8 LD	07/10/99	T. VU
04	ADDED TOPMARK TO TITLE	5/23/01	TU VU
05	ADD "GREEN" PGG NOMENCLATURE	10/14/04	TU VU
06	ADDED PACKAGE CODE	3/9/13	RAC

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XXX± ± XXXX± ±		APPROVALS DATE DRAWN 97J 01/15/98 CHECKED	
WWW.IDT.COM 		2975 Stender Way Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674	
TITLE PG/PGG PACKAGE OUTLINE (PG OR PA TOPMARK CODE) 4.4 mm BODY WIDTH TSSOP .65 mm PITCH			
SIZE	DRAWING No.	REV	
C	PSC-4056	06	
DO NOT SCALE DRAWING			SHEET 3 OF 3

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5PB1102PGGI	see page 8	Tubes	8-pin TSSOP	-40 to +105 °C
5PB1102PGGI8		Tape and Reel	8-pin TSSOP	-40 to +105 °C
5PB1104PGGI		Tubes	8-pin TSSOP	-40 to +105 °C
5PB1104PGGI8		Tape and Reel	8-pin TSSOP	-40 to +105 °C
5PB1106PGGI		Tubes	14-pin TSSOP	-40 to +105 °C
5PB1106PGGI8		Tape and Reel	14-pin TSSOP	-40 to +105 °C
5PB1108PGGI		Tubes	16-pin TSSOP	-40 to +105 °C
5PB1108PGGI8		Tape and Reel	16-pin TSSOP	-40 to +105 °C
5PB1110PGGI		Tubes	20-pin TSSOP	-40 to +105 °C
5PB1110PGGI8		Tape and Reel	20-pin TSSOP	-40 to +105 °C
5PB1102CMGI		Cut Tape	8-pin DFN	-40 to +105 °C
5PB1102CMGI8		Tape and Reel	8-pin DFN	-40 to +105 °C
5PB1104CMGI		Cut Tape	8-pin DFN	-40 to +105 °C
5PB1104CMGI8		Tape and Reel	8-pin DFN	-40 to +105 °C
5PB1104CMGI/W		Tape and Reel	8-pin DFN	-40 to +105 °C
5PB1106CMGI		Cut Tape	16-pin QFN	-40 to +105 °C
5PB1106CMGI8		Tape and Reel	16-pin QFN	-40 to +105 °C
5PB1108CMGI		Cut Tape	16-pin QFN	-40 to +105 °C
5PB1108CMGI8		Tape and Reel	16-pin QFN	-40 to +105 °C
5PB1110NDGI		Tubes	20-pin QFN	-40 to +105 °C
5PB1110NDGI8	Tape and Reel	20-pin QFN	-40 to +105 °C	

“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History

Rev.	Date	Originator	Description of Change
A	03/20/15	B. Chandhoke	Initial release.
B	05/19/15	B. Chandhoke	1. Expanded Output Enable function text in General Description, and within the note under "Output Logic Table". 2. Updated all "Buffer Additive Phase Jitter, RMS" conditions from 125MHz to 156.25MHz.
C	06/09/15	B. Chandhoke	1. Corrected typos in part numbers in DC Electrical Tables. 2. Updated existing Output Rise/Fall Time specs for 5pF load. 3. Added additional Output Rise/Fall specs for 2 pF load.
D	06/15/15	B. Chandhoke	Fixed typos in Output Rise/Fall Time 5pF specs for CL conditions; should be 5pF; not 2pF.
E	06/22/15	B. Chandhoke	Changed 3.3V Operating Voltage spec from 3.15 min to 3.135 min; 3.45 max to 3.465 max.
F	08/24/15	B. Chandhoke	1. Added 5PB1104CMGIW orderable part. 2. Updated Abs Max Ratings table for "Output Enable and All outputs" and "CLKIN"; changed -0.5 V to -0.4 and added -0.4 to... respectively.
G	05/13/16	H.G.	Replace NDG20 POD drawing with latest version.



Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com

Tech Support
email: clocks@idt.com

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