



Table 1. Pin Descriptions

| Name                 | Type   |                              | Description                                                                                                                                                                                                                                                                                       |
|----------------------|--------|------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A[1:2]               | Input  | Adjustable <sup>(1, 4)</sup> | Clock input. A[1:2] is the "true" side of the differential clock input.                                                                                                                                                                                                                           |
| $\overline{A[1:2]}$  | Input  | Adjustable <sup>(1, 4)</sup> | Complementary clock inputs. $\overline{A[1:2]}$ is the complementary side of A[1:2]. For LVTTTL single-ended operation, A[1:2] should be set to the desired toggle voltage for A[1:2]:<br>3.3V LVTTTL VREF = 1650mV<br>2.5V LVTTTL VREF = 1250mV                                                  |
| $\overline{G1}$      | Input  | LVTTTL                       | Gate control for differential outputs Q1 and $\overline{Q1}$ through Q5 and $\overline{Q5}$ . When $\overline{G1}$ is LOW, the differential outputs are active. When $\overline{G1}$ is HIGH, the differential outputs are asynchronously driven to the level designated by GL <sup>(2)</sup> .   |
| $\overline{G2}$      | Input  | LVTTTL                       | Gate control for differential outputs Q6 and $\overline{Q6}$ through Q10 and $\overline{Q10}$ . When $\overline{G2}$ is LOW, the differential outputs are active. When $\overline{G2}$ is HIGH, the differential outputs are asynchronously driven to the level designated by GL <sup>(2)</sup> . |
| GL                   | Input  | LVTTTL                       | Specifies output disable level. If HIGH, "true" outputs disable HIGH and "complementary" outputs disable LOW. If LOW, "true" outputs disable LOW and "complementary" outputs disable HIGH.                                                                                                        |
| Q[1:10]              | Output | LVDS                         | Clock outputs.                                                                                                                                                                                                                                                                                    |
| $\overline{Q[1:10]}$ | Output | LVDS                         | Complementary clock outputs.                                                                                                                                                                                                                                                                      |
| SEL                  | Input  | LVTTTL                       | Reference clock select. When LOW, selects A2 and $\overline{A2}$ . When HIGH, selects A1 and $\overline{A1}$ .                                                                                                                                                                                    |
| $\overline{PD}$      | Input  | LVTTTL                       | Power-down control. Shuts off entire chip. If LOW, the device goes into LOW power mode. Inputs and outputs are disabled. Both "true" and "complementary" outputs will pull to VDD. Set HIGH for normal operation. <sup>(3)</sup>                                                                  |
| FSEL                 | Input  | LVTTTL                       | At a rising edge, FSEL forces select to the input designated by SEL. Apply a LOW-to-HIGH transition to force an input selection. Set to logic LOW level at startup and if a forced input selection is not needed.                                                                                 |
| V <sub>DD</sub>      |        | Power                        | Power supply for the device core and inputs.                                                                                                                                                                                                                                                      |
| GND                  |        | Power                        | Ground.                                                                                                                                                                                                                                                                                           |

## NOTES:

- Inputs are capable of translating the following interface standards:  
Single-ended 3.3V and 2.5V LVTTTL levels  
Differential HSTL and eHSTL levels  
Differential LVEPECL (2.5V) and LVPECL (3.3V) levels  
Differential LVDS levels  
Differential CML levels
- Because the gate controls are asynchronous, runt pulses are possible. It is the user's responsibility to either time the gate control signals to minimize the possibility of runt pulses or be able to tolerate them in down stream circuitry.
- It is recommended that the outputs be disabled before entering power-down mode. It is also recommended that the outputs remain disabled until the device completes power-up after asserting  $\overline{PD}$ .
- The user must take precautions with any differential input interface standard being used in order to prevent instability when there is no input signal.

Table 2. Pin Characteristics (T<sub>A</sub> = +25°C, F = 1.0MHz)

| Symbol          | Parameter         | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-------------------|-----------------|---------|---------|---------|-------|
| C <sub>IN</sub> | Input Capacitance |                 |         |         | 3       | pF    |

NOTE: This parameter is measured at characterization but not tested.

## Function Tables

Table 3A. Gate Control Output Table

| Control Outputs |                | Outputs  |                      |
|-----------------|----------------|----------|----------------------|
| GL              | $\overline{G}$ | Q[1:16]  | $\overline{Q[1:16]}$ |
| 0               | 0              | Toggling | Toggling             |
| 0               | 1              | LOW      | HIGH                 |
| 1               | 0              | Toggling | Toggling             |
| 1               | 1              | HIGH     | LOW                  |

Table 3B. Input Selection Table

| Selection SEL pin | Inputs              |
|-------------------|---------------------|
| 0                 | A2/ $\overline{A2}$ |
| 1                 | A1/ $\overline{A1}$ |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item                                        | Rating                  |
|---------------------------------------------|-------------------------|
| Power Supply Voltage, $V_{DD}$              | -0.5V to +3.6V          |
| Input Voltage, $V_I$                        | -0.5V to +3.6V          |
| Output Voltage, $V_O$<br>Not to exceed 3.6V | -0.5 to $V_{DD} + 0.5V$ |
| Storage Temperature, $T_{STG}$              | -65°C to +150°C         |
| Junction Temperature, $T_J$                 | 150°C                   |

## Recommended Operating Range

| Symbol   | Description                   | Minimum | Typical | Maximum | Units |
|----------|-------------------------------|---------|---------|---------|-------|
| $T_A$    | Ambient Operating Temperature | -40     | +25     | +85     | °C    |
| $V_{DD}$ | Internal Power Supply Voltage | 2.3     | 2.5     | 2.7     | V     |

## DC Electrical Characteristics

**Table 4A. LVDS Power Supply DC Characteristics<sup>(1)</sup>,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

| Symbol    | Parameter                                  | Test Conditions                                                                     | Minimum | Typical <sup>(2)</sup> | Maximum | Units |
|-----------|--------------------------------------------|-------------------------------------------------------------------------------------|---------|------------------------|---------|-------|
| $I_{DDQ}$ | Quiescent $V_{DD}$<br>Power Supply Current | $V_{DD} = \text{Max.}$ ,<br>All Input Clocks = LOW <sup>(2)</sup> ; Outputs enabled |         |                        | 295     | mA    |
| $I_{TOT}$ | Total Power<br>$V_{DD}$ Supply Current     | $V_{DD} = 2.7V$ ;<br>$F_{\text{REFERENCE}}$ Clock = 650MHz                          |         |                        | 305     | mA    |
| $I_{PD}$  | Total Power Down<br>Supply Current         | $\overline{PD} = \text{LOW}$                                                        |         |                        | 5       | mA    |

NOTE 1: These power consumption characteristics are for all the valid input interfaces and cover the worst case conditions.

NOTE 2: The true input is held LOW and the complementary input is held HIGH.

**Table 4B. LVTTTL DC Characteristics<sup>(1)</sup>**,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ 

| Symbol    | Parameter                                     | Test Conditions                                  | Minimum | Typical <sup>(2)</sup> | Maximum | Units         |
|-----------|-----------------------------------------------|--------------------------------------------------|---------|------------------------|---------|---------------|
| $I_{IH}$  | Input High Current                            | $V_{DD} = 2.7\text{V}$                           |         |                        | $\pm 5$ | $\mu\text{A}$ |
| $I_{IL}$  | Input Low Current                             | $V_{DD} = 2.7\text{V}$                           |         |                        | $\pm 5$ | $\mu\text{A}$ |
| $V_{IK}$  | Clamp Diode Voltage                           | $V_{DD} = 2.3\text{V}$ , $I_{IN} = -18\text{mA}$ |         | -0.7                   | -1.2    | V             |
| $V_{IN}$  | DC Input Voltage                              |                                                  | -0.3    |                        | 3.6     | V             |
| $V_{IH}$  | DC Input High Voltage                         |                                                  | 1.7     |                        |         | V             |
| $V_{IL}$  | DC Input Low Voltage                          |                                                  |         |                        | 0.7     | V             |
| $V_{THI}$ | DC Input Threshold Crossing Voltage           |                                                  |         | $V_{DD}/2$             |         | V             |
| $V_{REF}$ | Single-Ended Reference Voltage <sup>(3)</sup> | 3.3V LVTTTL                                      |         | 1.65                   |         | V             |
|           |                                               | 2.5V LVTTTL                                      |         | 1.25                   |         | V             |

NOTE 1: See *Recommended Operating Range* table.NOTE 2: Typical values are at  $V_{DD} = 2.5\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.NOTE 3: For A[1:2] single-ended operation,  $\bar{A}[1:2]$  is tied to a DC reference voltage.**Table 4C. Differential DC Characteristics<sup>(1)</sup>**,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ 

| Symbol    | Parameter                              | Test Conditions                                  | Minimum | Typical <sup>(2)</sup> | Maximum  | Units         |
|-----------|----------------------------------------|--------------------------------------------------|---------|------------------------|----------|---------------|
| $I_{IH}$  | Input High Current                     | $V_{DD} = 2.7\text{V}$                           |         |                        | $\pm 5$  | $\mu\text{A}$ |
| $I_{IL}$  | Input Low Current                      | $V_{DD} = 2.7\text{V}$                           |         |                        | $\pm 5$  | $\mu\text{A}$ |
| $V_{IK}$  | Clamp Diode Voltage                    | $V_{DD} = 2.3\text{V}$ , $I_{IN} = -18\text{mA}$ |         | -0.7                   | -1.2     | V             |
| $V_{IN}$  | DC Input Voltage                       |                                                  | -0.3    |                        | 3.6      | V             |
| $V_{DIF}$ | DC Differential Voltage <sup>(3)</sup> |                                                  | 0.1     |                        |          | V             |
| $V_{CM}$  | DC Common Mode Input Voltage           |                                                  | 0.05    |                        | $V_{DD}$ | V             |

NOTE 1: See *Recommended Operating Range* table.NOTE 2:  $V_{DIF}$  specifies the minimum input differential voltage ( $V_{TR} - V_{CP}$ ) required for switching where  $V_{TR}$  is the "true" input level and  $V_{CP}$  is the "complement" input level. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.NOTE 3:  $V_{CM}$  specifies the maximum allowable range of  $(V_{TR} + V_{CP}) / 2$ .NOTE 4: Typical values are at  $V_{DD} = 2.5\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.

**Table 4D. LVDS DC Characteristics<sup>(1)</sup>,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol          | Parameter                                              | Test Conditions                | Minimum | Typical <sup>(2)</sup> | Maximum | Units |
|-----------------|--------------------------------------------------------|--------------------------------|---------|------------------------|---------|-------|
| $V_{OT(+)}$     | Differential Output Voltage for the True Binary State  |                                | 247     |                        | 454     | mV    |
| $V_{OT(-)}$     | Differential Output Voltage for the False Binary State |                                | 247     |                        | 454     | mV    |
| $\Delta V_{OT}$ | Change in $V_{OT}$ Between Complementary Output States |                                |         |                        | 50      | mV    |
| $V_{OS}$        | Output Common Mode Voltage (Offset Voltage)            |                                | 1.125   | 1.2                    | 1.375   | V     |
| $\Delta V_{OS}$ | Change in $V_{OS}$ Between Complementary Output States |                                |         |                        | 50      | mV    |
| $I_{OS}$        | Outputs Short Circuit Current                          | $V_{OUT+}$ and $V_{OUT-} = 0V$ |         | 12                     | 24      | mA    |
| $I_{OSD}$       | Differential Outputs Short Circuit Current             | $V_{OUT+} = V_{OUT-}$          |         | 6                      | 12      | mA    |

NOTE 1: See *Recommended Operating Range* table.NOTE 2: Typical values are at  $V_{DD} = 2.5V$ ,  $+25^\circ\text{C}$  ambient.

## AC Electrical Characteristics

**Table 5A. HSTL Differential Input AC Characteristics,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol      | Parameter                                               | Value          | Units |
|-------------|---------------------------------------------------------|----------------|-------|
| $V_{DIF}$   | Input Signal Swing <sup>(1)</sup>                       | 1              | V     |
| $V_X$       | Differential Input Signal Crossing Point <sup>(2)</sup> | 750            | mV    |
| $D_H$       | Duty Cycle                                              | 50             | %     |
| $V_{THI}$   | Input Timing Measurement Reference Level <sup>(3)</sup> | Crossing Point | V     |
| $t_R / t_F$ | Input Signal Edge Rate <sup>(4)</sup>                   | 2              | V/ns  |

NOTE 1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the  $V_{DIF}$  (AC) specification under actual use conditions.NOTE 2. A 750mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the  $V_X$  specification under actual use conditions.

NOTE 3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.

NOTE 4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

**Table 5B. eHSTL AC Differential Input Characteristics,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol      | Parameter                                               | Value          | Units |
|-------------|---------------------------------------------------------|----------------|-------|
| $V_{DIF}$   | Input Signal Swing <sup>(1)</sup>                       | 1              | V     |
| $V_X$       | Differential Input Signal Crossing Point <sup>(2)</sup> | 900            | mV    |
| $D_H$       | Duty Cycle                                              | 50             | %     |
| $V_{THI}$   | Input Timing Measurement Reference Level <sup>(3)</sup> | Crossing Point | V     |
| $t_R / t_F$ | Input Signal Edge Rate <sup>(4)</sup>                   | 2              | V/ns  |

NOTE 1.The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the  $V_{DIF}$  (AC) specification under actual use conditions.

NOTE 2.A 900mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the  $V_X$  specification under actual use conditions.

NOTE 3.In all cases, input waveform timing is marked at the differential cross-point of the input signals.

NOTE 4.The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

**Table 5C. LVEPECL (2.5V) and LVPECL (3.3V) Differential Input AC Characteristics,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol                          | Parameter                                               |         | Maximum        | Units |
|---------------------------------|---------------------------------------------------------|---------|----------------|-------|
| V <sub>DIF</sub>                | Input Signal Swing <sup>(1)</sup>                       |         | 732            | mV    |
| V <sub>X</sub>                  | Differential Input Signal Crossing Point <sup>(2)</sup> | LVEPECL | 1082           | mV    |
|                                 |                                                         | LVPECL  | 1880           | m     |
| D <sub>H</sub>                  | Duty Cycle                                              |         | 50             | %     |
| V <sub>THI</sub>                | Input Timing Measurement Reference Level <sup>(3)</sup> |         | Crossing Point | V     |
| t <sub>R</sub> / t <sub>F</sub> | Input Signal Edge Rate <sup>(4)</sup>                   |         | 2              | V/ns  |

NOTE 1.The 732mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the  $V_{DIF}$  (AC) specification under actual use conditions.

NOTE 2.A 1082mV LVEPECL (2.5V) and 1880mV LVPECL (3.3V) crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the  $V_X$  specification under actual use conditions.

NOTE 3.In all cases, input waveform timing is marked at the differential cross-point of the input signals.

NOTE 4.The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

**Table 5D. LVDS Differential Input AC Characteristics,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol      | Parameter                                               | Maximum        | Units |
|-------------|---------------------------------------------------------|----------------|-------|
| $V_{DIF}$   | Input Signal Swing <sup>(1)</sup>                       | 400            | mV    |
| $V_X$       | Differential Input Signal Crossing Point <sup>(2)</sup> | 1.2            | V     |
| $D_H$       | Duty Cycle                                              | 50             | %     |
| $V_{THI}$   | Input Timing Measurement Reference Level <sup>(3)</sup> | Crossing Point | V     |
| $t_R / t_F$ | Input Signal Edge Rate <sup>(4)</sup>                   | 2              | V/ns  |

NOTE 1.The 400mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the  $V_{DIF}$  (AC) specification under actual use conditions.

NOTE 2.A 1.2mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the  $V_X$  specification under actual use conditions.

NOTE 3.In all cases, input waveform timing is marked at the differential cross-point of the input signals.

NOTE 4.The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

**Table 5E. AC Differential Input Characteristics<sup>(1)</sup>,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol    | Parameter                                      | Minimum | Typical | Maximum  | Units |
|-----------|------------------------------------------------|---------|---------|----------|-------|
| $V_{DIF}$ | AC Differential Voltage <sup>(2)</sup>         | 0.1     |         | 3.6      | V     |
| $V_{IX}$  | Differential Input Crosspoint Voltage          | 0.05    |         | $V_{DD}$ | V     |
| $V_{CM}$  | Common Mode Input Voltage Range <sup>(3)</sup> | 0.05    |         | $V_{DD}$ | V     |
| $V_{IN}$  | Input Voltage                                  | -0.3    |         | +3.6     | V     |

NOTE 1. The output will not change state until the inputs have crossed and the minimum differential voltage range defined by  $V_{DIF}$  has been met or exceeded.

NOTE 2.  $V_{DIF}$  specifies the minimum input voltage ( $V_{TR} - V_{CP}$ ) required for switching where  $V_{TR}$  is the “true” input level and  $V_{CP}$  is the “complement” input level. The AC differential voltage must be achieved to guarantee switching to a new state.

NOTE 3.  $V_{CM}$  specified the maximum allowable range of  $(V_{TR} + V_{CP}) / 2$ .

**Table 5F. AC Characteristics<sup>(1,5)</sup>,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol      | Parameter                                                                                          | Test Conditions                                    | Minimum | Typical | Maximum | Units         |
|-------------|----------------------------------------------------------------------------------------------------|----------------------------------------------------|---------|---------|---------|---------------|
| $tsk(o)$    | Same Device Output Pin-to-Pin Skew <sup>(2)</sup>                                                  |                                                    |         |         | 25      | ps            |
| $tsk(p)$    | Pulse Skew <sup>(3)</sup>                                                                          |                                                    |         |         | 100     | ps            |
| $tsk(pp)$   | Part-to-Part Skew <sup>(4)</sup>                                                                   |                                                    |         |         | 300     | ps            |
| $tp_{LH}$   | Propagation Delay, Low-to-High                                                                     | $A/\bar{A}$ Crosspoint to $Qn/\bar{Qn}$ Crosspoint |         | 1.5     | 2       | ns            |
| $tp_{HL}$   | Propagation Delay, High-to-Low                                                                     |                                                    |         | 1.5     | 2       | ns            |
| $f_o$       | Frequency Range <sup>(6)</sup>                                                                     |                                                    |         |         | 650     | MHz           |
| $t_{PGE}$   | Output Gate Enable Crossing $V_{THI}$ -to- $Qn/\bar{Qn}$ Crosspoint                                |                                                    |         |         | 3.5     | ns            |
| $t_{PGD}$   | Output Gate Disable Crossing $V_{THI}$ -to- $Qn/\bar{Qn}$ Crosspoint Driven to GL Designated Level |                                                    |         |         | 3.5     | ns            |
| $t_{PWRDN}$ | $\overline{PD}$ Crossing $V_{THI}$ -to- $Qn = V_{DD}$ , $\bar{Qn} = V_{DD}$                        |                                                    |         |         | 100     | $\mu\text{S}$ |
| $t_{PWRUP}$ | Output Gate Disable Crossing $V_{THI}$ to $Qn/\bar{Qn}$ Driven to GL Designated Level              |                                                    |         |         | 100     | $\mu\text{S}$ |

NOTE 1. AC propagation measurements should not be taken within the first 100 cycles of startup.

NOTE 2. Skew measured between crosspoints of all differential output pairs under identical input and output interfaces, transitions and load conditions on any one device.

NOTE 3. Skew measured is the difference between propagation delay times  $tp_{HL}$  and  $tp_{LH}$  of any single differential output pair under identical input and output interfaces, transitions and load conditions on any one device.

NOTE 4. Skew measured is the magnitude of the difference in propagation times between any single differential output pair of two devices, given identical transitions and load conditions at identical  $V_{DD}$  levels and temperature.

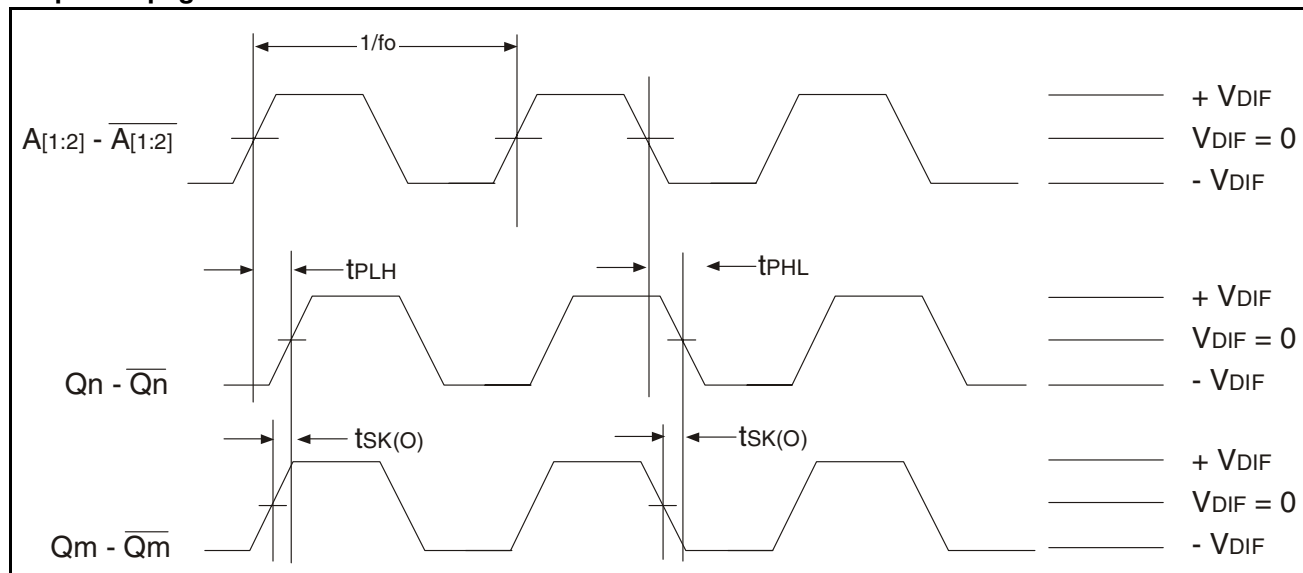
NOTE 5. All parameters are tested with a 50% input duty cycle.

NOTE 6. Guaranteed by design but not production tested.



## Differential AC Timing Waveforms

### Output Propagation and Skew Waveforms



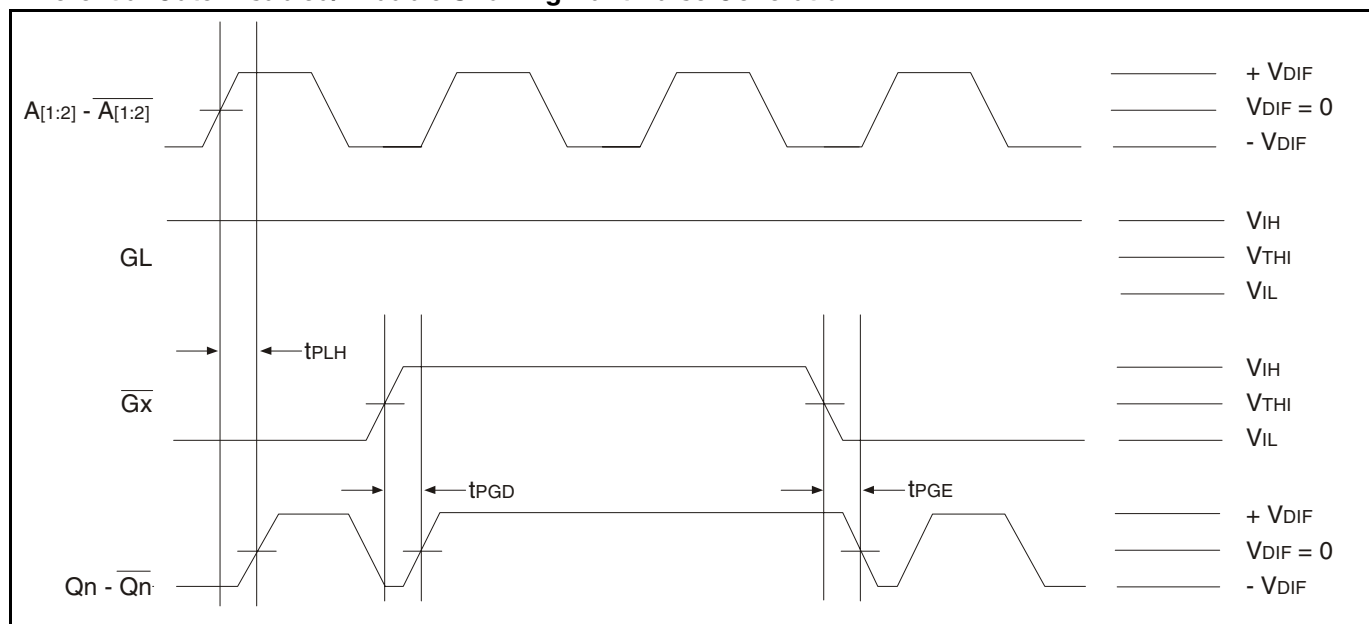
NOTE 1: Pulse skew is calculated using the following expression:

$$t_{sk(p)} = |t_{p_{HL}} - t_{p_{LH}}|$$

Note that the  $t_{p_{HL}}$  and  $t_{p_{LH}}$  shown above are not valid measurements for this calculation because they are not taken from the same pulse.

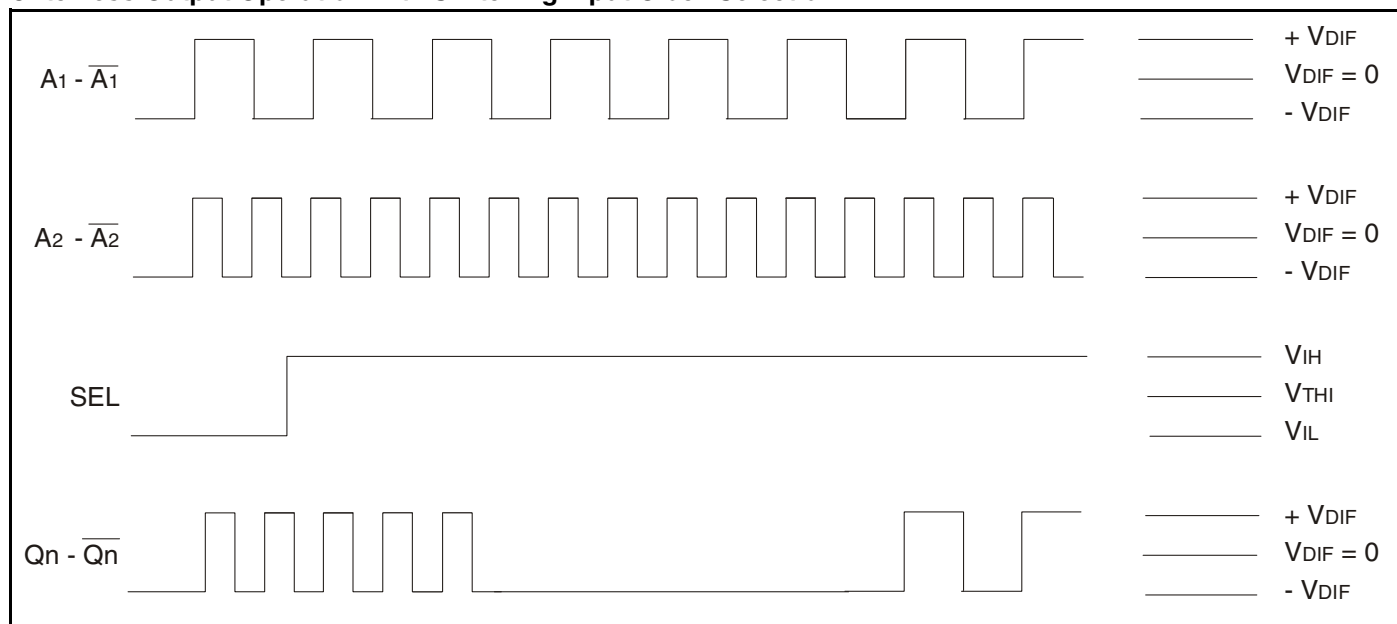
NOTE 2: AC propagation measurements should not be taken within the first 100 cycles of startup.

### Differential Gate Disabled/Endable Showing Runt Pulse Generation



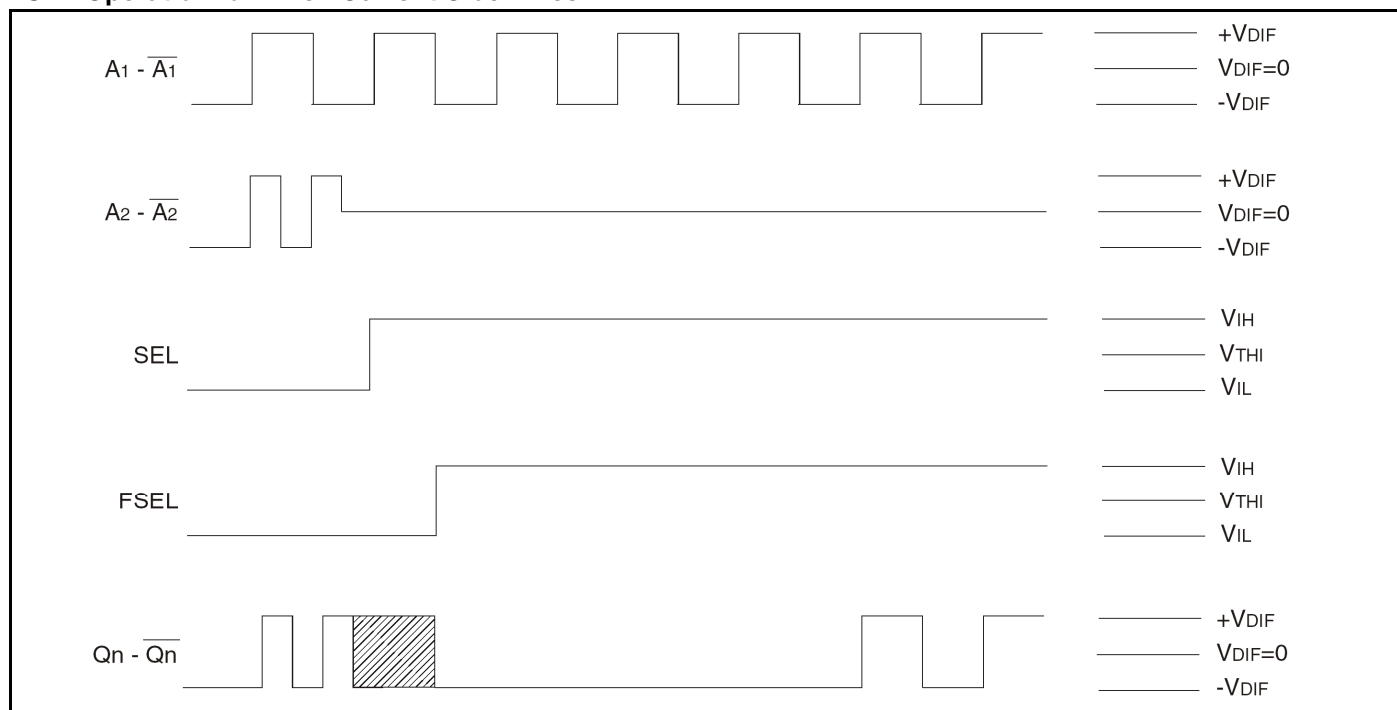
NOTE 1: As shown, it is possible to generate runt pulses on gate disable and enable of the outputs. It is the user's responsibility to time the  $\overline{G}$  signal to avoid this problem.

### Glitchless Output Operation with Switching Input Clock Selection



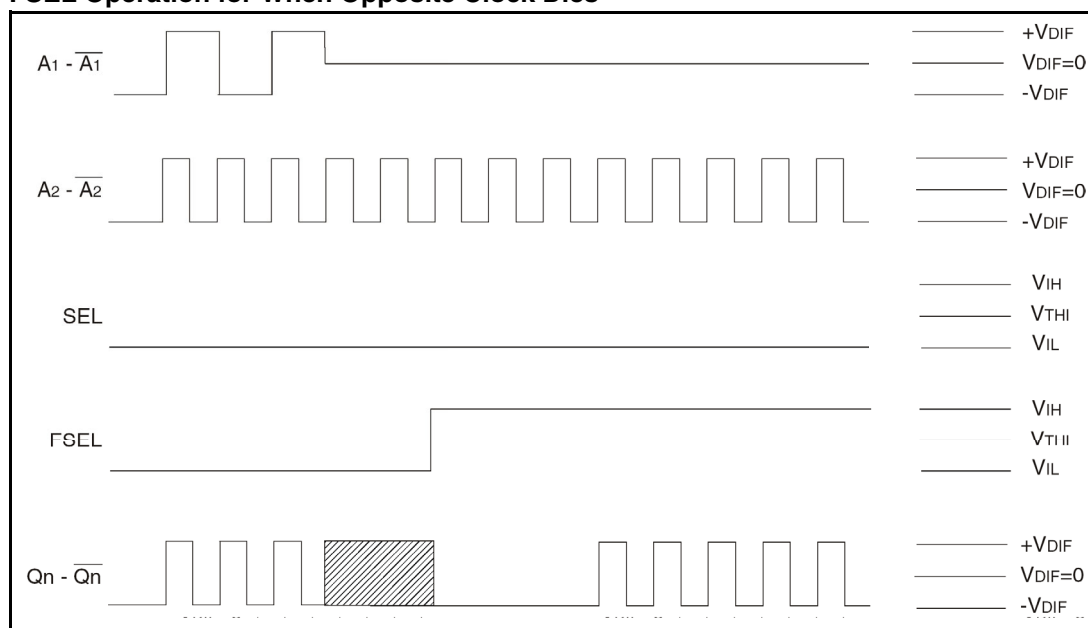
1. When SEL changes, the output clock goes LOW on the falling edge of the output clock up to three cycles later. The output then stays LOW for up to three clock cycles of the new input clock. After this, the output starts with the rising edge of the new input clock.
2. AC propagation measurements should not be taken within the first 100 cycles of startup.

### FSEL Operation for When Current Clock Dies



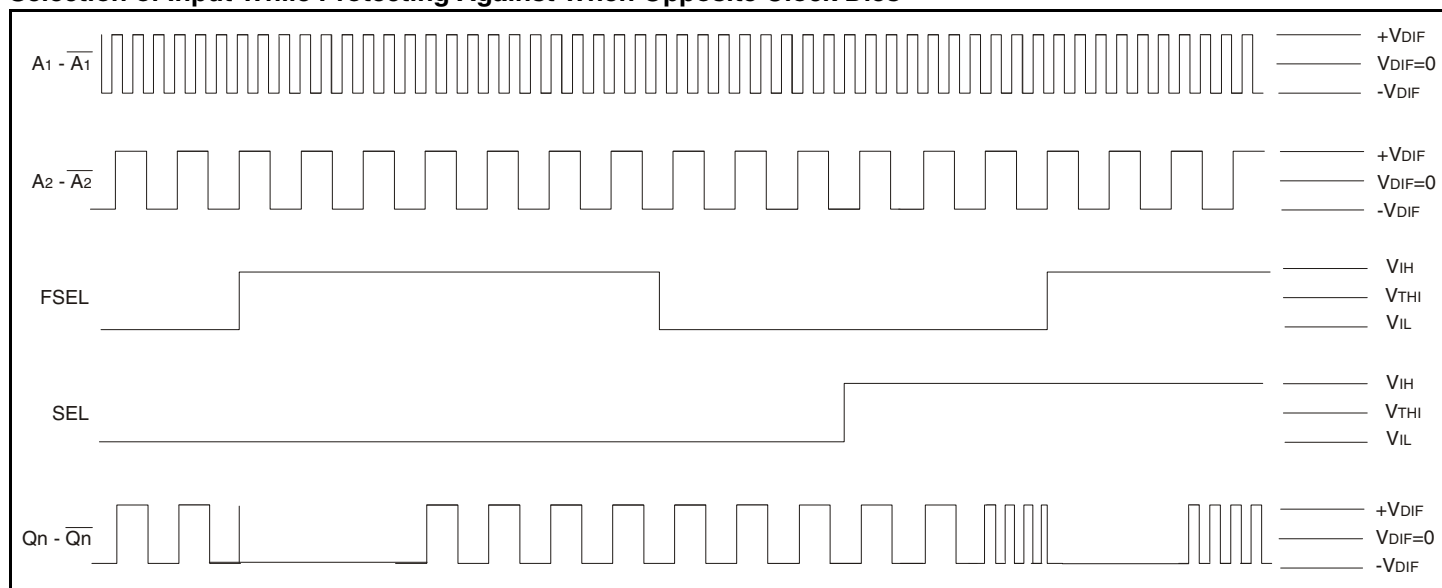
1. When the differential on the selected clock goes below the minimum DC differential, the outputs clock goes to an unknown state. When this happens, the SEL pin should be toggled and FSEL asserted in order to force selection of the new input clock. The output clock will start up after a number of cycles of the newly-selected input clock.
2. The FSEL pin should stay asserted until the problem with the dead clock can be fixed in the system.
3. It is recommended that the FSEL be tied LOW for systems that use only one input. If this is not possible, the user must guarantee that the unused input have a differential greater than or equal to the minimum DC differential specified in the datasheet.

## FSEL Operation for When Opposite Clock Dies



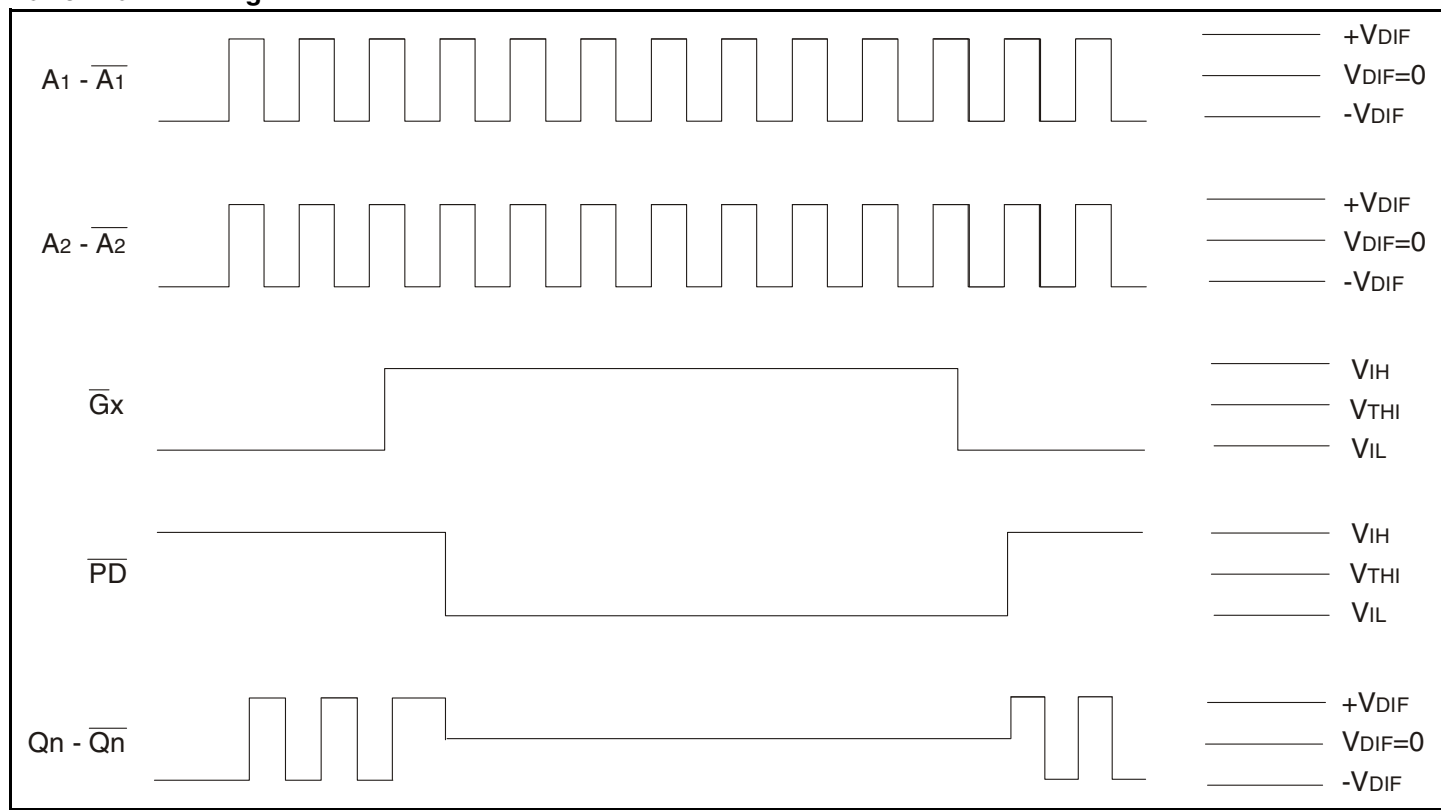
1. When the differential on the non-selected clock goes below the minimum DC differential, the outputs clock goes to an unknown state. When this happens, the FSEL pin should be asserted in order to force selection of the new input clock. The output clock will start up after a number of cycles of the newly-selected input clock.
2. The FSEL pin should stay asserted until the problem with the dead clock can be fixed in the system.
3. It is recommended that the FSEL be tied LOW for systems that use only one input. If this is not possible, the user must guarantee that the unused input have a differential greater than or equal to the minimum DC differential specified in the datasheet.

## Selection of Input While Protecting Against When Opposite Clock Dies



1. If the user holds FSEL HIGH, the output will not be affected by the deselected input clock.
2. The output will immediately be driven to LOW once FSEL is asserted. This may cause glitching on the output. The output will restart with the input clock selected by the SEL pin.
3. If the user decides to switch input clocks, the user must de-assert FSEL, then assert FSEL after toggling the SEL input pin. The output will be driven LOW and will restart with the input clock selected by the SEL pin.

## Power Down Timing



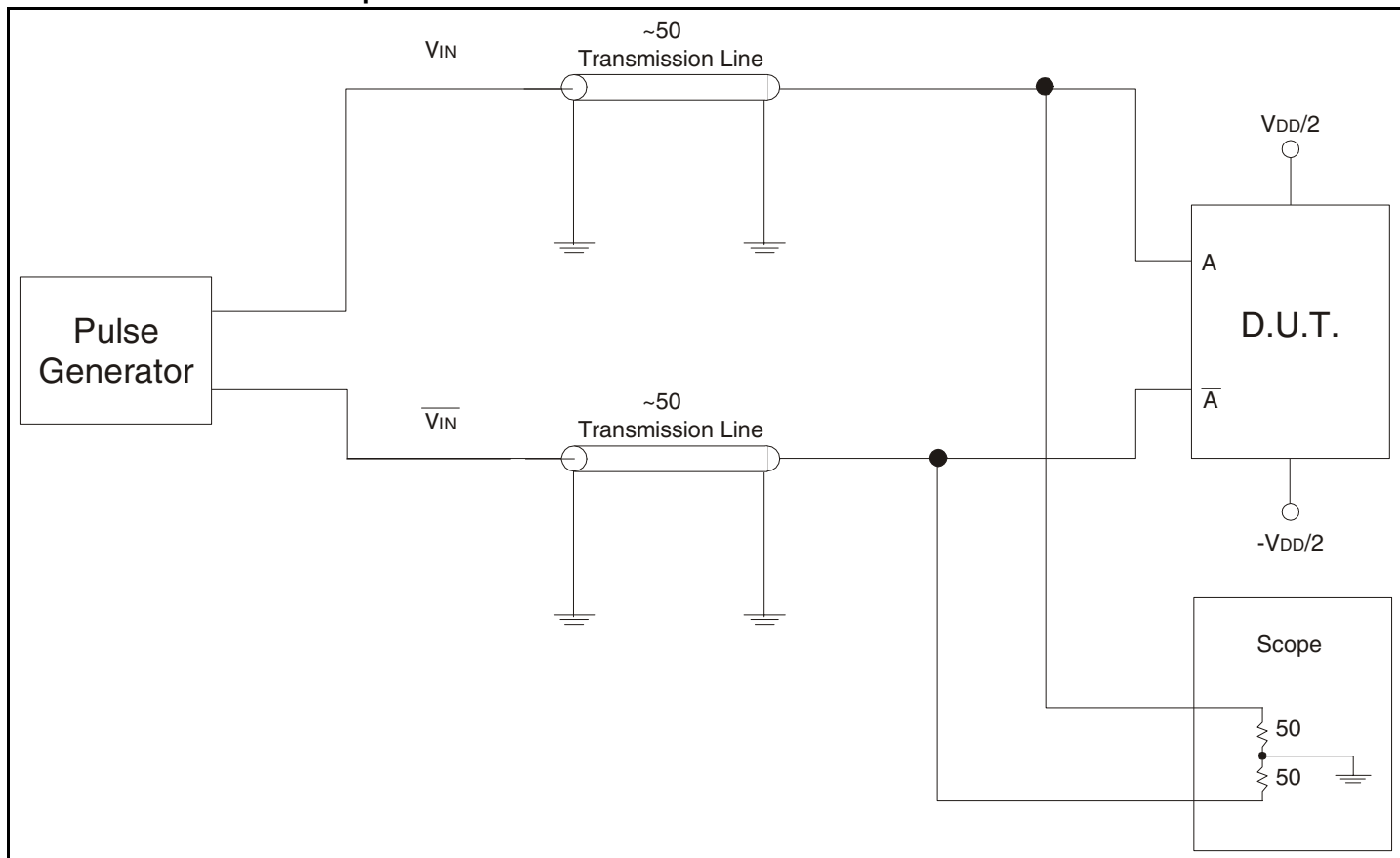
NOTE 1: It is recommended that outputs be disabled before entering power-down mode. It is also recommended that the outputs remain disabled until the device completes power-up after asserting  $\overline{PD}$ .

NOTE 2: The *Power Down Timing* diagram assumes that GL is HIGH.

NOTE 3: It should be noted that during power-down mode, the outputs are both pulled to  $V_{DD}$ . In the *Power Down Timing* diagram this is shown when  $Qn/\overline{Qn}$  goes to  $V_{DIF} = 0$ .

## Test Circuits and Conditions

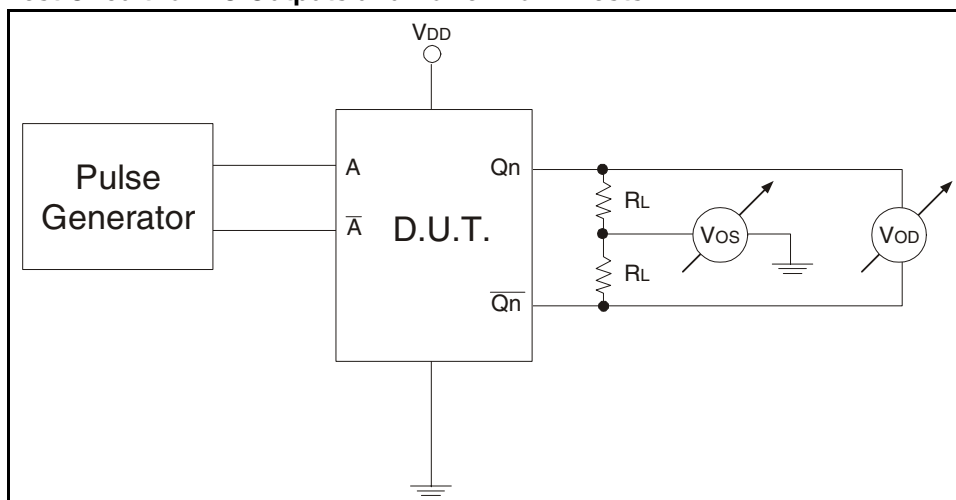
### Test Circuit for Differential Input



**Table 6A. Differential Input Test Conditions**

| Symbol    | $V_{DD} = 2.5V \pm 0.2V$         | Unit |
|-----------|----------------------------------|------|
| $V_{THI}$ | Crossing of A and $\overline{A}$ | V    |

## Test Circuit for DC Outputs and Power Down Tests



## Test Circuit for Propagation, Skew, and Gate Enable/Disable Timing

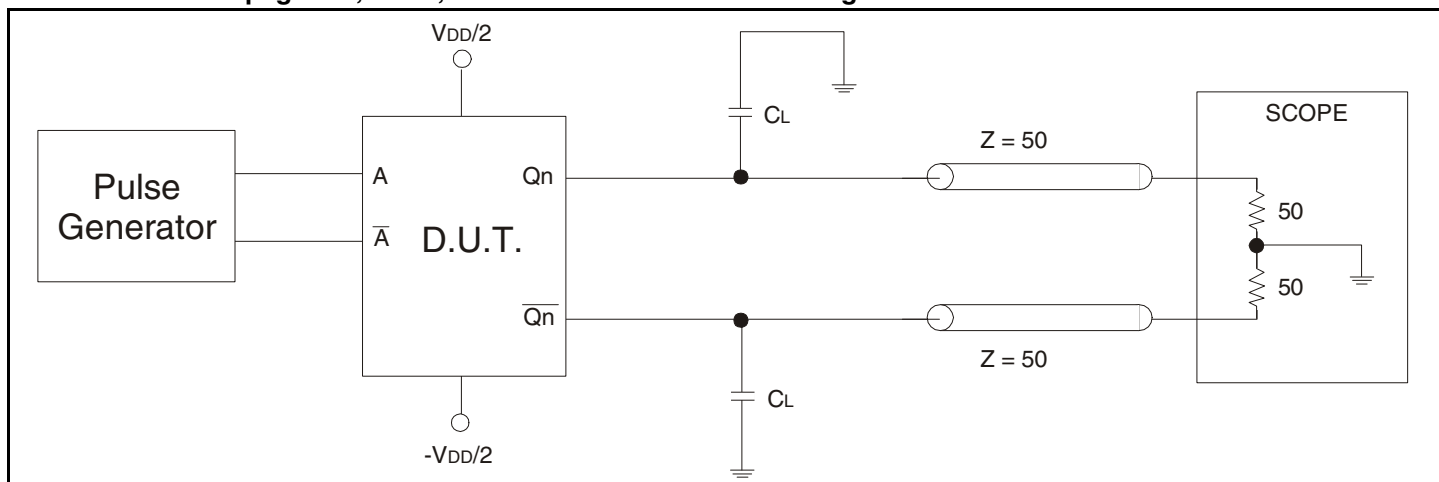


Table 6B. LVDS Output Test Conditions

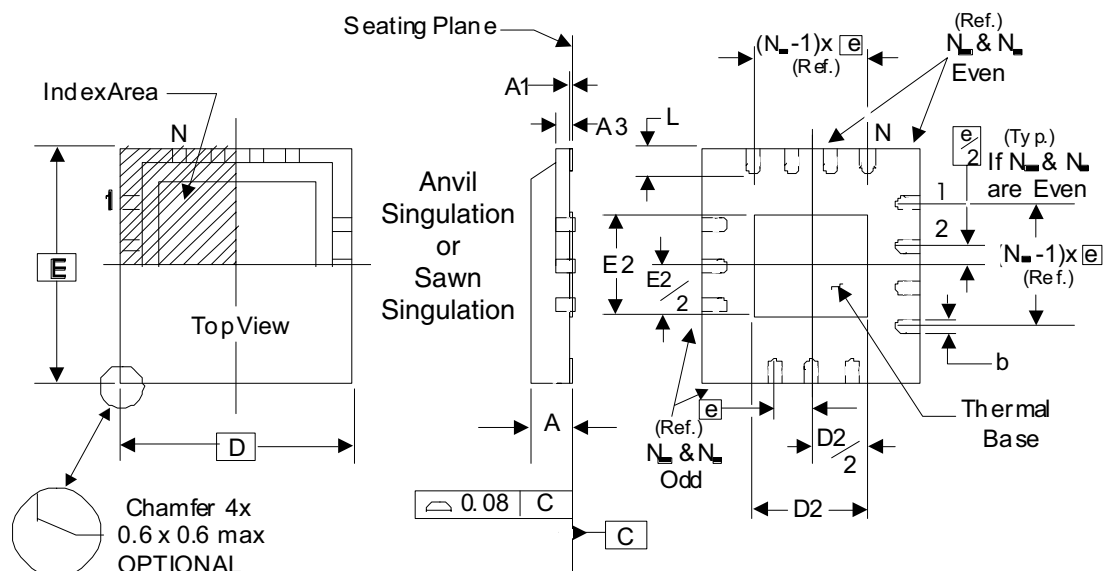
| Symbol | $V_{DD} = 2.5V \pm 0.2V$ | Unit     |
|--------|--------------------------|----------|
| $C_L$  | 0 <sup>(1)</sup>         | pF       |
|        | 8 <sup>(1,2)</sup>       | pF       |
| $R_L$  | 50                       | $\Omega$ |

NOTE 1: Specifications only apply to "Normal Operations" test condition. The  $T_{IA}/E_{IA}$  specification load is for reference only.

NOTE 2: The scope inputs are assumed to have a 2pF load to ground.  $T_{IA}/E_{IA} - 644$  specifies 5pF between the output pair. With  $C_L = 8pF$ , this gives the test circuit appropriate 5pF equivalent load.

## Package Outline and Package Dimensions

### Package Outline - K Suffix for 40 Lead VFQFPN



**Table 7. Package Dimensions**

| JEDEC Variation: VJJD-2/-5<br>All Dimensions in Millimeters |            |         |
|-------------------------------------------------------------|------------|---------|
| Symbol                                                      | Minimum    | Maximum |
| $N$                                                         | 40         |         |
| $A$                                                         | 0.80       | 1.00    |
| $A1$                                                        | 0          | 0.05    |
| $A3$                                                        | 0.25 Ref.  |         |
| $b$                                                         | 0.18       | 0.30    |
| $N_D$ & $N_E$                                               | 10         |         |
| $D$ & $E$                                                   | 6.00 Basic |         |
| $D2$ & $E2$                                                 | 1.75       | 4.80    |
| $e$                                                         | 0.50 Basic |         |
| $L$                                                         | 0.30       | 0.50    |

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFPN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 7 below

Ordering Information

Table 8. Ordering Information

| IDT         | XXXXX   | XX      | X        |  |                                                                      |
|-------------|---------|---------|----------|--|----------------------------------------------------------------------|
| Device Type | Package | Process |          |  |                                                                      |
|             |         |         | I        |  | -40°C to +85°C (Industrial)                                          |
|             |         |         | NL       |  | Thermally Enhanced Plastic Very Fine Pitch Quad Flat No Lead Package |
|             |         |         | NLG      |  | VFQFPN - Green                                                       |
|             |         |         | 5T93GL10 |  | 2.5V LVDS 1:10 Glitchless Clock Buffer Terabuffer™ II                |



## Revision History Sheet

| Rev | Table          | Page    | Description of Change                                                                               | Date    |
|-----|----------------|---------|-----------------------------------------------------------------------------------------------------|---------|
| A   | T1<br>T3A, T3B | 1       | Features Section added bullet "Recommends IDT5T9310 if glitchless input selection is not required". | 3/16/09 |
|     |                | 2       | Pin Description Table - FSEL pin, replaced description text.                                        |         |
|     |                | 3       | Added Function Tables.                                                                              |         |
|     |                | 10 - 11 | NOTE 3, replaced "HIGH" with "LOW".                                                                 |         |
|     |                | 15      | Added Package Outline and Dimensions.                                                               |         |
|     |                | 17      | Converted datasheet format.                                                                         |         |
| A   |                |         | Changed VFQFN to VFQFPN through the datasheet.                                                      | 3/18/09 |

**IDT5T93GL10**

**2.5V LVDS 1:10 GLITCHLESS CLOCK BUFFER TERABUFFER™ II**

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