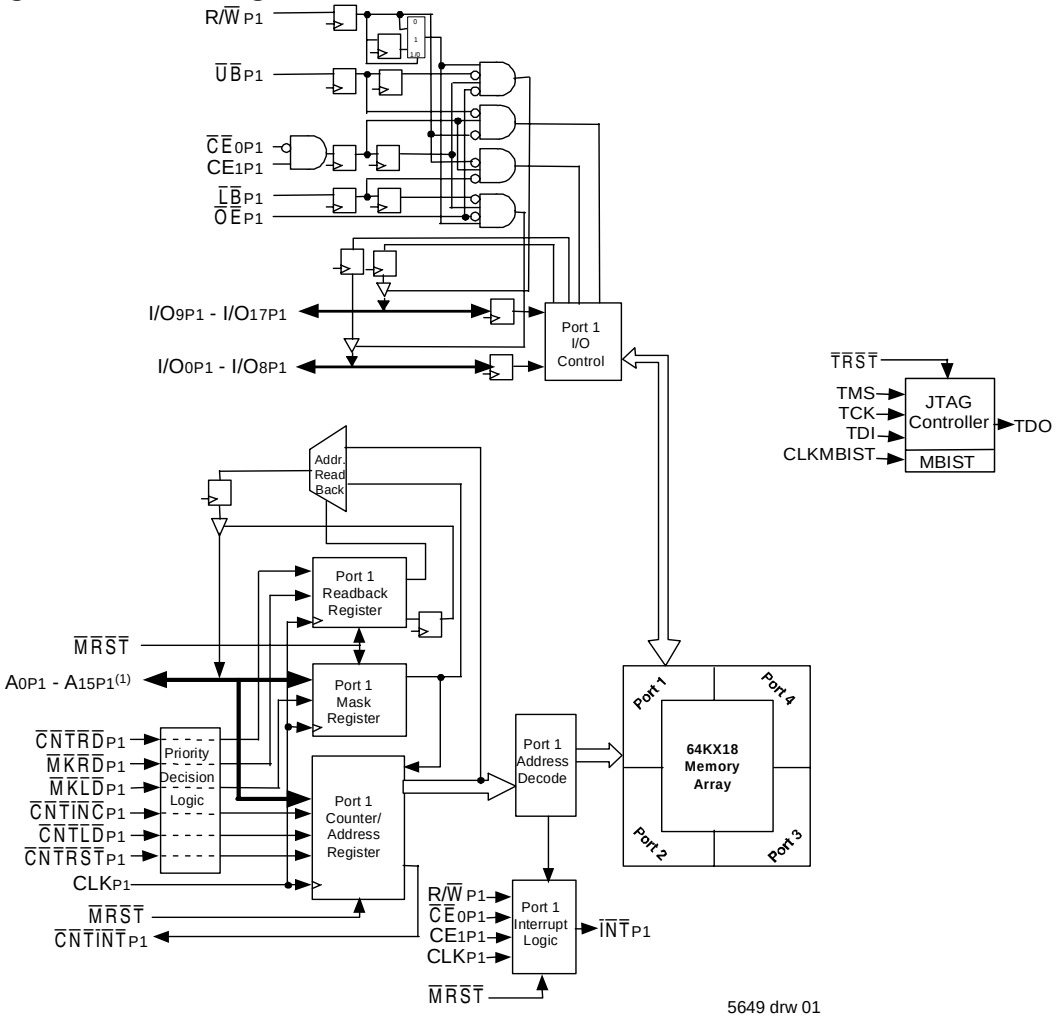
3.3V 64/32K X 18 SYNCHRONOUS FOURPORT™ STATIC RAM

IDT70V5388/78

Features

- **True four-ported memory cells which allow simultaneous access of the same memory location**
- **Synchronous Pipelined device**
  - *64/32K x 18 organization*
- **Pipelined output mode allows fast 200MHz operation**
- **High Bandwidth up to 14 Gbps (200MHz x 18 bits wide x 4 ports)**
- **LVTTL I/O interface**
- **High-speed clock to data access 3.0ns (max.)**
- **3.3V Low operating power**
- **Interrupt flags for message passing**
- **Width and depth expansion capabilities**
- **Counter readback on address lines**
- **Counter wrap-around control**
  - *Internal mask register controls counter wrap-around*
  - *Counter-Interrupt flags to indicate wrap-around*
- **Mask register readback on address lines**
- **Global Master reset for all ports**
- **Dual Chip Enables on all ports for easy depth expansion**
- **Separate upper-word and lower-word controls on all ports**
- **272-BGA package (27mm x 27mm 1.27mm ball pitch) and 256-BGA package (17mm x 17mm 1.0mm ball pitch)**
- **Commercial and Industrial temperature ranges**
- **JTAG boundary scan**
- **MBIST (Memory Built-In Self Test) controller**
- **Green parts available, see ordering information**

Port - 1 Logic Block Diagram(2)



5649 drw 01

NOTE:

1. A15X is a NC for IDT70V5378.
2. Port 2, Port 3, and Port 4 Logic Blocks are similar to Port 1 Logic Blocks.

JANUARY 2006

Description

The IDT70V5388/78 is a high-speed 64/32Kx18 bit synchronous FourPort RAM. The memory array utilizes FourPort memory cells to allow simultaneous access of any address from all four ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register and integrated burst counters, the 70V5388/78 has been optimized for applications having unidirectional or bi-directional data flow in bursts. An automatic power down feature, controlled by $\overline{CE}_0$ and CE_1, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT70V5388/78 provides a wide range of functions specially designed to facilitate system operations. These include full-boundary, maskable address counters with associated interrupts for each port, mailbox interrupt flags on each port to facilitate inter-port communications, Memory Built-In Self-Test (MBIST), JTAG support and an asynchronous Master Reset to simplify device initialization. In addition, the address lines have been set up as I/O pins, to permit the support of $\overline{CNTRD}$ (the ability to output the current value of the internal address counter on the address lines) and $\overline{MKRD}$ (the ability to output the current value of the counter mask register). For specific details on the device operation, please refer to the Functional Description and subsequent explanatory sections, beginning on page 21.

Pin Configuration[4]

70V5388/78BG
BG-272[2]

272-Pin BGA
Top View[3]

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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	$\overline{LB}$ P1	I/O17 P2	I/O15 P2	I/O13 P2	I/O11 P2	I/O9 P2	I/O16 P1	I/O14 P1	I/O12 P1	I/O10 P1	I/O10 P4	I/O12 P4	I/O14 P4	I/O16 P4	I/O9 P3	I/O11 P3	I/O13 P3	I/O15 P3	I/O17 P3	$\overline{LB}$ P4	A
B	VDD	$\overline{UB}$ P1	I/O16 P2	I/O14 P2	I/O12 P2	I/O10 P2	I/O17 P1	I/O13 P1	I/O11 P1	TMS	TDI	I/O11 P4	I/O13 P4	I/O17 P4	I/O10 P3	I/O12 P3	I/O14 P3	I/O16 P3	$\overline{UB}$ P4	VDD	B
C	A14 P1	A15[1] P1	CE1 P1	$\overline{CE}_0$ P1	R/$\overline{W}$ P1	I/O15 P1	VSS	VSS	I/O9 P1	TCK	TDO	I/O9 P4	VSS	VSS	I/O15 P4	R/$\overline{W}$ P4	$\overline{CE}_0$ P4	CE1 P4	A15[1] P4	A14 P4	C
D	VSS	A12 P1	A13 P1	$\overline{OE}$ P1	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	$\overline{OE}$ P4	A13 P4	A12 P4	VSS	D
E	A10 P1	A11 P1	$\overline{MKRD}$ P1	$\overline{CNTRD}$ P1													$\overline{CNTRD}$ P4	$\overline{MKRD}$ P4	A11 P4	A10 P4	E
F	A7 P1	A8 P1	A9 P1	$\overline{CNTINT}$ P1													$\overline{CNTINT}$ P4	A9 P4	A8 P4	A7 P4	F
G	VSS	A5 P1	A6 P1	$\overline{CNTINC}$ P1													$\overline{CNTINC}$ P4	A6 P4	A5 P4	VSS	G
H	A3 P1	A4 P1	$\overline{MKLD}$ P1	$\overline{CNTLD}$ P1													$\overline{CNTLD}$ P4	$\overline{MKLD}$ P4	A4 P4	A3 P4	H
J	VDD	A1 P1	A2 P1	VDD					GND[5]	GND[5]	GND[5]	GND[5]					VDD	A2 P4	A1 P4	VDD	J
K	A0 P1	$\overline{INT}$ P1	$\overline{CNTRST}$ P1	CLK P1					GND[5]	GND[5]	GND[5]	GND[5]					CLK P4	$\overline{CNTRST}$ P4	$\overline{INT}$ P4	A0 P4	K
L	A0 P2	$\overline{INT}$ P2	$\overline{CNTRST}$ P2	VSS					GND[5]	GND[5]	GND[5]	GND[5]					VSS	$\overline{CNTRST}$ P3	$\overline{INT}$ P3	A0 P3	L
M	VDD	A1 P2	A2 P2	CLK P2					GND[5]	GND[5]	GND[5]	GND[5]					CLK P3	A2 P3	A1 P3	VDD	M
N	A3 P2	A4 P2	$\overline{MKLD}$ P2	$\overline{CNTLD}$ P2													$\overline{CNTLD}$ P3	$\overline{MKLD}$ P3	A4 P3	A3 P3	N
P	VSS	A5 P2	A6 P2	$\overline{CNTINC}$ P2													$\overline{CNTINC}$ P3	A6 P3	A5 P3	VSS	P
R	A7 P2	A8 P2	A9 P2	$\overline{CNTINT}$ P2													$\overline{CNTINT}$ P3	A9 P3	A8 P3	A7 P3	R
T	A10 P2	A11 P2	$\overline{MKRD}$ P2	$\overline{CNTRD}$ P2													$\overline{CNTRD}$ P3	$\overline{MKRD}$ P3	A11 P3	A10 P3	T
U	VSS	A12 P2	A13 P2	$\overline{OE}$ P2	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	$\overline{OE}$ P3	A13 P3	A12 P3	VSS	U
V	A14 P2	A15[1] P2	CE1 P2	$\overline{CE}_0$ P2	R/$\overline{W}$ P2	I/O6 P2	VSS	VSS	I/O0 P2	$\overline{TRST}$	NC	I/O0 P3	VSS	VSS	I/O6 P3	R/$\overline{W}$ P3	$\overline{CE}_0$ P3	CE1 P3	A15[1] P3	A14 P3	V
W	VDD	$\overline{UB}$ P2	I/O7 P1	I/O5 P1	I/O3 P1	I/O1 P1	I/O8 P2	I/O4 P2	I/O2 P2	$\overline{MRST}$	CLKMBIST	I/O2 P3	I/O4 P3	I/O8 P3	I/O1 P4	I/O3 P4	I/O5 P4	I/O7 P4	$\overline{UB}$ P3	VDD	W
Y	$\overline{LB}$ P2	I/O8 P1	I/O6 P1	I/O4 P1	I/O2 P1	I/O0 P1	I/O7 P2	I/O5 P2	I/O3 P2	I/O1 P2	I/O1 P3	I/O3 P3	I/O5 P3	I/O7 P3	I/O0 P4	I/O2 P4	I/O4 P4	I/O6 P4	I/O8 P4	$\overline{LB}$ P3	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

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NOTES:
1. A15X is a NC for IDT70V5378.
2. This package code is used to reference the package diagram.
3. This text does not indicate orientation of the actual part marking.
4. Package body is approximately 27mm x 27mm x 2.33mm, with 1.27mm ball-pitch.
5. Central balls are for thermal dissipation only. They are connected to device VSS.

Pin Configuration[2]

70V5388/78BC
BC-256[3]

256-Pin BGA[4]
Top View

09/25/02

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	R/$\overline{W}$ P1	$\overline{OE}$ P1	$\overline{LB}$ P1	I/O16 P2	I/O13 P2	I/O9 P2	I/O14 P1	I/O10 P1	I/O9 P4	I/O12 P4	I/O16 P4	I/O11 P3	I/O15 P3	I/O17 P3	$\overline{UB}$ P4	CE1 P4	A
B	A15[1] P1	CE1 P1	$\overline{UB}$ P1	I/O17 P2	I/O14 P2	I/O10 P2	I/O15 P1	I/O11 P1	TDI	I/O13 P4	I/O17 P4	I/O12 P3	I/O16 P3	$\overline{LB}$ P4	R/$\overline{W}$ P4	$\overline{CE}_0$ P4	B
C	A14 P1	A13 P1	$\overline{CE}_0$ P1	I/O15 P2	I/O12 P2	I/O17 P1	I/O12 P1	I/O9 P1	TDO	I/O11 P4	I/O15 P4	I/O10 P3	I/O14 P3	$\overline{OE}$ P4	A15[1] P4	A14 P4	C
D	A10 P1	A12 P1	A11 P1	A9 P1	I/O11 P2	I/O16 P1	I/O13 P1	TMS	TCK	I/O10 P4	I/O14 P4	I/O9 P3	I/O13 P3	A11 P4	A12 P4	A13 P4	D
E	A7 P1	A8 P1	A6 P1	A5 P1	VDD	VDD	VDD	VDD	VDD	VDD	VDD	A6 P4	A7 P4	A8 P4	A10 P4	A9 P4	E
F	A3 P1	A4 P1	A2 P1	A1 P1	VDD	VDD	VSS	VSS	VSS	VDD	VDD	A1 P4	A2 P4	A3 P4	A5 P4	A4 P4	F
G	CLK P1	A0 P1	$\overline{CNTRD}$ P1	$\overline{CNTINC}$ P1	VDD	VSS	VSS	VSS	VSS	VSS	VSS	$\overline{CNTLD}$ P4	$\overline{CNTINC}$ P4	$\overline{CNTRD}$ P4	A0 P4	CLK P4	G
H	VSS	$\overline{CNTLD}$ P1	$\overline{CNTRST}$ P1	$\overline{CNTINT}$ P1	$\overline{INT}$ P1	$\overline{MKLD}$ P1	VSS	VSS	VSS	VSS	$\overline{CNTRST}$ P4	$\overline{MKRD}$ P4	$\overline{INT}$ P4	$\overline{CNTINT}$ P4	$\overline{MKLD}$ P4	VSS	H
J	CLK P2	$\overline{CNTRST}$ P2	$\overline{INT}$ P2	$\overline{CNTINT}$ P2	$\overline{MKRD}$ P1	VSS	VSS	VSS	VSS	VSS	VSS	$\overline{CNTRST}$ P3	$\overline{INT}$ P3	$\overline{CNTINT}$ P3	$\overline{MKLD}$ P3	CLK P3	J
K	$\overline{CNTRD}$ P2	$\overline{MKRD}$ P2	$\overline{CNTINC}$ P2	$\overline{CNTLD}$ P2	$\overline{MKLD}$ P2	VSS	VSS	VSS	VSS	VSS	VSS	$\overline{CNTLD}$ P3	$\overline{CNTINC}$ P3	$\overline{MKRD}$ P3	A0 P3	$\overline{CNTRD}$ P3	K
L	A3 P2	A4 P2	A2 P2	A1 P2	A0 P2	VDD	VDD	VSS	VSS	VSS	VDD	VDD	A1 P3	A3 P3	A4 P3	A2 P3	L
M	A8 P2	A9 P2	A7 P2	A6 P2	A5 P2	VDD	VDD	VDD	VDD	VDD	VDD	VDD	A5 P3	A7 P3	A8 P3	A6 P3	M
N	A11 P2	A12 P2	A10 P2	I/O5 P1	I/O1 P1	I/O6 P2	I/O2 P2	$\overline{TRST}$	CLKMBIST	I/O3 P3	I/O7 P3	I/O2 P4	A9 P3	A11 P3	A12 P3	A10 P3	N
P	A13 P2	A14 P2	R/$\overline{W}$ P2	I/O7 P1	I/O2 P1	I/O7 P2	I/O3 P2	$\overline{MRST}$	I/O0 P3	I/O4 P3	I/O8 P3	I/O3 P4	I/O6 P4	$\overline{CE}_0$ P3	A14 P3	A13 P3	P
R	A15[1] P2	CE1 P2	$\overline{UB}$ P2	I/O8 P1	I/O4 P1	I/O0 P1	I/O5 P2	I/O1 P2	I/O2 P3	I/O6 P3	I/O1 P4	I/O5 P4	I/O7 P4	$\overline{UB}$ P3	CE1 P3	A15[1] P3	R
T	$\overline{CE}_0$ P2	$\overline{OE}$ P2	$\overline{LB}$ P2	I/O6 P1	I/O3 P1	I/O8 P2	I/O4 P2	I/O0 P2	I/O1 P3	I/O5 P3	I/O0 P4	I/O4 P4	I/O8 P4	$\overline{LB}$ P3	$\overline{OE}$ P3	R/$\overline{W}$ P3	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

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NOTES:
1. A15X is a NC for IDT70V5378.
2. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
3. This package code is used to reference the package diagram.
4. This text does not indicate orientation of the actual part-marking.

Pin Definitions

Port 1	Port 2	Port 3	Port 4	Description
A_{0P1} - A_{15P1}(1)	A_{0P2} - A_{15P2}(1)	A_{0P3} - A_{15P3}(1)	A_{0P4} - A_{15P4}(1)	Address Inputs. In the $\overline{CNTRD}$ and $\overline{MKRD}$ operations, these pins serve as outputs for the internal address counter and the internal counter mask register respectively.
I/O_{0P1} - I/O_{17P1}	I/O_{0P2} - I/O_{17P2}	I/O_{0P3} - $I/0_{17P3}$	I/O_{0P4} - I/O_{17P4}	Data Bus Input/Output.
CLK_{P1}	CLK_{P2}	CLK_{P3}	CLK_{P4}	Clock Input. The maximum clock input rate is f_{MAX}. The clock signal can be free running or strobed depending on system requirements.
$\overline{MRST}$				Master Reset Input. $\overline{MRST}$ is an asycnchronous input, and affects all ports. It must be asserted LOW ($\overline{MRST}$ = V_{IL}) at initial power-up. Master Reset sets the internal value of all address counters to zero, and sets the counter mask registers for each port to 'unmasked'. It also resets the output flags for the mailboxes and the counter interrupts ($\overline{INT}$ = $\overline{CNTINT}$ = V_{IH}) and deselects all registered control signals.
$\overline{CE}_{0P1}$, CE_{1P1}	$\overline{CE}_{0P2}$, CE_{1P2}	$\overline{CE}_{0P3}$, CE_{1P3}	$\overline{CE}_{0P4}$, CE_{1P4}	Chip Enable Inputs. To activate any port, both signals must be asserted to their active states ($\overline{CE}_0$ = V_{IL}, CE_1 = V_{IH}). A given port is disabled if either chip enable is deasserted ($\overline{CE}_0$ = V_{IH} and/or CE_1 = V_{IL}).
$R/\overline{W}_{PI}$	$R/\overline{W}_{P2}$	$R/\overline{W}_{P3}$	$R/\overline{W}_{P4}$	Read/Write Enable Input. This signal is asserted LOW ($R/\overline{W}$ = V_{IL}) in order to write to the FourPort memory array, and it is asserted HIGH ($R/\overline{W}$ = V_{IH}) in order to read from the array.
$\overline{LB}_{P1}$	$\overline{LB}_{P2}$	$\overline{LB}_{P3}$	$\overline{LB}_{P4}$	Lower Byte Select Input (I/O_0 - I/O_8). Asserting this signal LOW ($\overline{LB}$ = V_{IL}) enables read/write operations to the lower byte. For read operations, this signal is used in conjunction with $\overline{OE}$ in order to drive output data on the lower byte of the data bus.
$\overline{UB}_{P1}$	$\overline{UB}_{P2}$	$\overline{UB}_{P3}$	$\overline{UB}_{P4}$	Upper Byte Select Input (I/O_9 - I/O_{17}). Asserting this signal LOW ($\overline{LB}$ = V_{IL}) enables read/write operations to the upper byte. For read operations, this signal is used in conjunction with $\overline{OE}$ in order to drive output data on the upper byte of the data bus.
$\overline{OE}_{P1}$	$\overline{OE}_{P2}$	$\overline{OE}_{P3}$	$\overline{OE}_{P4}$	Output Enable Input. Asserting this signal LOW ($\overline{OE}$ = V_{IL}) enables the device to drive data on the I/O pins during read operation. $\overline{OE}$ is an asychronous input.
$\overline{CNTLD}_{P1}$	$\overline{CNTLD}_{P2}$	$\overline{CNTLD}_{P3}$	$\overline{CNTLD}_{P4}$	Counter Load Input. Asserting this signal LOW ($\overline{CNTLD}$ = V_{IL}) loads the address on the address lines (A_0 - A_{15}(1)) into the internal address counter for that port.
$\overline{CNTINC}_{P1}$	$\overline{CNTINC}_{P2}$	$\overline{CNTINC}_{P3}$	$\overline{CNTINC}_{P4}$	Counter Increment Input. Asserting this signal LOW ($\overline{CNTINC}$ = V_{IL}) increments the internal address counter for that port on each rising edge of the clock signal. The counter will increment as defined by the counter mask register for that port (default mode is to advance one address on each clock cycle).
$\overline{CNTRD}_{P1}$	$\overline{CNTRD}_{P2}$	$\overline{CNTRD}_{P3}$	$\overline{CNTRD}_{P4}$	Counter Readback Input. When asserted LOW ($\overline{CNTRD}$ = V_{IL}) causes that port to output the value of its internal address counter on the address lines for that port. Counter readback is independent of the chip enables for that port. If the port is activated ($\overline{CE}_0$ = V_{IL} and CE_1 = V_{IH}), during the counter readback operation, then the data bus will output the data associated with that readback address in the FourPort memory array (assuming that the byte enables and output enables are also asserted). Truth Table III indicates the required states for all other counter controls during this operation. The specific operation and timing of this funcion is described in detail in the text.
$\overline{CNTRST}_{P1}$	$\overline{CNTRST}_{P2}$	$\overline{CNTRST}_{P3}$	$\overline{CNTRST}_{P4}$	Counter Reset Input. Asserting this signal LOW ($\overline{CNTRST}$ = V_{IL}) resets the address counter for that port to zero.
$\overline{CNTINT}_{P1}$	$\overline{CNTINT}_{P2}$	$\overline{CNTINT}_{P3}$	$\overline{CNTINT}_{P4}$	Counter Interrupt Flag Output. This signal is asserted LOW ($\overline{CNTINT}$ = V_{IL}) when the internal address counter for that port 'wraps around' from max address [(the counter will increment as defined by the counter mask register for that port (default mode is to advance one address on each clock cycle)] to address min. as the result of counter increment ($\overline{CNTINT}$ = V_{IL}). The signal goes LOW for one clock cycle, then automatically resets.

5649 tbl 01

Pin Definitions (con't.)

Port 1	Port 2	Port 3	Port 4	Description
$\overline{MKLD}_{P1}$	$\overline{MKLD}_{P2}$	$\overline{MKLD}_{P3}$	$\overline{MKLD}_{P4}$	Counter Mask Register Load Input. Asserting this signal LOW ($\overline{MKLD}$ = V_{IL}) loads the address on the address lines (A_0 - A_{15}[1]) into the counter mask register for that port. Counter mask register operations are described in detail in the text.
$\overline{MKRD}_{P1}$	$\overline{MKRD}_{P2}$	$\overline{MKRD}_{P3}$	$\overline{MKRD}_{P4}$	Counter Mask Register Readback Input. Asserting this signal LOW ($\overline{MKRD}$ = V_{IL}) causes that port to output the value of its internal counter mask register on the address lines (A_0 - A_{15}[1]) for that port. Address Counter and Counter-Mask Operational Table indicates the required states for all other counter controls during this operation. Counter mask register readback is independent of the chip enables for that port. If the port is activated ($\overline{CE}_0$ = V_{IL} and CE_1 = V_{IH}) during the counter mask register readback operation, then the data bus will output the data associated with that address in the FourPort memory array (assuming that the byte enables and output enables are also asserted). The specific operation and timing of this function is described in detail in the text.
$\overline{INT}_{P1}$	$\overline{INT}_{P2}$	$\overline{INT}_{P3}$	$\overline{INT}_{P4}$	Interrupt Flag Output. The FourPort is equipped with mailbox functions: each port has a specific address wthin the memory array which, when written by any of the other ports, will generate an interrupt flag to that port. The port clears its interrupt by reading that address. The memory location is a valid address for data storage: a full 18-bit word can be stored for recall by the target port or any other port. The mailbox functions and associated interrupts are described in detail in the text.
TMS				JTAG Input: Test Mode Select
$\overline{TRST}$				JTAG Input: Test Mode Reset (Intialize TAP Controller and reset the MBIST Controller)
TCK				JTAG Input: Test Clock
TDI				JTAG Input: Test Data Input (serial)
TDO				JTAG Output: Test Data Output (serial)
CLKMBIST				MBIST Input: MBIST Clock
GND				Thermal Grounds (should be treated like V_{SS})
V_{DD}				Core Power Supply (3.3V)
V_{SS}				Electrical Grounds (0V)

5649 tbl 02

NOTE:
1. A_{15X} is a NC for IDT70V5378.

Truth Table I—Read/Write and Enable Control(1,2,3)

$\overline{OE}$	CLK	$\overline{CE}_0$	CE_1	$\overline{UB}$	$\overline{LB}$	R/$\overline{W}$	Upper Byte I/O_{9-17}	Lower Byte I/O_{0-8}	MODE
X	↑	H	X	X	X	X	High-Z	High-Z	Deselected–Power Down
X	↑	X	L	X	X	X	High-Z	High-Z	Deselected–Power Down
X	↑	L	H	H	H	X	High-Z	High-Z	All Bytes Deselected
X	↑	L	H	H	L	L	High-Z	D_{IN}	Write to Lower Byte Only
X	↑	L	H	L	H	L	D_{IN}	High-Z	Write to Upper Byte Only
X	↑	L	H	L	L	L	D_{IN}	D_{IN}	Write to Both Bytes
L	↑	L	H	H	L	H	High-Z	D_{OUT}	Read Lower Byte Only
L	↑	L	H	L	H	H	D_{OUT}	High-Z	Read Upper Byte Only
L	↑	L	H	L	L	H	D_{OUT}	D_{OUT}	Read Both Bytes
H	↑	X	X	X	X	X	High-Z	High-Z	Outputs Disabled

5649 tbl 03

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. $\overline{CNTLD}$, $\overline{CNTINC}$, $\overline{CNTRST}$ = V_{IH}.
3. $\overline{OE}$ is an asynchronous input signal.

Truth Table II—Address Counter & Mask Control(1,2)

External Address	Previous Internal Address	Internal Address Used	CLK	$\overline{CNTLD}$	$\overline{CNTINC}$	$\overline{CNTRST}$	$\overline{MKLD}$	I/O	MODE
X	X	0	↑	X	X	L(3)	X	$D_{I/O}(0)$	Counter Reset to Address 0
An	Ap	Ap	↑	X	X	H	L	$D_{I/O}(p)$	Counter disabled (Ap reused)
An	X	An	↑	L(3)	X	H	H	$D_{I/O}$ (n)	External Address Used
An	Ap	Ap	↑	H	H	H	H	$D_{I/O}(p)$	External Address Blocked—Counter disabled (Ap reused)
X	Ap	Ap + 1(5)	↑	H	L(4)	H	H	$D_{I/O}(p+1)$(6)	Counter Enabled—Internal Address generation

5649 tbl 04

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. Read and write operations are controlled by the appropriate setting of R/$\overline{W}$, $\overline{CE}_0$, CE_1, $\overline{LB}$, $\overline{UB}$ and $\overline{OE}$.
3. $\overline{CNTLD}$ and $\overline{CNTRST}$ are independent of all other memory control signals including $\overline{CE}_0$, CE_1 and $\overline{LB}$, $\overline{UB}$.
4. The address counter advances if $\overline{CNTINC}$ = V_{IL} on the rising edge of CLK, regardless of all other memory control signals including $\overline{CE}_0$, CE_1, $\overline{LB}$, $\overline{UB}$.
5. The counter will increment as defined by the counter mask register for that port (default mode is to advance one address on each clock cycle).

Address Counter and Counter-Mask Control Operational Table (Any Port)(1,2)

CLK	$\overline{MRST}$	$\overline{CNTRST}$	$\overline{MKLD}$	$\overline{CNTLD}$	$\overline{CNTINC}$	$\overline{CNTRD}$	$\overline{MKRD}$	Mode	Operation
X	L	X	X	X	X	X	X	Master-Reset	Counter/Address Register Reset and Mask Register Set (resets chip as per reset state definition)
↑	H	L	X	X	X	X	X	Reset	Counter/Address Register Reset
↑	H	H	L	X	X	X	X	Load	Load of Address Lines into Mask Register
↑	H	H	H	L	X	X	X	Load	Load of Address Lines into Counter/Address Register
↑	H	H	H	H	L	X	X	Increment	Counter Increment
↑	H	X	X	X	X	L	X	Read-back	Readback Counter on Address Lines
↑	H	X	X	X	X	H	L	Read-back	Readback Mask Register on Address Lines
↑	H	H	H(3)	H	H	X	X	Hold	Counter Hold

5649 tbl 05

NOTES:
1. "X" = "don't care", "H" = V_{IH}, "L" = V_{IL}.
2. Counter operation and mask register operation is independent of Chip Enable.
3. $\overline{MKLD}$ = V_{IL} will also hold the counter. Please refer to Truth Table II.

Recommended Operating Temperature and Supply Voltage(1)

Grade	Ambient Temperature	GND	V_{DD}
Commercial	0°C to +70°C	0V	3.3V ± 150mV
Industrial	-40°C to +85°C	0V	3.3V ± 150mV

5649 tbl 06

NOTES:
1. This is the parameter TA. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.15	3.3	3.45	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage (Address, Control & I/O Inputs)	2.0	—	V_{DD} + 150mV(2)	V
V_{IL}	Input Low Voltage	-0.3(1)	—	0.8	V

5649 tbl 07

NOTES:
1. Undershoot of $V_{IL} \geq$ -1.5V for pulse width less than 10ns is allowed.
2. V_{TERM} must not exceed V_{DD} + 150mV.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T_{BIAS}(3)	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{JN}	Junction Temperature	+150	°C
I_{OUT}	DC Output Current	50	mA

5623 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{DD} + 150mV for more than 25% of the cycle time or 4ns maximum, and is limited to $\leq$ 20mA for the period of $V_{TERM} \geq V_{DD}$ + 150mV.
3. Ambient Temperature under DC Bias. No AC conditions. Chip Deselected.

Capacitance(1)

(T_A = +25°C, F = 1.0MHz)

Symbol	Parameter	Conditions(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	8	pF
C_{OUT}(3)	Output Capacitance	V_{OUT} = 3dV	10.5	pF

5649 tbl 09

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. C_{OUT} also references $C_{I/O}$.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 150mV)

Symbol	Parameter	Test Conditions	70V5388/78S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current(1)	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	10	µA
$\|I_{LI}\|$	JTAG Input Leakage Current(1,2)	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	30	µA
$\|I_{LO}\|$	Output Leakage Current(1)	V_{OUT} = 0V to V_{DD}, Outputs in tri-state mode	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = +4mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{DD} = Min.	2.4	—	V

5649 tbl 10

NOTE:
1. At $V_{DD} \leq$ 2.0V leakages are undefined.
2. Applicable only for TMS, TDI and $\overline{TRST}$ inputs.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[3] (V_{DD} = 3.3V ± 150mV)

Symbol	Parameter	Test Condition	Version		70V5388/78S200 Com'l Only		70V5388/78S166 Com'l & Ind		70V5388/78S133 Com'l & Ind		70V5388/78S100 Com'l & Ind		Unit
					Typ.[4]	Max.	Typ.[4]	Max.	Typ.[4]	Max.	Typ.[4]	Max.	
I_{DD}	Dynamic Operating Current (All Ports Active)	$\overline{CE}_1 = \overline{CE}_2 = \overline{CE}_3 = \overline{CE}_4$[5] = V_{IL}, Outputs Disabled, f = f_{MAX}[1]	COM'L	S	405	470	340	395	275	320	205	240	mA
			IND	S	—	—	340	400	275	325	205	245	
I_{SB1}	Standby Current (All Ports - TTL Level Inputs)	$\overline{CE}_1 = \overline{CE}_2 = \overline{CE}_3 = \overline{CE}_4$[5] = V_{IH}, Outputs Disabled, f = f_{MAX}[1]	COM'L	S	195	225	160	190	130	155	100	120	mA
			IND	S	—	—	160	195	130	160	100	125	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_A$ = V_{IL} and $\overline{CE}_B = \overline{CE}_C = \overline{CE}_D$ = V_{IH}[5] Active Port, Outputs Disabled, f=f_{MAX}[1]	COM'L	S	250	290	210	240	170	195	130	150	mA
			IND	S	—	—	210	245	170	200	130	155	
I_{SB3}	Full Standby Current (All Ports - CMOS Level Inputs)	All Ports Outputs Disabled, $\overline{CE}$[5] ≥ V_{DD} - 0.2V, V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V, f = 0[2]	COM'L	S	1.5	15	1.5	15	1.5	15	1.5	15	mA
			IND	S	—	—	1.5	15	1.5	15	1.5	15	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_A$ ≤ 0.2V and $\overline{CE}_B = \overline{CE}_C = \overline{CE}_D$ ≥ V_{DD} - 0.2V[5] V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V Active Port, Outputs Disabled, f = f_{MAX}[1]	COM'L	S	250	290	210	240	170	195	130	150	mA
			IND	S	—	—	210	245	170	200	130	155	

5649 tbl 11

NOTES:
1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t_{CYC}, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Parameters are identical for all ports.
4. V_{DD} = 3.3V, T_A = 25°C for Typ, and are not production tested. $I_{DD\,DC}$(f=0) = 120mA (Typ).
5. $\overline{CE}_X$ = V_{IL} means $\overline{CE}_{0X}$ = V_{IL} and CE_{1X} = V_{IH}
   $\overline{CE}_X$ = V_{IH} means $\overline{CE}_{0X}$ = V_{IH} or CE_{1X} = V_{IL}
   $\overline{CE}_X$ ≤ 0.2V means $\overline{CE}_{0X}$ ≤ 0.2V and CE_{1X} ≥ V_{DD} - 0.2V
   $\overline{CE}_X$ ≥ V_{DD} - 0.2V means $\overline{CE}_{0X}$ ≥ V_{DD} - 0.2V or CE_{1X} - 0.2V
   "X" represents indicator for appropriate port.

AC Test Conditions (V_{DDQ} - 3.3V)

Input Pulse Levels (Address & Controls)	GND to 3.0V
Input Pulse Levels (I/Os)	GND to 3.0V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figure 1

5649 tbl 12

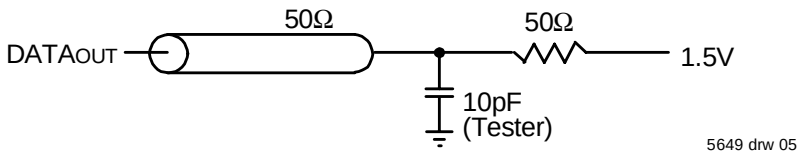


Figure 1. AC Output Test Load
***(For t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})**

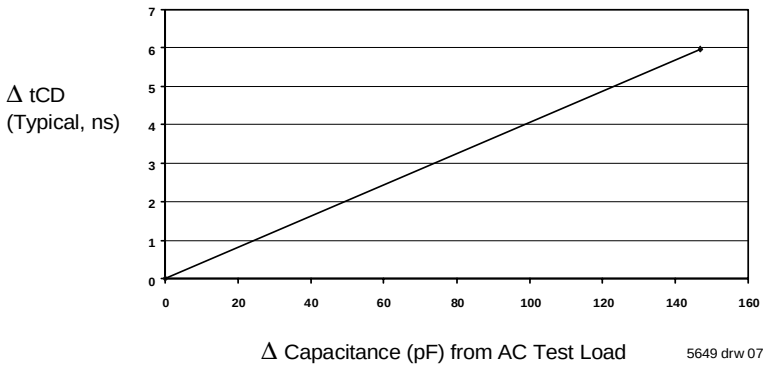


Figure 2. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing) (V_{DD} = 3.3V ± 150mV, T_A = 0°C to +70°C)

		70V5388/78S200 Com'l Only		70V5388/78S166 Com'l & Ind		70V5388/78S133 Com'l & Ind		70V5388/78S100 Com'l & Ind		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
f_{MAX2}	Maximum Frequency	—	200	—	166	—	133	—	100	MHz
t_{CYC2}	Clock Cycle Time	5	—	6	—	7.5	—	10	—	ns
t_{CH2}	Clock HIGH Time	2.0	—	2.1	—	2.6	—	4	—	ns
t_{CL2}	Clock LOW Time	2.0	—	2.1	—	2.6	—	4	—	ns
t_{SA}	Address Setup Time	1.5	—	1.7	—	1.8	—	2	—	ns
t_{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.7	—	ns
t_{SC}	Chip Enable Setup Time	1.5	—	1.7	—	1.8	—	2	—	ns
t_{HC}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	0.7	—	ns
t_{SW}	R/W Setup Time	1.5	—	1.7	—	1.8	—	2	—	ns
t_{HW}	R/W Hold Time	0.5	—	0.5	—	0.5	—	0.7	—	ns
t_{SD}	Input Data Setup Time	1.5	—	1.7	—	1.8	—	2	—	ns
t_{HD}	Input Data Hold Time	0.5	—	0.5	—	0.5	—	0.7	—	ns
t_{SB}	Byte Setup Time	1.5	—	1.7	—	1.8	—	2	—	ns
t_{HB}	Byte Hold Time	0.5	—	0.5	—	0.5	—	0.7	—	ns
t_{SCLD}	$\overline{CNTLD}$ Setup Time	1.5	—	1.7	—	1.8	—	2	—	ns
t_{HCLD}	$\overline{CNTLD}$ Hold Time	0.5	—	0.5	—	0.5	—	0.7	—	ns
t_{SCINC}	$\overline{CNTINC}$ Setup Time	1.5	—	1.7	—	1.8	—	2	—	ns
t_{HCINC}	$\overline{CNTINC}$ Hold Time	0.5	—	0.5	—	0.5	—	0.7	—	ns
t_{SCRST}	$\overline{CNTRST}$ Setup Time	1.5	—	1.7	—	1.8	—	2	—	ns
t_{HCRST}	$\overline{CNTRST}$ Hold Time	0.5	—	0.5	—	0.5	—	0.7	—	ns
t_{SCRD}	$\overline{CNTRD}$ Setup Time	1.5	—	1.7	—	1.8	—	2	—	ns
t_{HCRD}	$\overline{CNTRD}$ Hold Time	0.5	—	0.5	—	0.5	—	0.7	—	ns
t_{SMLD}	$\overline{MKLD}$ Setup Time	1.5	—	1.7	—	1.8	—	2	—	ns
t_{HMLD}	$\overline{MKLD}$ Hold Time	0.5	—	0.5	—	0.5	—	0.7	—	ns
t_{SMRD}	$\overline{MKRD}$ Setup Time	1.5	—	1.7	—	1.8	—	2	—	ns
t_{HMRD}	$\overline{MKRD}$ Hold Time	0.5	—	0.5	—	0.5	—	0.7	—	ns
t_{OE}	Output Enable to Data Valid	—	4.0	—	4.0	—	4.2	—	5	ns
t_{OLZ} [1,5]	$\overline{OE}$ to LOW-Z	1	—	1	—	1	—	1	—	ns
t_{OHZ} [1,5]	$\overline{OE}$ to HIGH-Z	1	3.4	1	3.6	1	4.2	1	4.5	ns
t_{CD2}	Clock to Data Valid	—	3.0	—	3.2	—	3.4	—	3.6	ns
t_{CA2}	Clock to Counter Address Readback Valid	—	3.4	—	3.6	—	4.2	—	5	ns
t_{CM2}	Clock to Mask Register Readback Valid	—	3.4	—	3.6	—	4.2	—	5	ns
t_{DC}	Data Output Hold After Clock HIGH	1	—	1	—	1	—	1	—	ns
t_{CKHZ} [1,2,5]	Clock HIGH to Output HIGH-Z	1	3	1	3	1	3	1	3	ns
t_{CKLZ} [1,2,5]	Clock HIGH to Output LOW-Z	1	—	1	—	1	—	1	—	ns

5649 tbl 13a

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing) (V_{DD} = 3.3V ± 150mV, T_A = 0°C to +70°C)

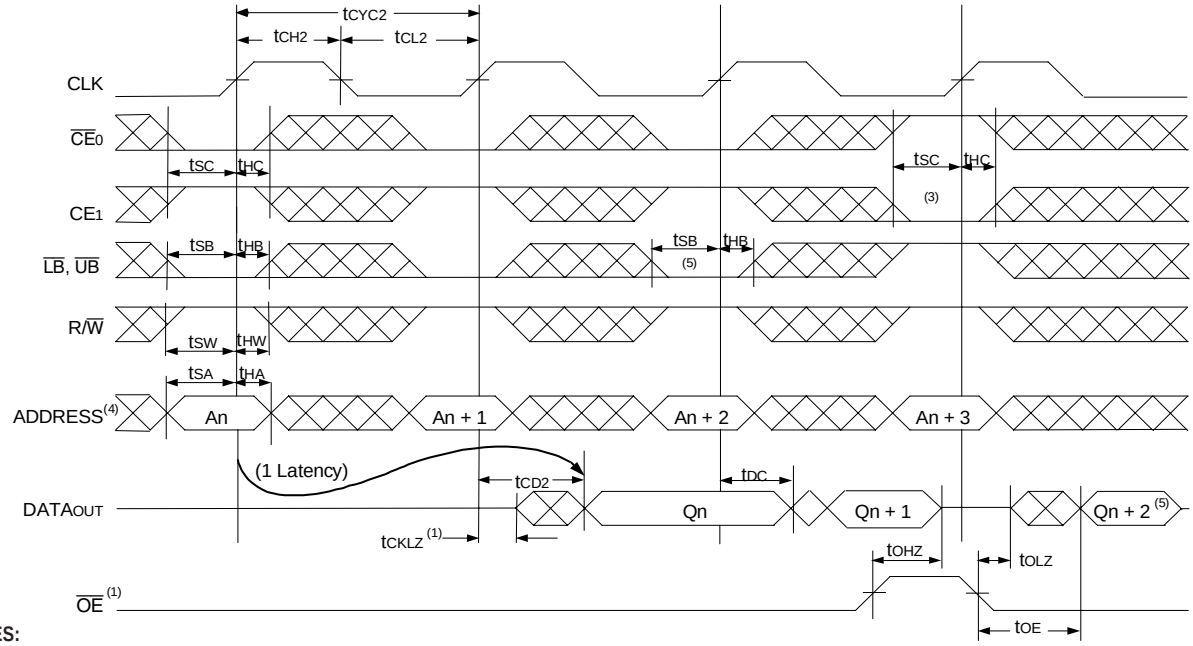
		70V5388/78S200 Com'l Only		70V5388/78S166 Com'l & Ind		70V5388/78S133 Com'l & Ind		70V5388/78S100 Com'l & Ind		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
Interrupt Timing										
t_{SINT}	Clock to $\overline{INT}$ Set Time	—	5	—	6	—	7.5	—	10	ns
t_{RINT}	Clock to $\overline{INT}$ Reset Time	—	5	—	6	—	7.5	—	10	ns
t_{SCINT}	Clock to $\overline{CNTINT}$ Set Time	—	5	—	6	—	7.5	—	10	ns
t_{RCINT}	Clock to $\overline{CNTINT}$ Reset Time	—	5	—	6	—	7.5	—	10	ns
Master Reset Timing										
t_{RS}	Master Reset Pulse Width	7.5	—	7.5	—	7.5	—	10	—	ns
t_{RSR}	Master Reset Recovery Time	7.5	—	7.5	—	7.5	—	10	—	ns
t_{ROF}	Master Reset to Output Flags Reset Time	—	6.5	—	6.5	—	6.5	—	8	ns
Port to Port Delays										
t_{CCS}[3]	Clock-to-Clock Setup Time	4.5	—	5	—	6.5	—	9	—	ns
JTAG Timing[4]										
f_{JTAG}	Maximum JTAG TAP Controller Frequency	—	10	—	10	—	10	—	10	MHz
t_{TCYC}	TCK Clock Cycle Time	100	—	100	—	100	—	100	—	ns
t_{TH}	TCK Clock High Time	40	—	40	—	40	—	40	—	ns
t_{TL}	TCK Clock Low Time	40	—	40	—	40	—	40	—	ns
t_{JS}	JTAG Setup	20	—	20	—	20	—	20	—	ns
t_{JH}	JTAG Hold	20	—	20	—	20	—	20	—	ns
t_{JCD}	TCK Clock Low to TDO Valid (JTAG Data Output)	—	20	—	20	—	20	—	20	ns
t_{JDC}	TCK Clock Low to TDO Invalid (JTAG Data Output Hold)	0	—	0	—	0	—	0	—	ns
f_{BIST}	Maximum CLKMBIST Frequency	—	200	—	166	—	133	—	100	MHz
t_{BH}	CLKMBIST High Time	2	—	2.5	—	3	—	4	—	ns
t_{BL}	CLKMBIST Low Time	2	—	2.5	—	3	—	4	—	ns
t_{JRST}	JTAG Reset	50	—	50	—	50	—	50	—	ns
t_{JRSR}	JTAG Reset Recovery	50	—	50	—	50	—	50	—	ns

5649 tbl 13b

NOTES:
1. Guaranteed by design (not production tested).
2. Valid for both data and address outputs.
3. This parameter defines the time necessary for one port to complete a write and have valid data available at that address for access from the other port(s). Attempting to read data before t_{CCS} has elapsed will result in the output of indeterminate data.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.
5. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 1).

Switching Waveforms

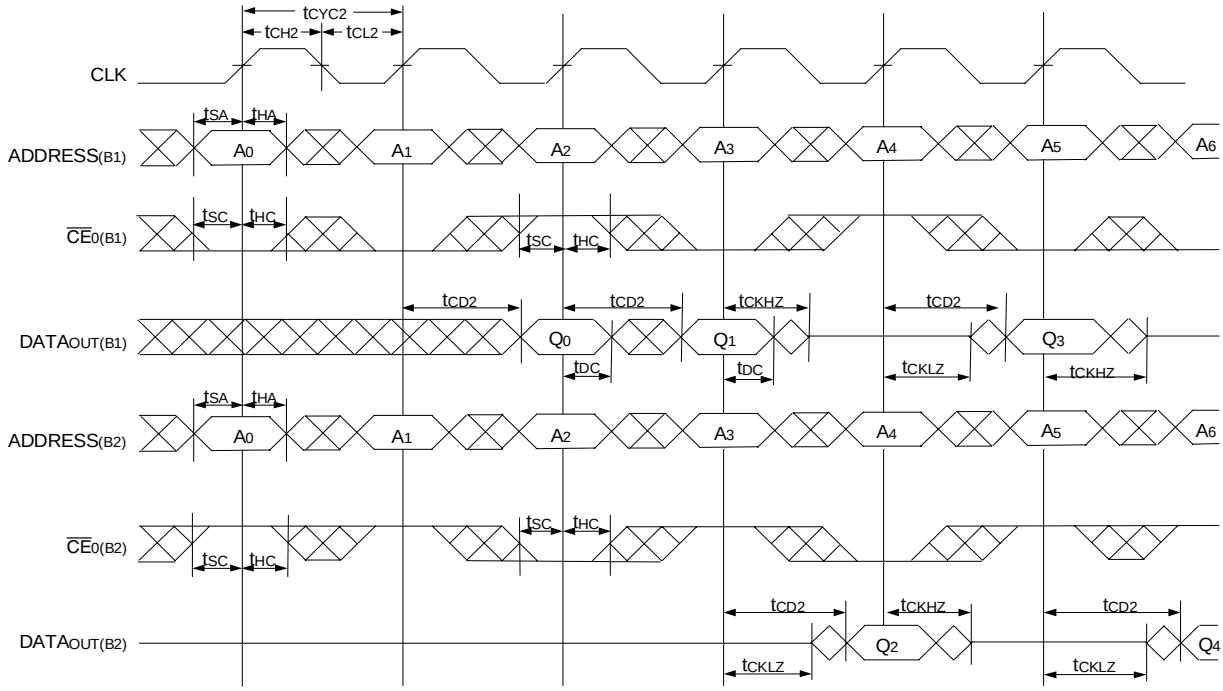
Timing Waveform of Read Cycle(2)



5649 drw 08

NOTES:
1. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
2. $\overline{CNTLD}$ = V_{IL}, $\overline{CNTINC}$ and $\overline{CNTRST}$ = V_{IH}.
3. The output is disabled (High-Impedance state) by $\overline{CE}_0$ = V_{IH}, CE_1 = V_{IL}, $\overline{LB}$, $\overline{UB}$ = V_{IH} following the next rising edge of the clock. Refer to Truth Table I.
4. Addresses do not have to be accessed sequentially since $\overline{CNTLD}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If $\overline{LB}$, $\overline{UB}$ was HIGH, then the appropriate Byte of $DATA_{OUT}$ for Qn + 2 would be disabled (High-Impedance state).

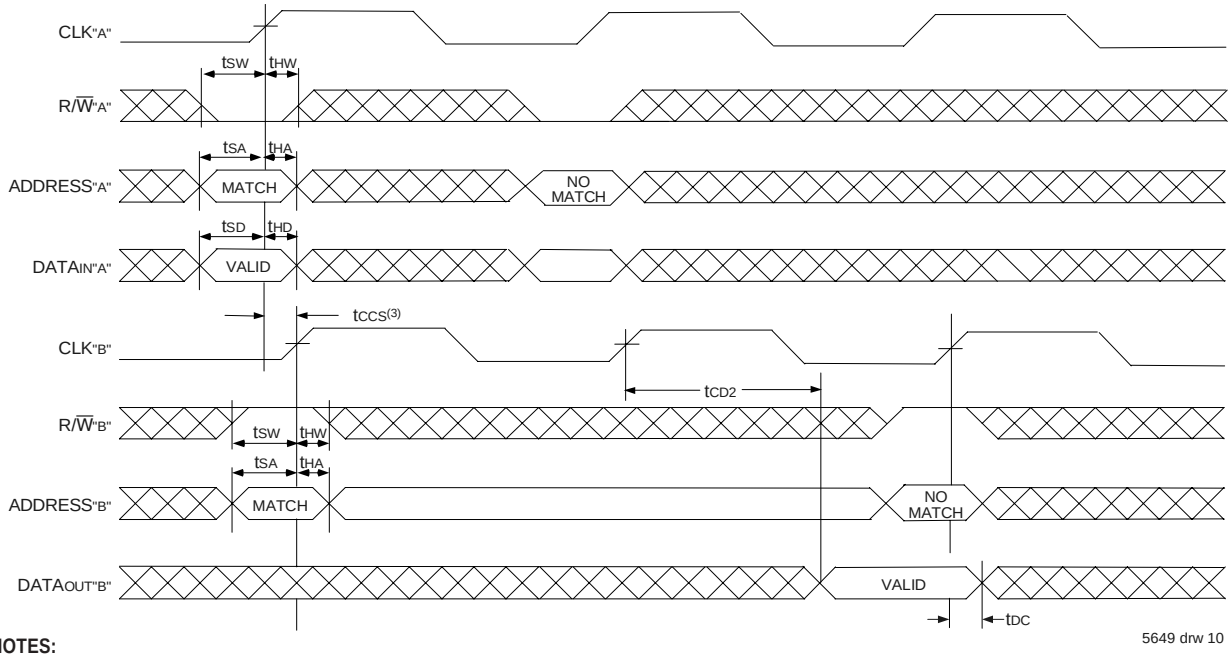
Timing Waveform of a Multi-Device Read(1,2)



5649 drw 09

NOTES:
1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70V5388/78 for this waveform, and are setup for depth expansion in this example. $ADDRESS_{(B1)}$ = $ADDRESS_{(B2)}$ in this situation.
2. $\overline{LB}$, $\overline{UB}$, $\overline{OE}$, and $\overline{CNTLD}$ = V_{IL}; $CE_{1(B1)}$, $CE_{1(B2)}$, R/$\overline{W}$, $\overline{CNTINC}$, and $\overline{CNTRST}$ = V_{IH}.

Timing Waveform of Port A Write to Port B Read(1,2,4)

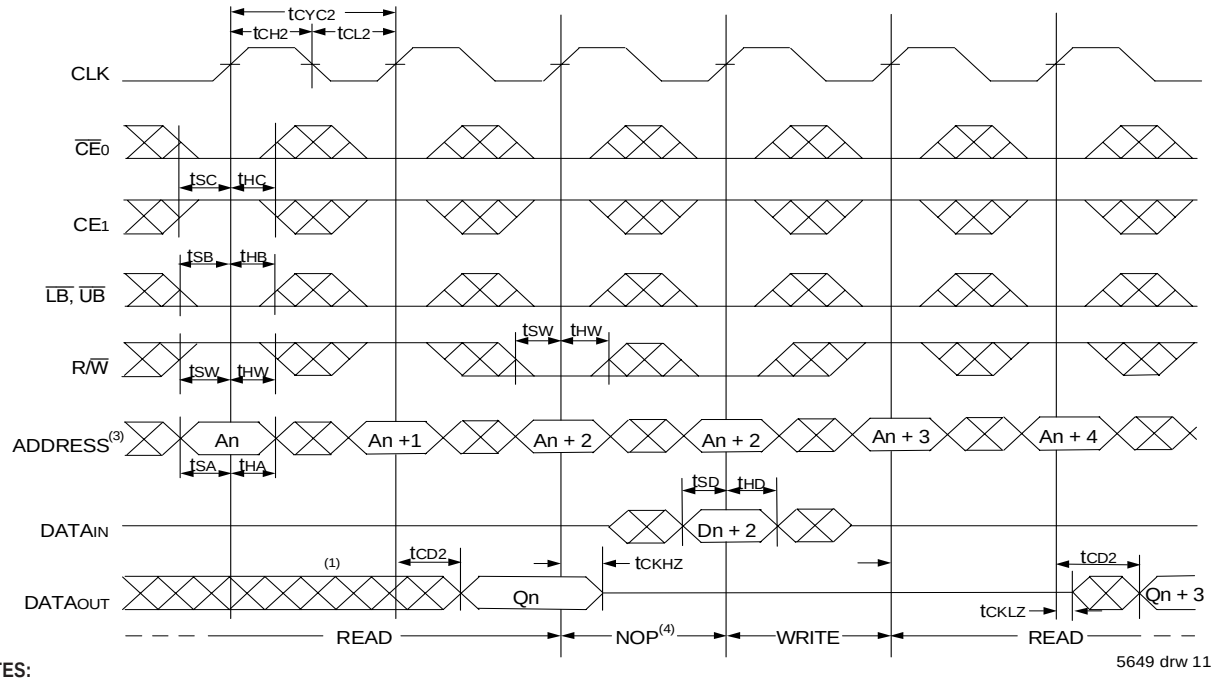


5649 drw 10

NOTES:

1. $\overline{CE_0}$, $\overline{LB}$, $\overline{UB}$, and $\overline{CNTLD}$ = V_{IL}; CE_1, $\overline{CNTINC}$, $\overline{CNTRST}$, $\overline{MRST}$, $\overline{MKLD}$, $\overline{MKRD}$ and $\overline{CNTRD}$ = V_{IH}.
2. $\overline{OE}$ = V_{IL} for Port "B", which is being read from. $\overline{OE}$ = V_{IH} for Port "A", which is being written to.
3. If $t_{CCS} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (ie, time from write to valid read on opposite port will be t_{CCS} + 2 t_{CYC2} + t_{CD2}). If t_{CCS} > minimum, then data from Port "B" read is available on first Port "B" clock cycle (ie, time from write to valid read on opposite port will be t_{CCS} + t_{CYC2} + t_{CD2}).
4. All timing is the same for all ports. Port "A" may be any port. Port "B" is any other port on the device.

Timing Waveform of Read-to-Write-to-Read ($\overline{OE}$ = V_{IL})(2)

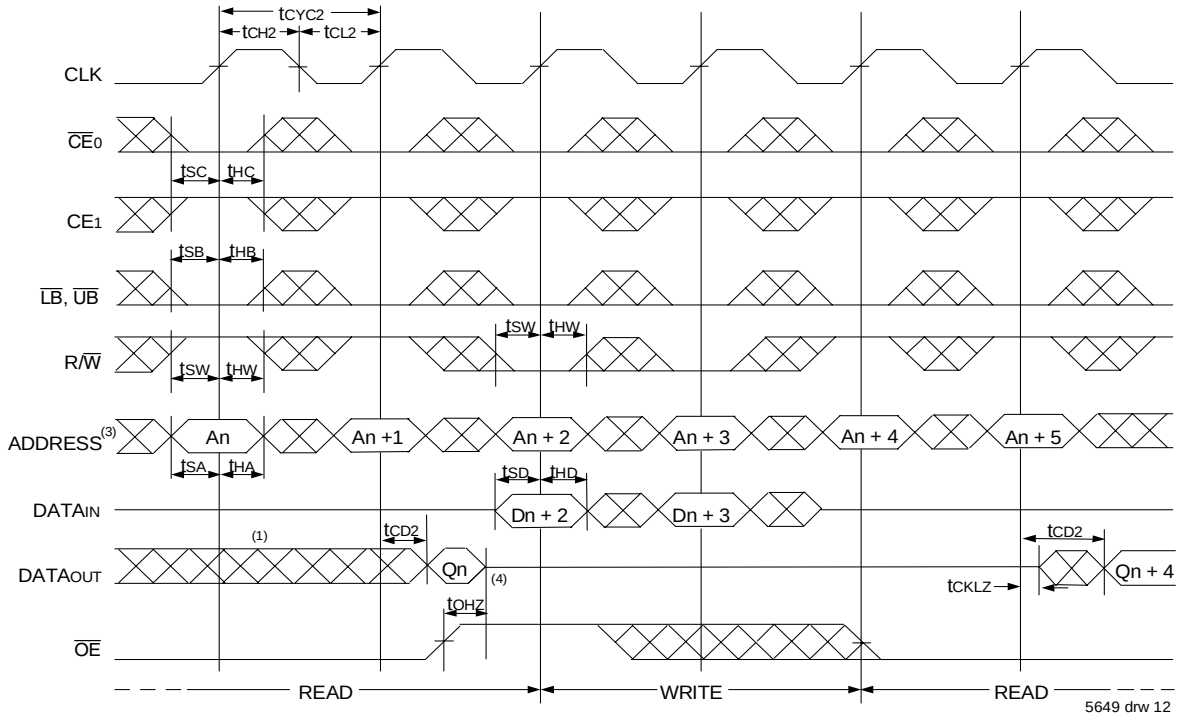


5649 drw 11

NOTES:

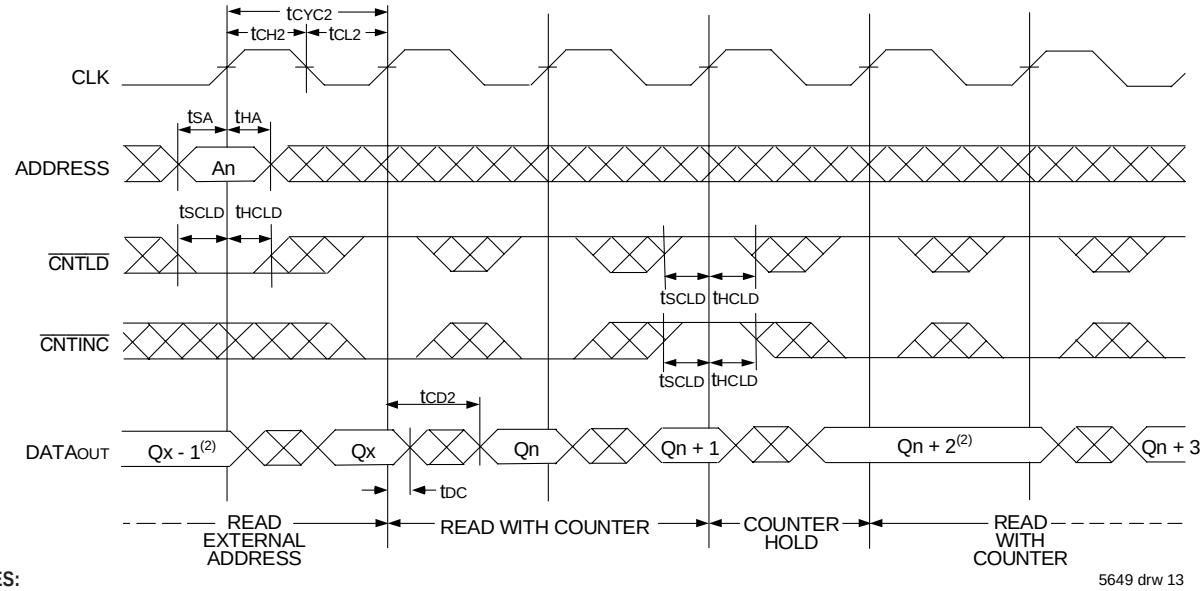
1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CNTLD}$ = V_{IL}; $\overline{CNTINC}$, and $\overline{CNTRST}$, $\overline{MRST}$, $\overline{MKLD}$, $\overline{MKRD}$ and $\overline{CNTRD}$ = V_{IH}. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{CNTLD}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Read-to-Write-to-Read ($\overline{OE}$ Controlled)(2)



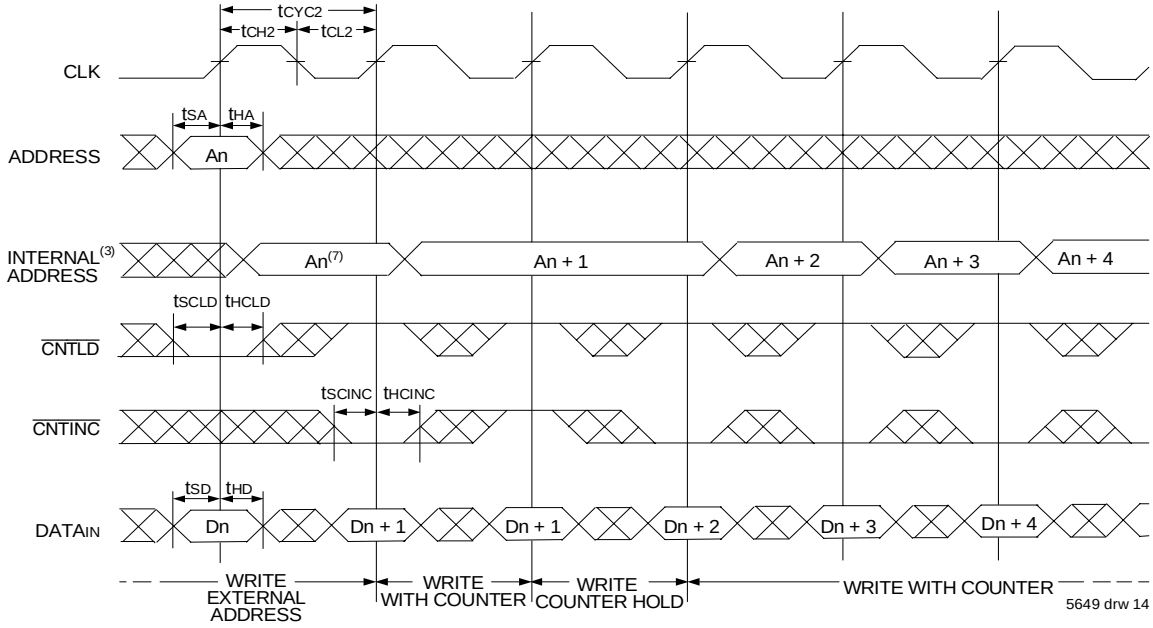
NOTES:
1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CNTLD}$ = V_{IL}; $\overline{CNTINC}$, $\overline{CNTRST}$, $\overline{MRST}$, $\overline{MKLD}$, $\overline{MKRD}$ and $\overline{CNTRD}$ = V_{IH}.
3. Addresses do not have to be accessed sequentially since $\overline{CNTLD}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

Timing Waveform of Read with Address Counter Advance(1)

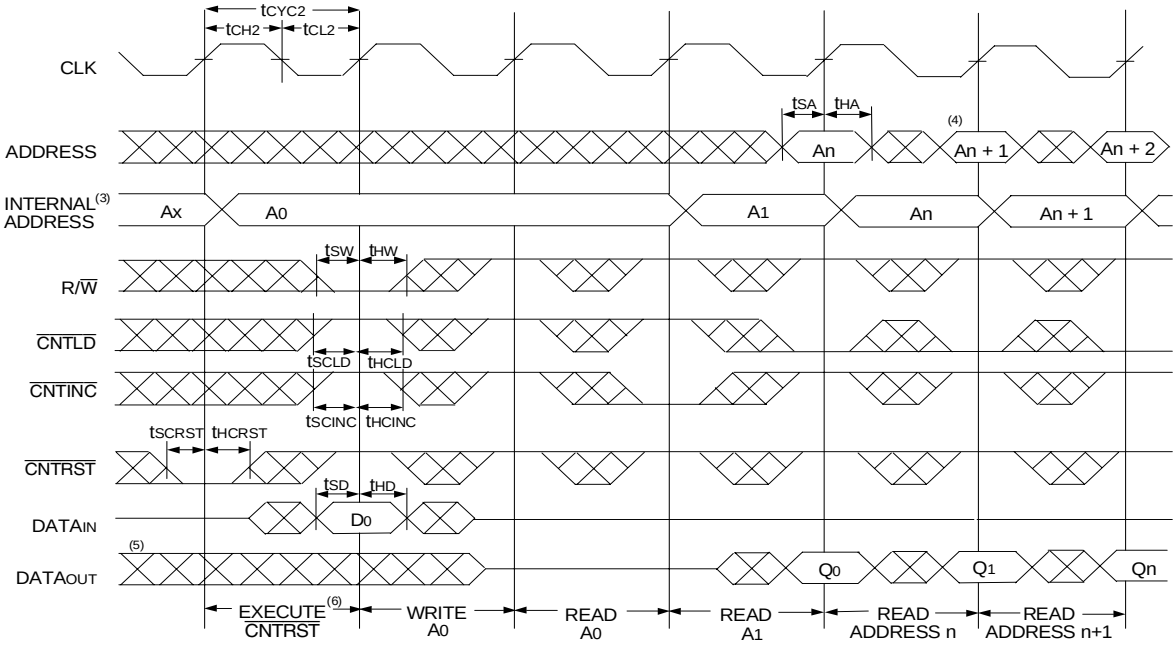


NOTES:
1. $\overline{CE_0}$, $\overline{LB}$ and $\overline{UB}$ = V_{IL}; CE_1, $\overline{CNTRST}$, $\overline{MRST}$, $\overline{MKLD}$, $\overline{MKRD}$ and $\overline{CNTRD}$ = V_{IH}.
2. If there is no address change via $\overline{CNTLD}$ = V_{IL} (loading a new address) or $\overline{CNTINC}$ = V_{IL} (advancing the address), i.e. $\overline{CNTLD}$ = V_{IH} and $\overline{CNTINC}$ = V_{IH}, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance(1)

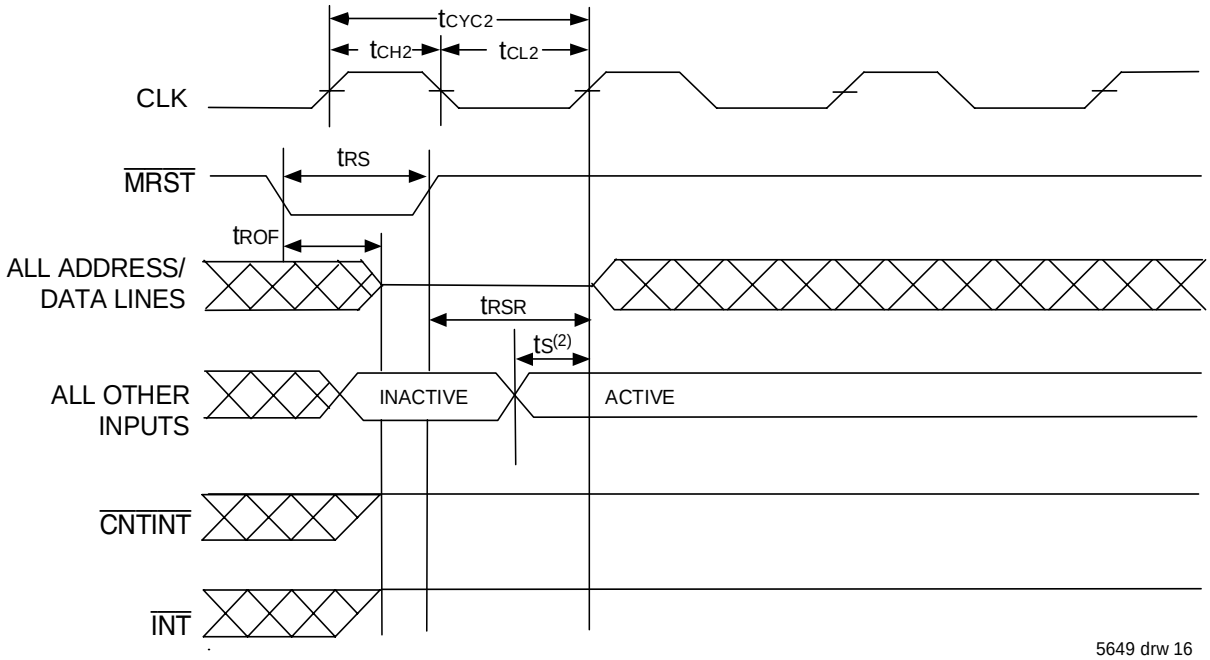


Timing Waveform of Counter Reset(2)



NOTES:
1. $\overline{CE_0}$, $\overline{LB}$, $\overline{UB}$, and R/$\overline{W}$ = V_{IL}; CE_1 and $\overline{CNTRST}$, $\overline{MRST}$, $\overline{MKLD}$, $\overline{MKRD}$, and $\overline{CNTRD}$ = V_{IH}.
2. $\overline{CE_0}$, $\overline{LB}$, $\overline{UB}$ = V_{IL}; CE_1 = V_{IH}.
3. The "Internal Address" is equal to the "External Address" when $\overline{CNTLD}$ = V_{IL} and equals the counter value when $\overline{CNTLD}$ = V_{IH}.
4. Addresses do not have to be accessed sequentially since $\overline{CNTLD}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during $\overline{CNTRST}$ operation. A READ or WRITE cycle may be coincidental with the counter $\overline{CNTRST}$ cycle: Address 0000h will be accessed. Extra cycles are shown here simply for clarification. For more information on $\overline{CNTRST}$ function refer to Truth Table II.
7. $\overline{CNTINC}$ = V_{IL} advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1'Address is written to during this cycle.

Timing Waveform of Master Reset(1)



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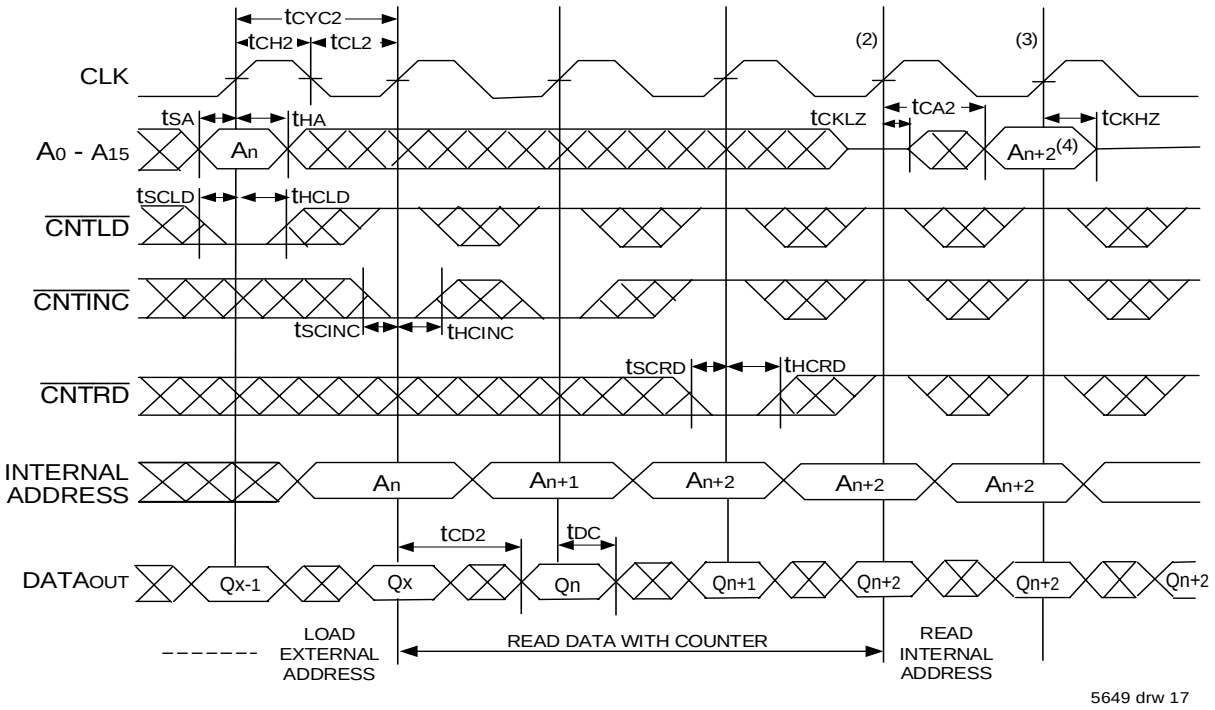
NOTES:

1. Master Reset will reset the device. For JTAG and MBIST reset please refer to the JTAG Timing specification.
2. ts is the set-up time required for all input control signals.

Timing Waveform of Load and Read Address Counter(1,2,3)



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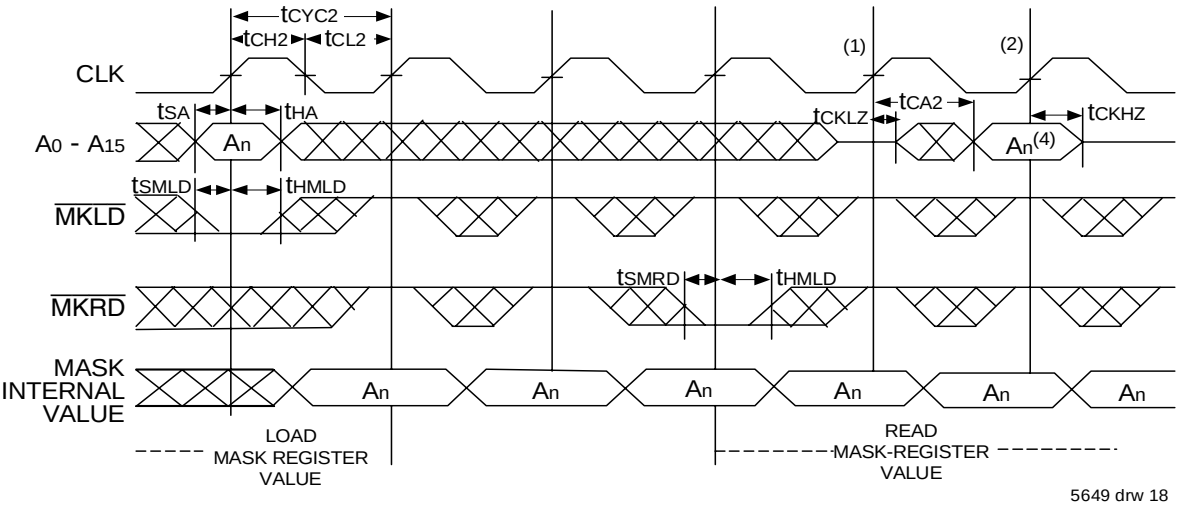
NOTES:
1. $\overline{CE_0}$, $\overline{OE}$, $\overline{LB}$ and $\overline{UB}$ = V_{IL}; CE_1, R/$\overline{W}$, $\overline{CNTRST}$, $\overline{MRST}$, $\overline{MKLD}$ and $\overline{MKRD}$ = V_{IH}.
2. Address in output mode. Host must not be driving address bus after time t_{CKLZ} in next clock cycle.
3. Address in input mode. Host can drive address bus after t_{CKHZ}.
4. This is the value of the address counter being read out on the address lines.

Timing Waveform of Load and Read Mask Register(1,2,3,4)



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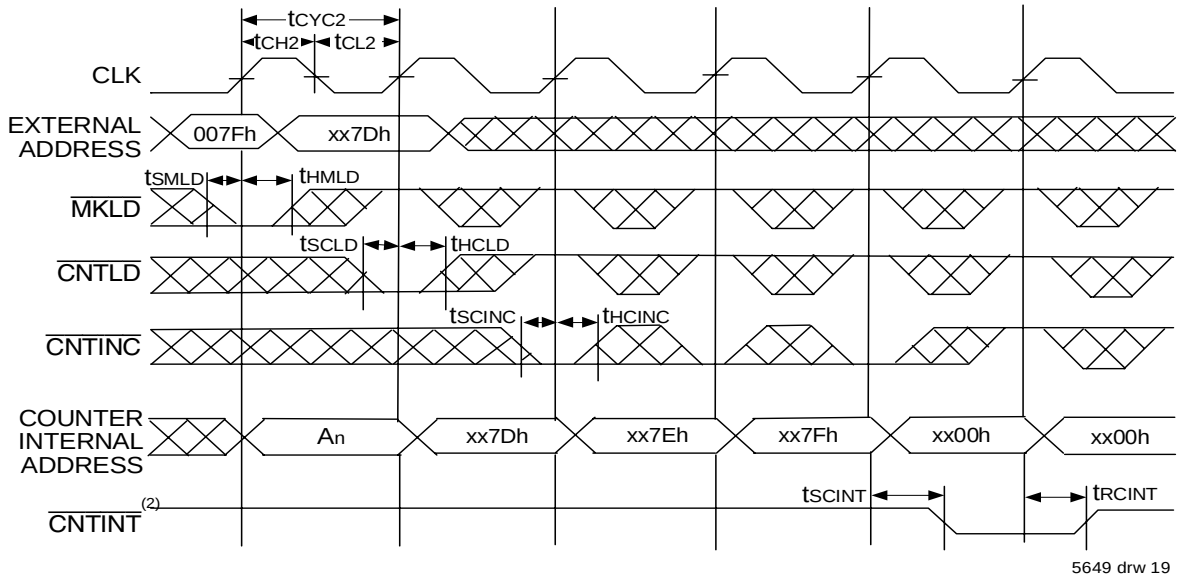
NOTES:
1. Address in output mode. Host must not be driving address bus after time t_{CKLZ} in next clock cycle.
2. Address in input mode. Host can drive address bus after t_{CKHZ}.
3. $\overline{CE_0}$, $\overline{OE}$, $\overline{LB}$ and $\overline{UB}$ = V_{IL}; CE_1, R/$\overline{W}$, $\overline{CNTRST}$, $\overline{MRST}$, $\overline{CNTLD}$, $\overline{CNTRD}$ and $\overline{CNTINC}$ = V_{IH}.
4. This is the value of the mask register being read out on the address lines.

Timing Waveform of Counter Interrupt(1,3)



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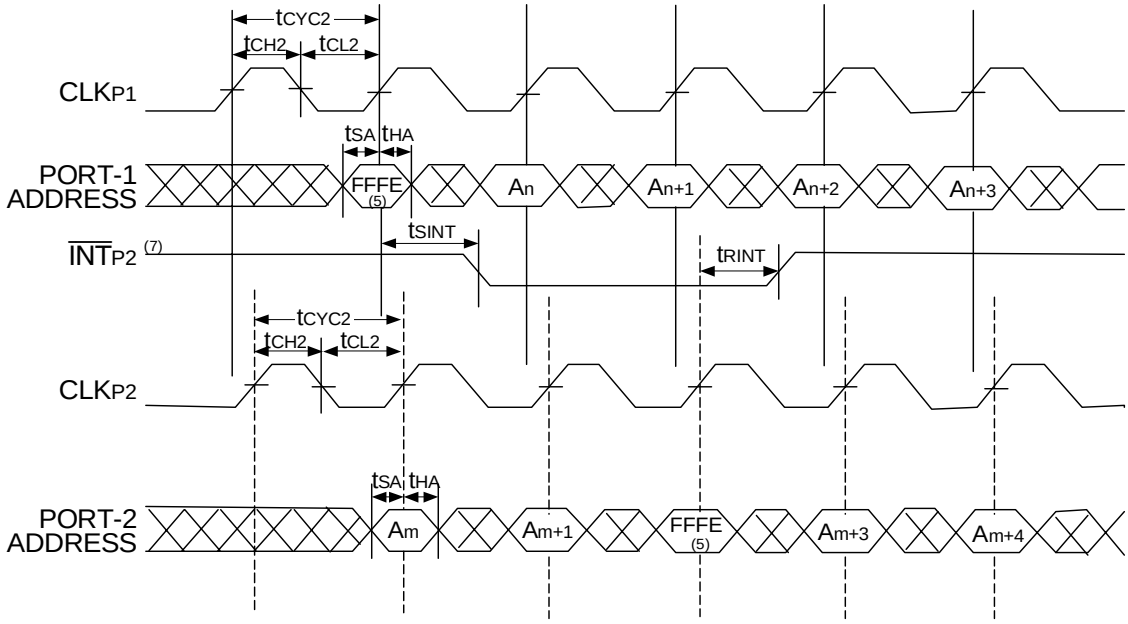
Timing Waveform of Mailbox Interrupt Timing(4,6)



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NOTES:

1. $\overline{CE_0}$, $\overline{OE}$, $\overline{LB}$ and $\overline{UB}$ = V_{IL}; CE_1, R/$\overline{W}$, $\overline{CNTRST}$, $\overline{MRST}$, $\overline{CNTRD}$ and $\overline{MKRD}$ = V_{IH}.
2. $\overline{CNTINT}$ is always driven.
3. $\overline{CNTINT}$ goes LOW as the counter address increments (via $\overline{CNTINC}$ = V_{IL}) past the maximum value programmed into the mask register and 'wraps around' to xx00h $\overline{CNTINT}$ stays LOW for one cycle, then resets. In this example, the mask register was programmed at xx7Fh ('x' indicates "Don't Care"). The Counter Mask Register operations are detailed on page 24.
4. $\overline{CNTRST}$, $\overline{MRST}$, $\overline{CNTRD}$ $\overline{CNTINC}$, $\overline{MKRD}$ and $\overline{MKLD}$ = V_{IH}. The mailbox interrupt circuitry relies on the state of the chip enables, the read/write signal, and the address location to generate or clear interrupts as appropriate - other control signals such as $\overline{OE}$, $\overline{LB}$ and $\overline{UB}$ are "Don't Care". Please refer to Truth Table III (page 22) for further explanation.
5. Address FFFEh is the mailbox location for Port 2 of IDT70V5388. Refer to Truth Table III for mailbox location of other Ports (page 22).
6. Port 1 is configured for a write operation (setting the interrupt) in this example, and Port 2 is configured for a read operation (clearing the interrupt). Ports 1 and 2 are used for an example: any port can set an interrupt to any other port per the operations in Truth Table III (page 22).
7. The interrupt flag is always set with respect to the rising edge of the writing port's clock, and cleared with respect to the rising edge of the reading port's clock.

Functional Description

The IDT70V5388/78 provides a true synchronous FourPort Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal and the duration of the R/$\overline{W}$ input signal. This is done in order to offer the fastest possible cycle times and highest data throughput. At 200 MHz, the device supports a cycle time of 5 ns, and provides a pipelined data output of 3.0 ns from clock edge to data valid. Four ports operating at 200 MHz, each with a bus width of 18 bits, results in a data throughput rate of nearly 14 Gbps.

As a true synchronous device, the IDT70V5388/78 provides the flexibility to clock each port independently: the ports may run at different frequencies and/or out of synchronization with each other. As a true FourPort device, the IDT70V5388/78 is capable of performing simultaneous reads from all ports on the same address location. Care should be taken when attempting to write and read address locations simultaneously: the timing diagrams depict the critical parameter t_{CCS}, which determines the amount of time needed to ensure that the write has successfully been completed and so valid data is available for output. Violation of t_{CCS} may produce indeterminate data for the read. Two or more ports attempting to write the same address location simultaneously will result in indeterminate data recorded at that address.

Each port is equipped with dual chip enables, $\overline{CE}_0$ and CE_1. A HIGH on $\overline{CE}_0$ or a LOW on CE_1 for one clock cycle on any port will power down the internal circuitry on that port in order to reduce static power consumption. The multiple chip enables also allow easier banking of multiple IDT70V5388/78s for depth expansion configurations. One cycle is required with chip enables reasserted to reactivate the outputs.

Depth and Width Expansion

The IDT70V5388/78 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V5388/78 can also be used in applications requiring expanded width, as indicated in Figure 3. Through combining the control signals, the devices can be grouped as necessary to accommodate applications requiring 36-bits or wider.

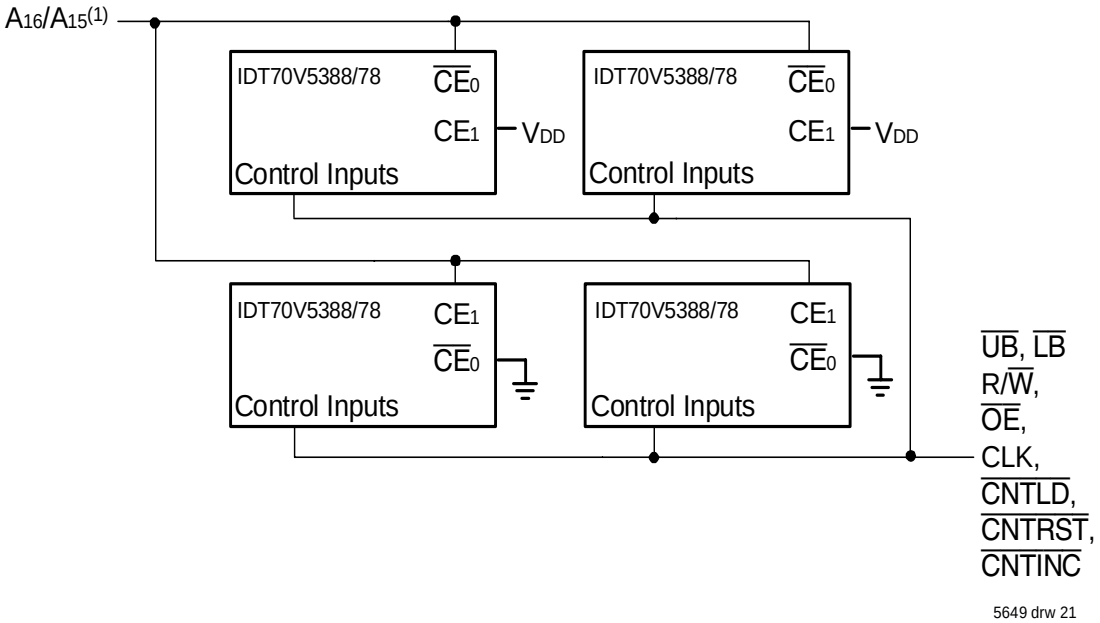

Figure 3. Depth and Width Expansion with IDT70V5388/78

NOTE:
1. A_{16} is for IDT70V5388, A_{15} is for IDT70V5378.

Mailbox Interrupts

The IDT70V5388/78 supports mailbox interrupts, facilitating communication among the devices attached to each port. If the user chooses the interrupt function, then each of the upper four address locations in the memory array are assigned as a mailbox for one of the ports: FFFFh (7FFFh for IDT70V5378) is the mailbox for Port 1, FFFEh (7FFEh for IDT70V5378) is the mailbox for Port 2, FFFDh (7FFDh for IDT70V5378) is the mailbox for Port 3, and FFFCh (7FFCh for IDT70V5378) is the mailbox for Port 4. Truth Table III details the operation of the mailbox interrupt functions.

A given port's interrupt is set (i.e., $\overline{INT}$ goes LOW) whenever any other port on the device writes to the given port's address. For example, Port 1's $\overline{INT}$ will go LOW if Port 2, Port 3, or Port 4 write to FFFFh (7FFFh for IDT70V5378). The $\overline{INT}$ will go LOW in relation to the clock on the writing port (see also the Mailbox Interrupt Timing waveform on page 20). If a port writes to its own mailbox, no interrupt is generated.

The mailbox location is a valid memory address: the user can store an 18-bit data word at that location for retrieval by the target port. In the event that two or more ports attempt to set an interrupt to the same port at the same time, the interrupt signal will go LOW, but the data actually stored at that location will be indeterminate. The actual interrupt is generated as a result of evaluating the state of the address pins, the chip enables, and the R/$\overline{W}$ pin: if the user wishes to set an interrupt to a specific port without changing the data stored in that port's mailbox, it is possible to do so by disabling the byte enables during that write cycle.

Once $\overline{INT}$ has gone LOW for a specific port, that port can reset the $\overline{INT}$ by reading its assigned mailbox. In the case of Port 1, it would clear its $\overline{INT}$ signal by reading FFFFh (7FFFh for IDT70V5378). As stated previously, the interrupt operation executes based on the state of the address pins, the chip enables, and the R/$\overline{W}$ pin: it is possible to clear the interrupt by asserting a read to the appropriate location while keeping the output enable ($\overline{OE}$) or the byte enables deasserted, and so avoid having to drive data on the I/O bus. The $\overline{INT}$ is reset, or goes HIGH again, in relation to the reading port's clock signal.

Master Reset

The IDT70V5388/78 is equipped with an asynchronous Master Reset input, which can be asserted independently of all clock inputs and will take effect per the Master Reset timing waveform on page 18. The Master Reset sets the internal value of all address counters to zero, and sets the counter mask register on each port to all ones (i.e., completely unmasked). It also resets all mailbox interrupts and counter interrupts to HIGH (i.e., non-asserted) and sets all registered control signals to a deselected state. A Master Reset operation must be performed after power-up, in order to initialize the various registers on the device to a known state. Master Reset will reset the device. For JTAG and MBIST reset please refer to the JTAG Section on page 25.

Truth Table III—Mailbox Interrupt Flag Operations

Port 1[1,2]				Port 2[1,2]				Port 3[1,2]				Port 4[1,2]				
R/$\overline{W}$	$\overline{CE}$	A_{15}-A_0[4]	$\overline{INT}$	R/$\overline{W}$	$\overline{CE}$	A_{15}-A_0[4]	$\overline{INT}$	R/$\overline{W}$	$\overline{CE}$	A_{15}-A_0[4]	$\overline{INT}$	R/$\overline{W}$	$\overline{CE}$	A_{15}-A_0[4]	$\overline{INT}$	Function
X	X	X	L	L	L	FFFF	X	L	L	FFFF	X	L	L	FFFF	X	Set Port 1 $\overline{INT}$ Flag[3]
H	L	FFFF	H	X	X	X	X	X	X	X	X	X	X	X	X	Reset Port 1 $\overline{INT}$ Flag
L	L	FFFE	X	X	X	X	L	L	L	FFFE	X	L	L	FFFE	X	Set Port 2 $\overline{INT}$ Flag[3]
X	X	X	X	H	L	FFFE	H	X	X	X	X	X	X	X	X	Reset Port 2 $\overline{INT}$ Flag
L	L	FFFD	X	L	L	FFFD	X	X	X	X	L	L	L	FFFD	X	Set Port 3 $\overline{INT}$ Flag[3]
X	X	X	X	X	X	X	X	H	L	FFFD	H	X	X	X	X	Reset Port 3 $\overline{INT}$ Flag
L	L	FFFC	X	L	L	FFFC	X	L	L	FFFC	X	X	X	X	L	Set Port 4 $\overline{INT}$ Flag[3]
X	X	X	X	X	X	X	X	X	X	X	X	H	L	FFFC	H	Reset Port 4 $\overline{INT}$ Flag

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NOTES:

1. The status of $\overline{OE}$ is a "Don't Care" for the interrupt logic circuitry. If it is desirable to reset the interrupt flag on a given port while keeping the I/O bus in a tri-state condition, then this can be accomplished by setting $\overline{OE}$ = V_{IH} while the read access is asserted to the appropriate address location.
2. The status of the $\overline{LB}$ and $\overline{UB}$ controls are "Don't Care" for the interrupt circuitry. If it is desirable to set the interrupt flag to a specific port without overwriting the data value already stored at the mailbox location, then this can be accomplished by setting $\overline{LB}$ = $\overline{UB}$ = V_{IH} during the write access for that specific mailbox. Similarly, if it desirable to reset the interrupt flag on a given port while keeping the I/O bus in a tri-state condition, then this can be accomplished by setting $\overline{LB}$ = $\overline{UB}$ = V_{IH} while the read access is asserted to the appropriate address location.
3. The interrupt to a specific port can be set by any one of the other three ports. The appropriate control states for the other three ports are depicted above. In the event that two or more ports attempt to set the same interrupt flag simultaneously via a valid data write, the data stored at the mailbox location will be indeterminate.
4. A_{15} is a NC for IDT70V5378, therefore Mailbox Interrupt Addresses are 7FFF, 7FFE, 7FFD and 7FFC. Address comparison will be for A_0 - A_{14}.

Address Counter Control Operations

Each port on the IDT70V5388/78 is equipped with an internal address counter, to ease the process of bursting data into or out of the device. Truth Table II depicts the specific operation of the counter functions, to include the order of priority among the signals. All counter controls are independent of chip enables. The device supports the ability to load a new address value on each access, or to load an address value on a given clock cycle via the $\overline{CNTLD}$ control and then allow the counter to increase that value by preset increments on each successive clock via the $\overline{CNTINC}$ control (see also the Counter Mask Operations section that follows). The counter can be suspended on any clock cycle by disabling the $\overline{CNTINC}$, and it can be reset to zero on any clock cycle by asserting the $\overline{CNTRST}$ control. $\overline{CNTRST}$ only affects the address value stored in the counter: it has no effect on the counter mask register.

When the counter reaches the maximum value in the array (i.e., address FFFFh for IDT70V5388 and address 7FFFh for IDT70V5378) or it reaches the highest value permitted by the Counter Mask Register, it then 'wraps around' to the beginning of the array. When Address Min is reached via counter increment (i.e., not as a result of an external address load), then the $\overline{CNTINT}$ signal for that port is driven low for one clock cycle, automatically resetting on the next cycle.

When the $\overline{CNTRD}$ control is asserted, the IDT70V5388/78 will output the current address stored in the internal counter for that port as noted in the Load and Read Address Counter timing waveform on page 19. The address will be output on the address lines. During this output, the data I/Os will be driven in accordance with the settings of the chip enables, byte enables, and the output enable on that port: the device does not automatically tri-state these pins during the address readback operation.

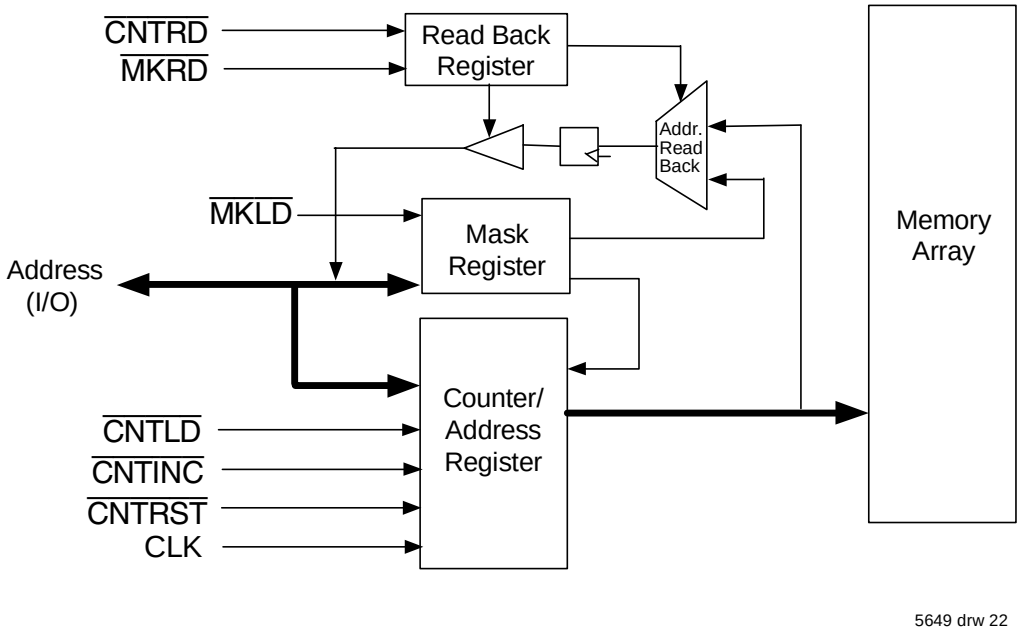

Figure 4. Logic Block Diagram for Read Back Operations

Counter-Mask Register

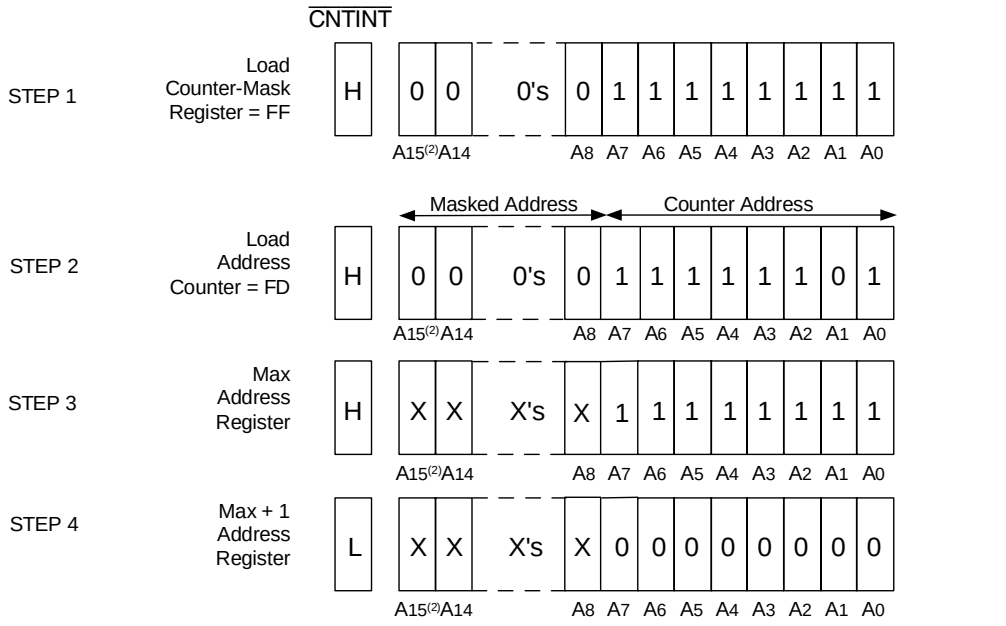

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Figure 5. Programmable Counter-Mask Register Operation (1)

NOTE:
1. The "X's" in this diagram represent the upper bits of the counter.
2. A_{15} is a NC for IDT70V5378.

The internal address counter on each port has an associated Counter Mask Register that allows for configuration of the internal address counter on that port. Truth Table III groups the operations of the address counter with those of the counter mask register, to include Master Reset and applicable readback operations.

Each bit in the mask register controls the corresponding bit in the internal address counter: writing a "1" to a bit in the mask register allows that bit to increment in response to $\overline{CNTINC}$, while writing a "0" to a bit masks it (i.e., locks it at whatever value is loaded via $\overline{CNTLD}$). The mask register is extremely flexible: every bit can be controlled independently of every other bit. The counter simply concatenates those bits that have not been masked, giving the user great selectivity in determining which portions of the memory array are available to a particular port for burst operations.

Figure 5 illustrates the operation of the Counter Mask Register in simply constraining a port to a selected portion of the array, specifically addresses 0000h to 00FFh. In step one, the mask register is loaded with 00FFh via $\overline{MKLD}$ (see also the Load and Read Mask Register timing waveform on page 19). In step two, a starting address of 00FD is asserted for the start point of a burst, and the $\overline{CNTINC}$ control is enabled. Step three indicates the address counter incrementing to 00FFh. In step four, the internal counter determines that all address values greater than 00FFh have been masked, and so it increments past this 'max' value to 0000h. As a result of reaching 0000h via the $\overline{CNTINC}$ operation, the $\overline{CNTINT}$ output for this port is automatically triggered – it will go low for one clock cycle and then reset.

The example depicted in Figure 5 is a very simple one: it is also possible to mask non-contiguous bits, such as loading 5555h in the mask register. As stated previously, the address counter simply concatenates all bits that have not been masked and continues to increment those bits in accordance with the $\overline{CNTINC}$ control: in this fashion, if the mask register is set at 5555h and a start address of 0007h is asserted via $\overline{CNTLD}$, the next value the counter will increment to in response to the $\overline{CNTINC}$ control is 0012h, then 0013h, then 0016h, etc.

Besides supporting precise control of which portions of the array are available to a particular port in burst operations, the independent control on the mask register bits also provides excellent flexibility in determining the value by which the counter will increment. For example, setting bit 0 of the mask register to "0" masks it from counter operation, effectively configuring that port to count by increments of two. This can be very useful in configuring two ports to work in combination, effectively creating a single 36-bit port. Thus, Port 1 can be configured to count by two starting on even addresses (the start point is asserted via $\overline{CNTLD}$), and Port 2 can be configured to count by two starting on odd addresses (again via $\overline{CNTLD}$). The two ports together will operate on 36-bit data words, storing half of each word in an even-numbered address, the other half in an odd-numbered address. Setting bits 1 and 0 of the mask register on a given port to "0" configures that port to count

in increments of four: masking bits 2, 1, and 0 configures that port to count in increments of eight, and so on. The ability to set the increments by which the counters will advance gives the user the ability to interleave memory operations among the ports, minimizing the concerns that a given address might be written by more than one port at any given point in time (an operation that would have indeterminate results).

JTAG Support

The IDT70V5388/78 provides a serial boundary scan test access port . The JTAG tables starting on page 29 provide the specific details for the JTAG implementation on this device.

The IDT70V5388/78 executes a JTAG test logic reset upon power-up. This power-up reset will initialize the TAP controller and MBIST controller. In most power environments no further action is required. However, if the user has any concern about the system's voltage states during power-up, then the user can use the optional $\overline{TRST}$ input as part of a board's power on reset sequence. The $\overline{TRST}$ pin also provides an alternate means of resetting the JTAG test logic when required, and is available for use by external JTAG controllers as an asynchronous reset signal. If the user does not plan to rely on the optional $\overline{TRST}$ pin, but wants to use JTAG functionality, the $\overline{TRST}$ pin should either be tied HIGH (preferred implementation) or left floating.

If JTAG operations are not desired, the user has a number of options for disabling the JTAG functions. One would be to simply tie TCK LOW, leaving all other JTAG pins floating (alternatively, TDI and TMS could be tied HIGH). Since the device executes a JTAG reset upon power-up: with TCK tied LOW, no further clocking of the TAP will occur and no JTAG operations will take place. Alternatively, the user can opt to tie $\overline{TRST}$ LOW (either in lieu of or in addition to tying TCK LOW) and the TAP will be locked in a reset condition, blocking all JTAG operations.

Memory Built-In-Test Operations

Go-NoGo Testing

The IDT70V5388/78 is equipped with a self-test function that can be run by the user as the result of a single instruction, implemented via the JTAG TAP interface. If multiple FourPort devices are used on the same board, all can execute MBIST simultaneously, facilitating board checkout.

The MBIST function executes a Go-NoGo test within the device, which then captures pass-fail information and failure count in a special register called the MBIST Result Register (MRR). Upon completion of the test, the MRR can be scanned out via the JTAG interface, using the internal scan operation. Bit zero of the MRR (MRR[0]) is a don't care. Bit one of the MRR (MRR[1])indicates the pass/fail status: a "0" indicates some sort of failure was noted, while a "1" indicates that the memory array passed. The rest of the MRR contains the total number of failed read cycles in the entire MBIST sequence.

The IDT70V5388/78 MBIST function has been supplemented with the ability for the user to force a failure report from the device. This allows the user the flexibility of validating the MBIST function itself, by verifying that the device is able to report faults as well as passing results. The two modes of operation, normal MBIST testing and forced error reporting, are controlled via the JTAG TAP interface using the instruction PROGRAM_MBIST_MODE_SELECT. For further detail, please refer to the System Interface Parameters table on page 28.

The MBIST function executes once the RUNBIST instruction is input via the JTAG interface. The entire MBIST test will be performed with a deterministic number of TCK cycles depending on the TCK and CLKMBIST frequency. This can be calculated by using the following formula:

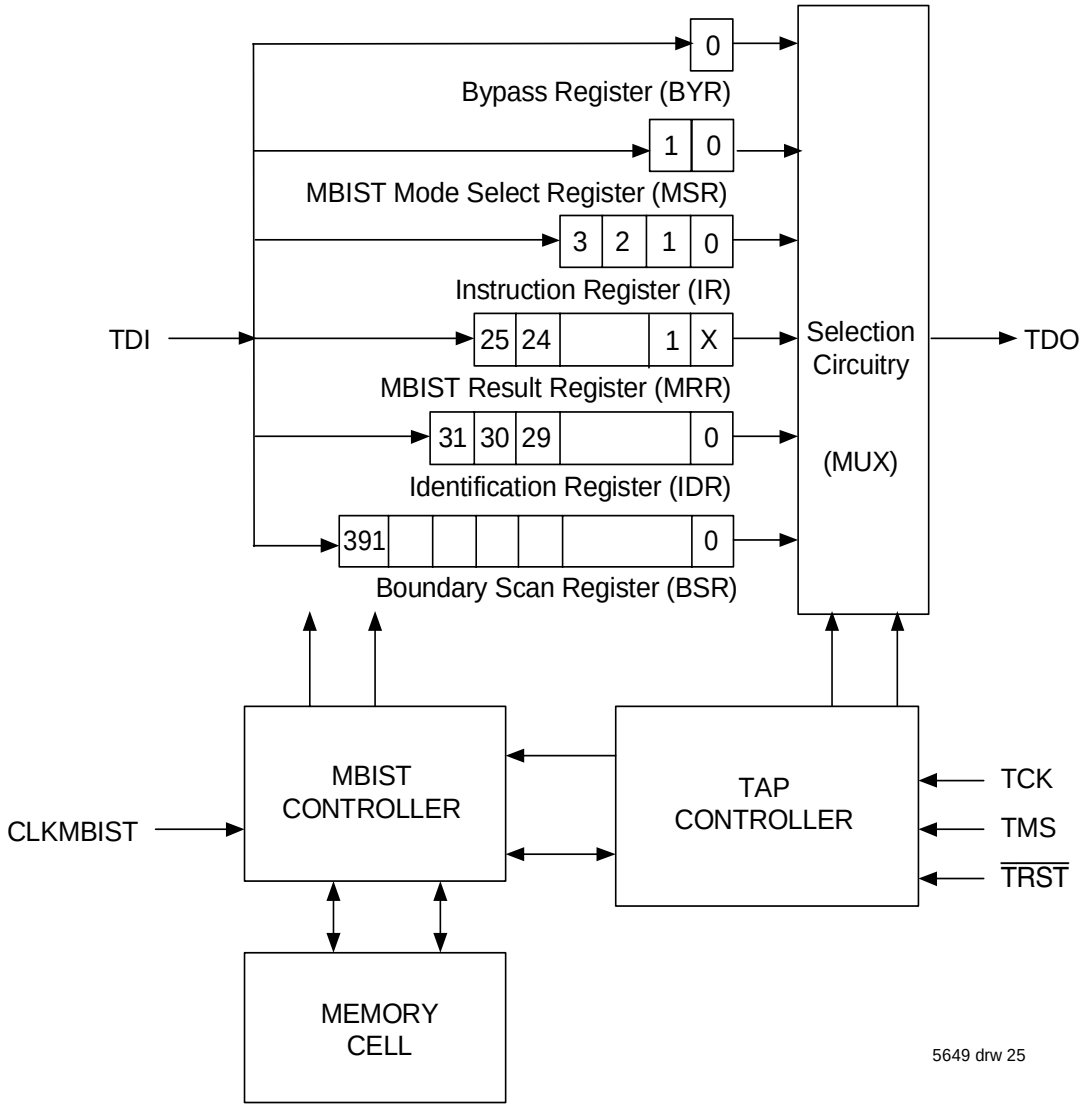
$$t_{CYC} = \frac{t_{CYC[CLKMBIST]}}{t_{CYC[TCK]}} \times m + SPC, \text{ where:}$$

t_{CYC} is the total number of TCK cycles required to run MBIST.

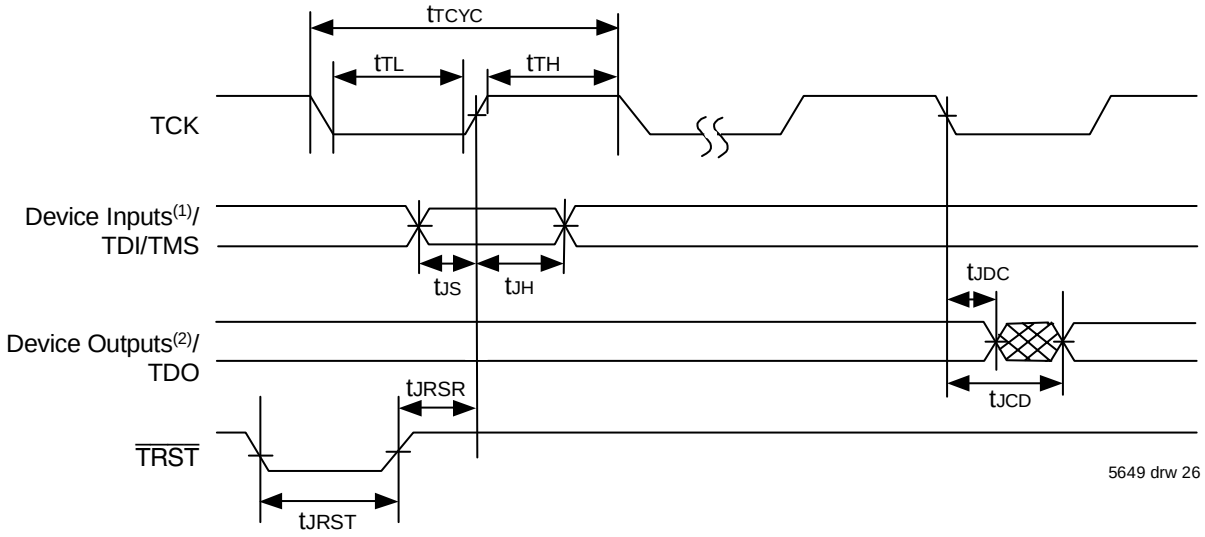
SPC is the synchronization padding cycles (typically 4-6 cycles, to accommodate state machine overhead, turn-around cycles, etc.)

m is a constant that represents the number of read and write operations required to run the internal MBIST algorithms (14,811,136) for both IDT70V5388 and IDT70V5378.

JTAG/BIST TAP Controller Block Diagram



JTAG Timing Specifications



NOTES:

1. Device inputs = All device inputs except TDI, TMS, and $\overline{\text{TRST}}$.
2. Device outputs = All device outputs except TDO.
3. To reset the test (JTAG) port without resetting the device, TMS must be held LOW for 5 cycles, or $\overline{\text{TRST}}$ must be held LOW for one cycle.

Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	0x0	Reserved for version number
IDT Device ID (27:12)	0x31D(1)	Defines IDT part number
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register

5649 tbl 15

NOTE:
1. Device ID for IDT70V5378 is 0x31E.

Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
MBIST Mode Select Register (MSR)	2
Bypass (BYR)	1
Identification (IDR)	32
Boundary Scan (BSR)	392 Note (3)
MBIST Result (MRR)	26

5649 tbl 16

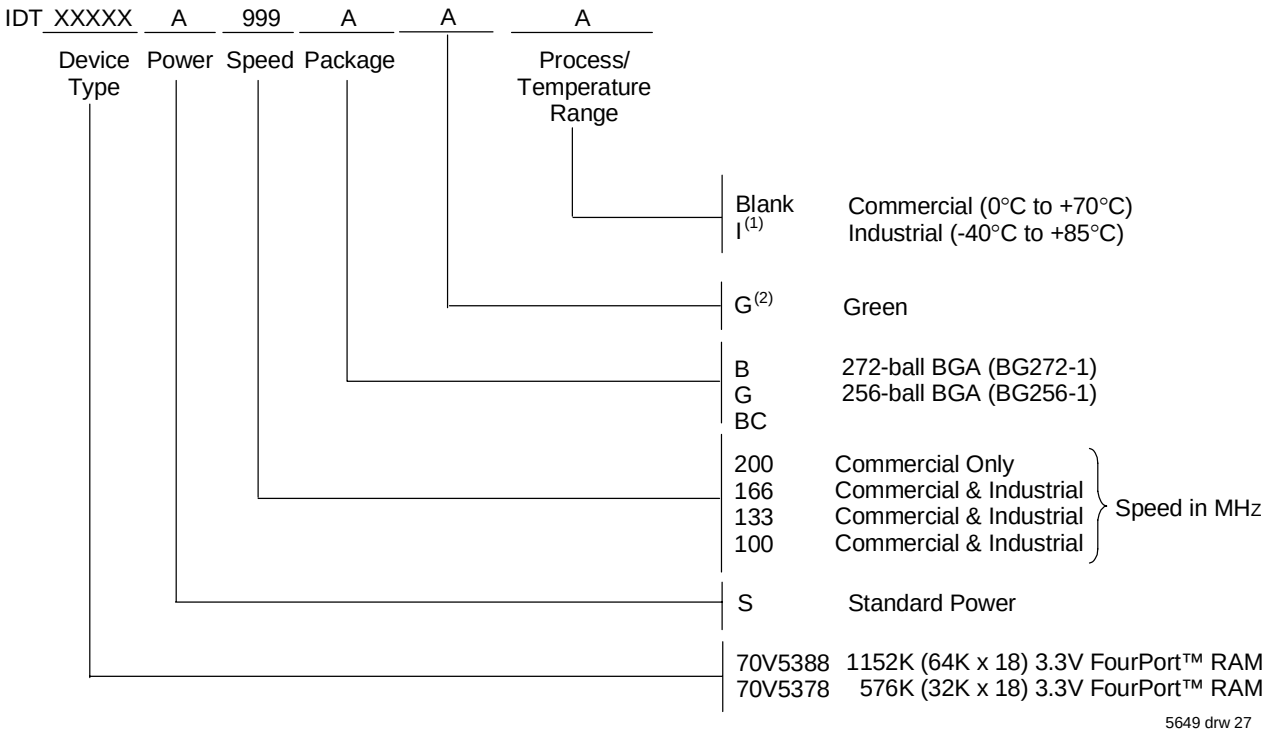
System Interface Parameters

Instruction	Code	Description
EXTEST	0000	Forces contents of the boundary scan cells onto the device outputs(1). Places the boundary scan register (BSR) between TDI and TDO.
BYPASS	1111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	0111	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0110	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state.
SAMPLE/PRELOAD	0001	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs(2) to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.
MBIST_MODE_SELECT	1010	Places the MBIST Mode Register between TDI and TDO. A value of '00' written into this register will allow MBIST to run in standard memory test mode, outputting valid results as appropriate via the MBIST Result Register. A value of '11' written into the MBIST Mode Register will force the MBIST Result Register (MRR) to report a result of 'FAIL'., with 8E0000 failed read cycles noted (i.e., the MRR content = (8E0000h, 0, x). The value of the MBIST Mode Register is not guaranteed at power-up and is not affected by Master reset and JTAG reset.
RUNBIST	1000	Invokes MBIST. Internally updates MBIST result register with Go-NoGo information and number of issues. PROGRAM_MBIST_MODE_REGISTER must be run prior to executing RUNBIST in order to ensure valid results. There is no need to repeat this instruction unless the mode of operation is changed: the MMR will retain its programmed value until overwritten or the device is powered down.
INT_SCAN	0100	Scans out partial information. Places MBIST result register (MRR) between TDI & TDO.
CLAMP	0101	Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the Bypass register (BYR) between TDI & TDO.
RESERVED	0010, 0011	Several combinations are reserved. Do not use codes other than those identified above.
PRIVATE	1001, 1011, 1100, 1101, 1110	Several combinations arePRIVATE (for IDT internal use). Do not use codes other than those identified above.

5649 tbl 17

NOTES:
1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and $\overline{\text{TRST}}$.
3. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website (www.idt.com), or by contacting your local IDT sales representative.

Ordering Information



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NOTES:
1. Contact your local sales office for industrial temp. range for other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.

Datasheet Document History

08/20/02:		Initial Public Datasheet
09/25/02:		Added 0.5M Density to Datasheet
08/20/03:	Page 10	Changed power numbers in DC Electrical Characteristics table Removed Preliminary status
01/31/06:	Page 1	Added green availability to features
	Page 29	Added green indicator to ordering information

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