LOW SKEW, 1-TO-24 DIFFERENTIAL-TO-LVCMOS/LVTTL FANOUT BUFFER

ICS8344I

General Description

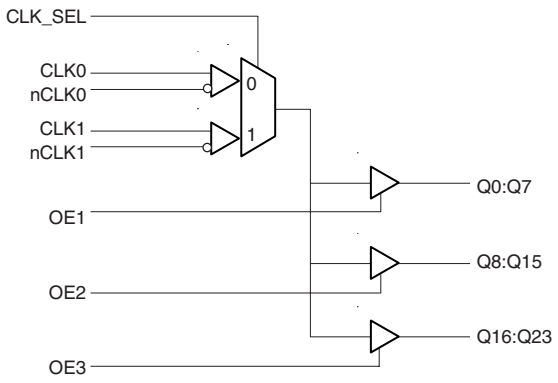
The ICS8344I is a low voltage, low skew fanout buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS8344I has two selectable clock inputs. The CLK0, nCLK0 and CLK1, nCLK1 pairs can accept most standard differential input levels. The ICS8344I is designed to translate any differential signal levels to LVCMOS/LVTTL levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased to 48 by utilizing the ability of the outputs to drive two series terminated lines. Redundant clock applications can make use of the dual clock input. The dual clock inputs also facilitate board level testing. ICS8344I is characterized at full 3.3V, full 2.5V and mixed 3.3V input and 2.5V output operating supply modes.

Guaranteed output and part-to-part skew characteristics make the ICS8344I ideal for those clock distribution applications demanding well defined performance and repeatability.

Features

- Twenty-four LVCMOS/LVTTL outputs, 7Ω typical output impedance
- Two selectable differential clock input pairs for redundant clock applications
- CLKx, nCLKx pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 100MHz
- Translates any single-ended input signal to LVCMOS/LVTTL with resistor bias on nCLK input
- Multiple output enable pins for disabling unused outputs in reduced fanout applications
- Output skew: 275ps (maximum)
- Part-to-part skew: 600ps (maximum)
- Bank skew: 150ps (maximum)
- Supply modes:
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment

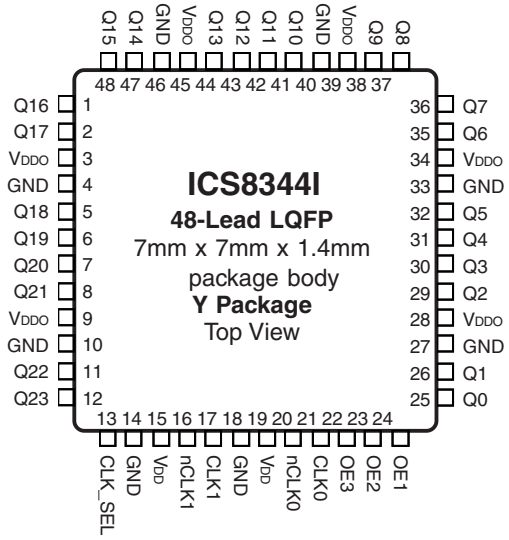


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2, 5, 6 7, 8, 11, 12	Q16, Q17, Q18, Q19 Q20, Q21, Q22, Q23	Output		Single-ended LVCMOS/LVTTL outputs. 7Ω typical output impedance.
3, 9, 28, 34, 39, 45	V_{DDO}	Power		Output supply pins.
4, 10, 14,18, 27, 33, 40, 46	GND	Power		Power supply ground.
13	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1, nCLK1 inputs. When LOW, selects CLK0, nCLK0. LVTTL / LVCMOS interface levels.
15, 19	V_{DD}	Power		Positive supply pins.
16	nCLK1	Input	Pullup	Inverting differential clock input.
17	CLK1	Input	Pulldown	Non-inverting differential clock input.
20	nCLK0	Input	Pullup	Inverting differential clock input.
21	CLK0	Input	Pulldown	Non-inverting differential clock input.
22	OE3	Input	Pullup	Output enable. Controls enabling and disabling of outputs Q16 through Q23. LVCMOS/LVTTL interface levels.
23	OE2	Input	Pullup	Output enable. Controls enabling and disabling of outputs Q8 through Q15. LVCMOS/LVTTL interface levels.
24	OE1	Input	Pullup	Output enable. Controls enabling and disabling of outputs Q0 through Q7. LVCMOS/LVTTL interface levels.
25, 26, 29, 30 31, 32, 35, 36	Q0, Q1, Q2, Q3 Q4, Q5, Q6, Q7	Output		Single-ended LVCMOS/LVTTL outputs. 7Ω typical output impedance.
37, 38, 41, 42 43, 44, 47, 48	Q8, Q9, Q10, Q11 Q12, Q13, Q14, Q15	Output		Single-ended LVCMOS/LVTTL outputs. 7Ω typical output impedance.

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)				20	pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance			7		Ω

TABLE 3A. OUTPUT ENABLE FUNCTION TABLE

Bank 1		Bank 2		Bank 3	
Input	Output	Input	Output	Input	Output
OE1	Q0-Q7	OE2	Q8-Q15	OE3	Q16-Q23
0	Hi-Z	0	Hi-Z	0	Hi-Z
1	Enabled	1	Enabled	1	Enabled

TABLE 3B. CLOCK SELECT FUNCTION TABLE

Control Input	Clock	
CLK_SEL	CLK0, nCLK0	CLK1, nCLK1
0	Selected	De-selected
1	De-selected	Selected

TABLE 3C. CLOCK INPUT FUNCTION TABLE

Inputs			Outputs	Input to Output Mode	Polarity
OE1, OE2, OE3	CLK	nCLK	Q0 thru Q23		
1	0	1	LOW	Differential to Single Ended	Non Inverting
1	1	0	HIGH	Differential to Single Ended	Non Inverting
1	0	Biased; NOTE 1	LOW	Single Ended to Differential	Non Inverting
1	1	Biased; NOTE 1	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	0	HIGH	Single Ended to Differential	Inverting
1	Biased; NOTE 1	1	LOW	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section on page 13, Figure 8, which discusses wiring the differential input to accept single ended levels.

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Quiescent Power Supply Current				95	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = 3.3V±5\%$, $V_{DDO} = 2.5V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Quiescent Power Supply Current				95	mA

Table 4C. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 2.5V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Quiescent Power Supply Current				95	mA

TABLE 4D. LVCMOS DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK_SEL, OE1, OE2, OE3		2		3.8	V
V_{IL}	Input Low Voltage	CLK_SEL, OE1, OE2, OE3		-0.3		0.8	V
I_{IH}	Input High Current	OE1, OE2, OE3	$V_{DD} = V_{IN} = 3.465V$			5	µA
		CLK_SEL	$V_{DD} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	OE1, OE2, OE3	$V_{DD} = 3.465$, $V_{IN} = 0V$	-150			µA
		CLK_SEL	$V_{DD} = 3.465$, $V_{IN} = 0V$	-5			µA
V_{OH}	Output High Voltage		$V_{DD} = V_{DDO} = 3.135V$ I_{OH} = -36mA	2.6			V
V_{OL}	Output Low Voltage		$V_{DD} = V_{DDO} = 3.135V$ I_{OL} = 36mA			0.6	V

TABLE 4E. LVCMOS DC CHARACTERISTICS, $V_{DD} = 3.3V±5\%$, $V_{DDO} = 2.5V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK_SEL, OE1, OE2, OE3		2		3.8	V
V_{IL}	Input Low Voltage	CLK_SEL, OE1, OE2, OE3		-0.3		0.8	V
I_{IH}	Input High Current	OE1, OE2, OE3	$V_{DD} = V_{IN} = 3.465V$			5	µA
		CLK_SEL	$V_{DD} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	OE1, OE2, OE3	$V_{DD} = 3.465$, $V_{IN} = 0V$	-150			µA
		CLK_SEL	$V_{DD} = 3.465$, $V_{IN} = 0$	-5			µA
V_{OH}	Output High Voltage		$V_{DD} = 3.135V$, $V_{DDO} = 2.375V$ I_{OH} = -27mA	2			V
V_{OL}	Output Low Voltage		$V_{DD} = 3.135V$, $V_{DDO} = 2.365V$ I_{OL} = 27mA			0.63	V

TABLE 4F. LVCMOS DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK_SEL, OE1, OE2, OE3		2		2.9	V
V_{IL}	Input Low Voltage	CLK_SEL, OE1, OE2, OE3		-0.3		0.8	V
I_{IH}	Input High Current	OE1, OE2, OE3	$V_{DD} = V_{IN} = 2.625V$			5	µA
		CLK_SEL	$V_{DD} = V_{IN} = 2.625V$			150	µA
I_{IL}	Input Low Current	OE1, OE2, OE3	$V_{DD} = 2.625$, $V_{IN} = 0V$	-150			µA
		CLK_SEL	$V_{DD} = 2.625$, $V_{IN} = 0V$	-5			µA
V_{OH}	Output High Voltage		V_{DD} = VDDO = 2.375V I_{OH} = -27mA	2			V
V_{OL}	Output Low Voltage		V_{DD} = VDDO = 2.375V I_{OL} = 27mA			0.6	V

TABLE 4G. DIFFERENTIAL DC CHARACTERISTICS, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK0, nCLK1				5	µA
		CLK0, CLK1				150	µA
I_{IL}	Input Low Current	nCLK0, nCLK1		-150			µA
		CLK0, CLK1		-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				100	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	f ≤ 100MHz	2.6		4.3	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1	f ≤ 100MHz	2.4		4.3	ns
*t*sk(b)	Bank Skew; NOTE 2, 6				150	ps
*t*sk(o)	Output Skew; NOTE 3, 6				275	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6				600	ps
t_R	Output Rise Time; NOTE 5	30% to 70%	300		1700	ps
t_F	Output Fall Time; NOTE 5	30% to 70%	300		1400	ps
odc	Output Duty Cycle		40%		60%	%
t_{EN}	Output Enable Time; NOTE 5	f = 66.7MHz			5	ns
t_{DIS}	Output Disable TIme; NOTE 5	f = 66.7MHz			4	ns

All parameters measured at 100MHz unless noted otherwise.
NOTE 1: Measured from the diffferential input crossing point to $V_{DDO}/2$.
NOTE 2: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at $V_{DDO}/2$.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				100	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	f ≤ 100MHz	2.6		4.5	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1	f ≤ 100MHz	2.6		4.5	ns
*t*sk(b)	Bank Skew; NOTE 2, 6				150	ps
*t*sk(o)	Output Skew; NOTE 3, 6				275	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6				600	ps
t_R	Output Rise Time; NOTE 5	30% to 70%	300		1700	ps
t_F	Output Fall Time; NOTE 5	30% to 70%	300		1400	ps
odc	Output Duty Cycle		40%		60%	%
t_{EN}	Output Enable Time; NOTE 5	f = 66.7MHz			6	ns
t_{DIS}	Output Disable TIme; NOTE 5	f = 66.7MHz			6	ns

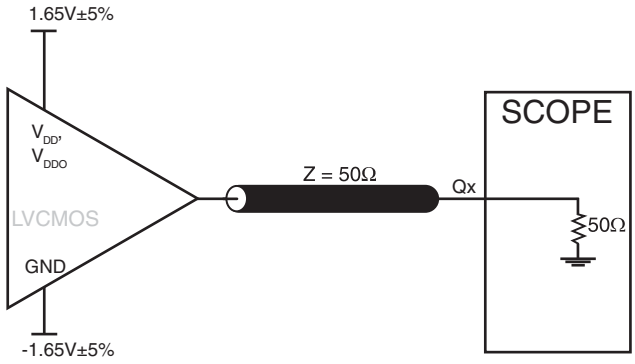
All parameters measured at 100MHz unless noted otherwise.
NOTE 1: Measured from the diffferential input crossing point to V_{DDO}/2.
NOTE 2: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5C. AC CHARACTERISTICS, V_{DD} = V_{DDO} = 2.5V±5%, TA = -40°C TO 85°C

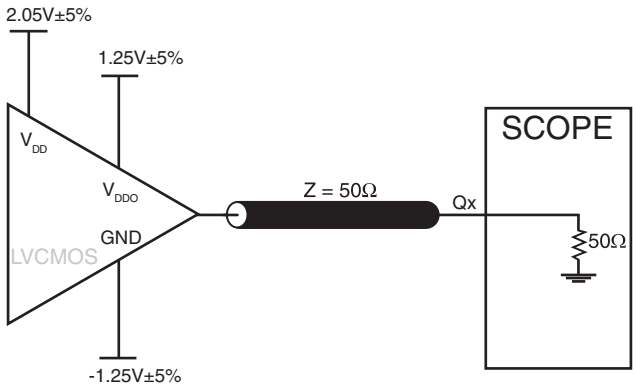
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				100	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	f ≤ 100MHz	2.7		4.3	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1	f ≤ 100MHz	2.7		4.3	ns
*t*sk(b)	Bank Skew; NOTE 2, 6				150	ps
*t*sk(o)	Output Skew; NOTE 3, 6				275	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6				600	ps
t_R	Output Rise Time; NOTE 5	30% to 70%	300		1700	ps
t_F	Output Fall Time; NOTE 5	30% to 70%	300		1400	ps
odc	Output Duty Cycle		40%		60%	%
t_{EN}	Output Enable Time; NOTE 5	f = 66.7MHz			6	ns
t_{DIS}	Output Disable TIme; NOTE 5	f = 66.7MHz			6	ns

For NOTES, please see Table 5B above.

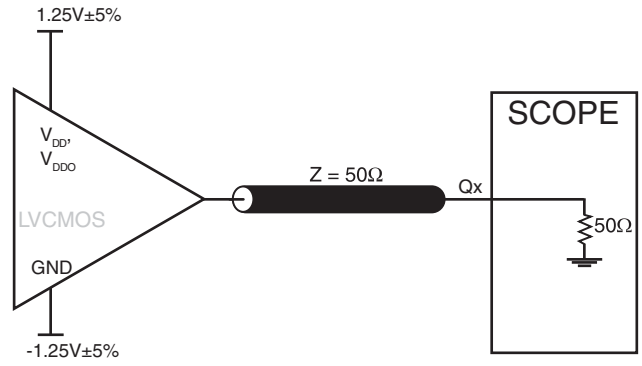
PARAMETER MEASUREMENT INFORMATION



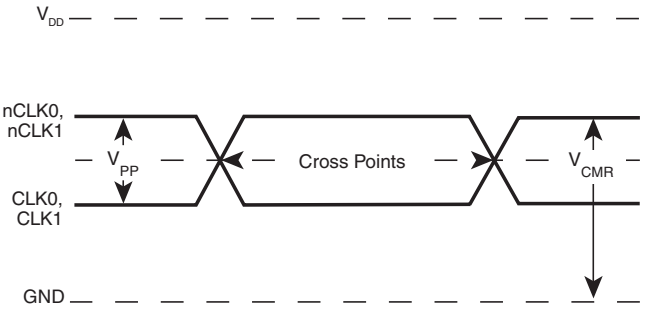
3.3V OUTPUT LOAD AC TEST CIRCUIT



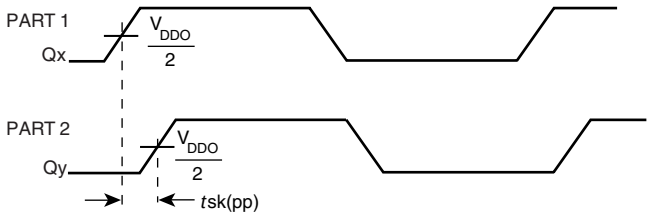
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



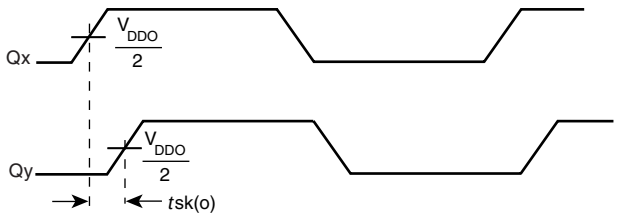
2.5V OUTPUT LOAD AC TEST CIRCUIT



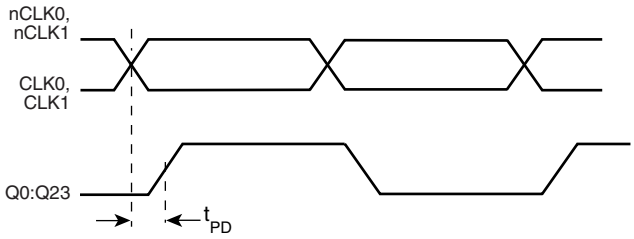
DIFFERENTIAL INPUT LEVEL



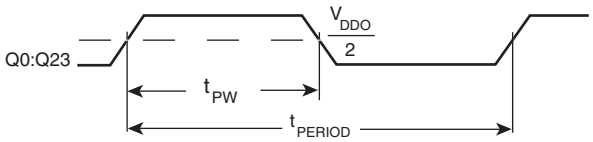
PART-TO-PART SKEW



OUTPUT SKEW

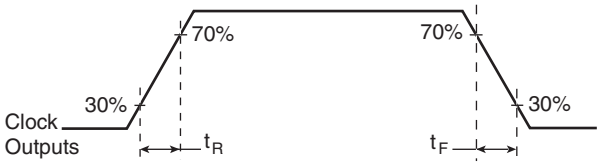


PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

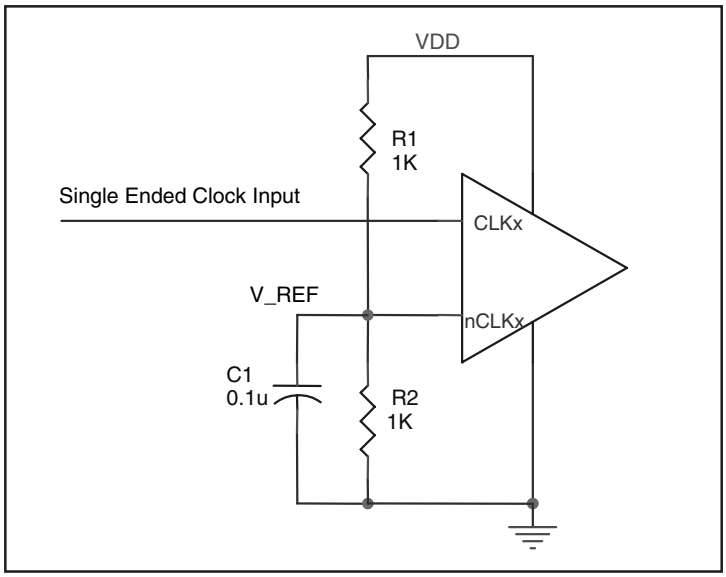


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK/nCLK INPUTS

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUTS

All unused LVCMOS output can be left floating. There should be no trace attached.

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A,* the input termination applies for IDT HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

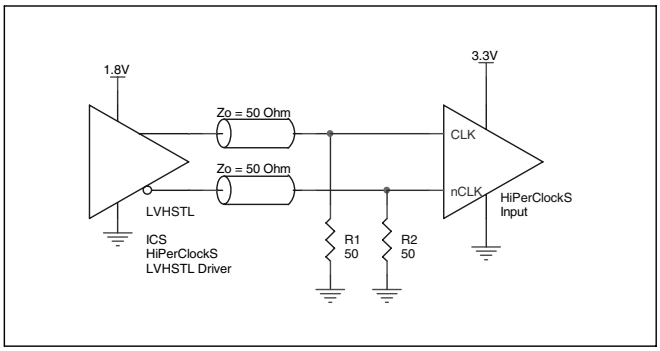


Figure 2A. HiPerClockS CLK/nCLK Input Driven by IDT HiPerClockS LVHSTL Driver

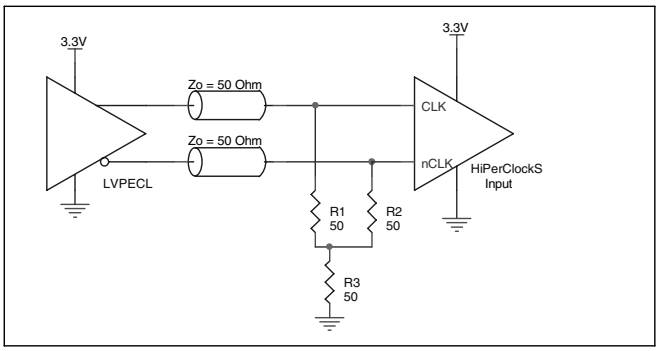


Figure 2B. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

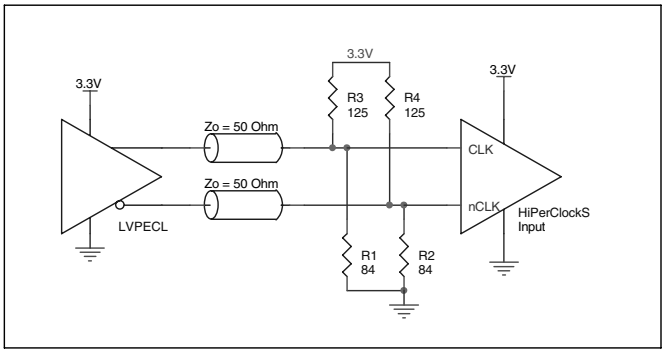


Figure 2C. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

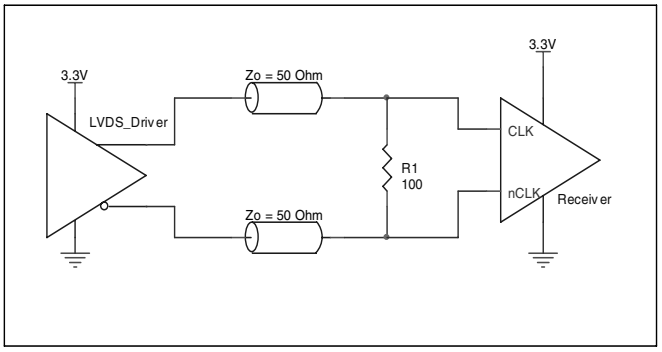


Figure 2D. HiPerClockS CLK/nCLK Input Driven by 3.3V LVDS Driver

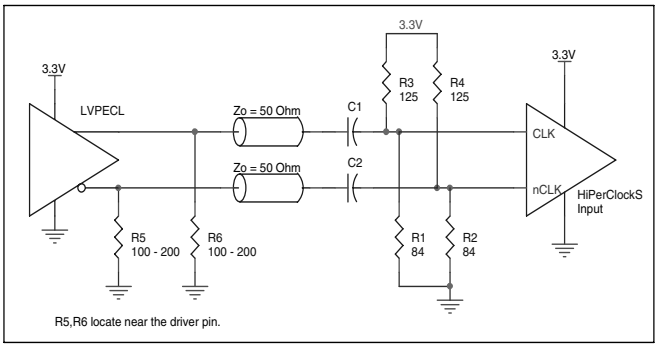


Figure 2E. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver with AC Couple

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 48 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8344I is: 1,449

Package Outline - Y Suffix for 48 Lead LQFP

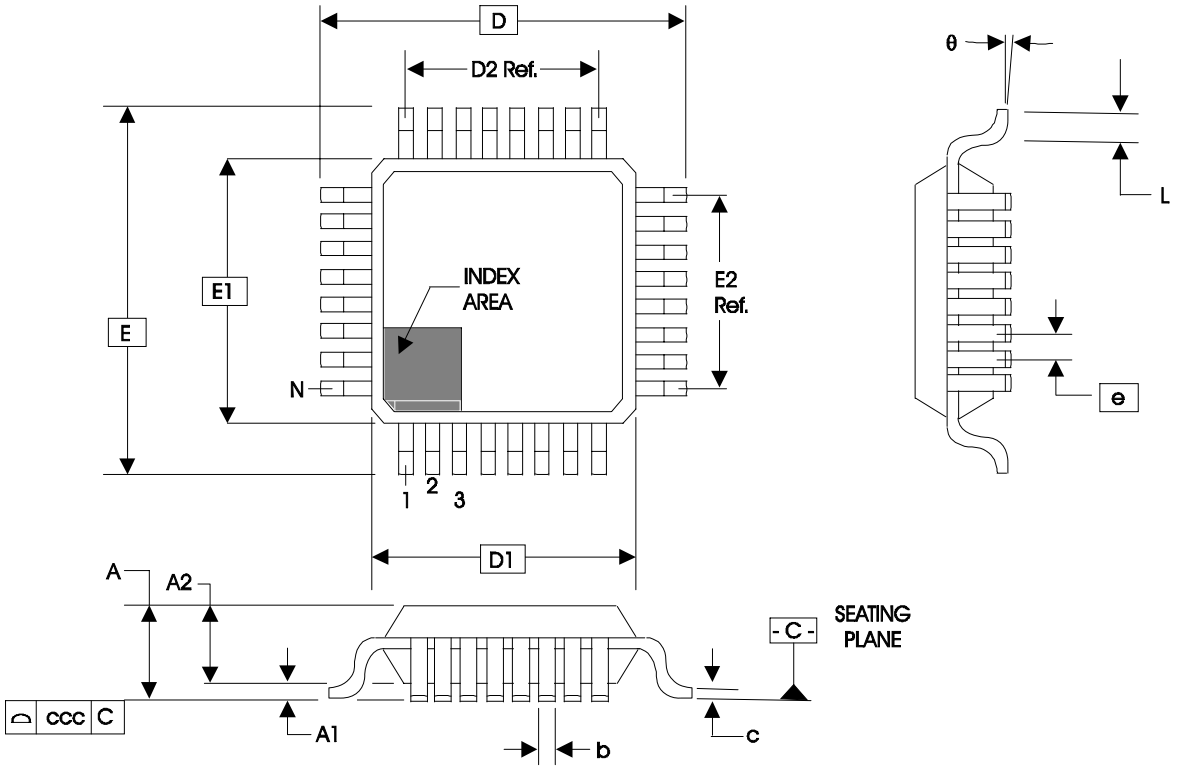


Table 7. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N		48	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50 Ref.	
e		0.50 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8344BYI	ICS8344BYI	48 Lead LQFP	tray	-40°C to 85°C
8344BYIT	ICS8344BYI	48 Lead LQFP	1000 tape & reel	-40°C to 85°C
8344BYILF	ICS8344BYILF	48 lead "Lead-Free" LQFP	tray	-40°C to 85°C
8344BYILFT	ICS8344BYILF	48 lead "Lead-Free" LQFP	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B		1 10 11 14	Features Section - added lead-free bullet. Pin Characteristics Table - changed C_{IN} 4pF max. to 4pF typical. Added *Recommendations for Unused Input and Output Pins.* Added *Differential Clock Input Interface.* Ordering Information Table - added lead-free part number, marking and note. Updated format throughout the datasheet.	5/23/07

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support
netcom@idt.com
480-763-2056

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan
Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe
IDT Europe, Limited
321 Kingston Road
Leatherhead, Surrey
KT22 7TU
England
+44 (0) 1372 363 339
Fax: +44 (0) 1372 378851

www.IDT.com