

### General Description

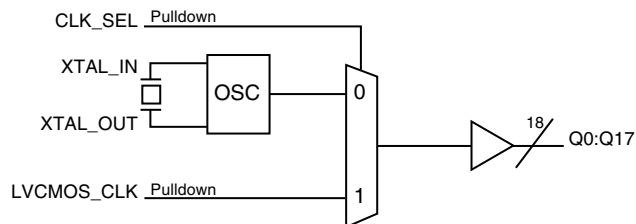
The 83918 is a low skew, 1:18 Crystal-to- LVCMOS/LVTTL Fanout Buffer. The 83918 has selectable LVCMOS/LVTTL clock or crystal inputs. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines.

The 83918 is characterized at full 3.3V, full 2.5V and mixed 3.3V/2.5V, 3.3V/1.8V, and 2.5V/1.8V output operating supply modes. Guaranteed output and part-to-part skew characteristics make the 83918 ideal for those clock distribution applications demanding well defined performance and repeatability.

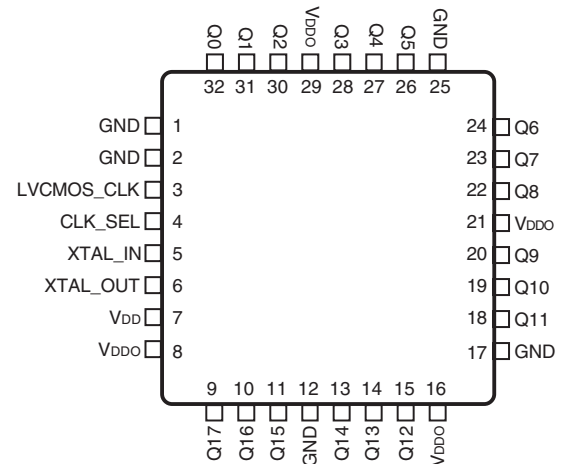
### Features

- Eighteen LVCMOS/LVTTL output
- Selectable crystal oscillator interface or LVCMOS\_CLK
- Maximum output frequency: 200MHz
- Crystal input frequency range: 10MHz to 40MHz
- RMS phase jitter using a 25MHz crystal (1kHz – 1MHz): 0.449ps (typical) @ 3.3V/3.3V
- Output skew: 75ps (maximum) @ 3.3V/3.3V
- Operating supply modes:  
Core/Output  
3.3V/3.3V  
3.3V/2.5V  
3.3V/1.8V  
2.5V/2.5V  
2.5V/1.8V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

### Block Diagram



### Pin Assignment



**83918**

**32 Lead LQFP**

**7mm x 7mm x 1.4mm package body**

**Y Package**

**Top View**

**Table 1. Pin Descriptions**

| Number                                                                            | Name                                                                                       | Type   |          | Description                                                                                                         |
|-----------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------|--------|----------|---------------------------------------------------------------------------------------------------------------------|
| 1, 2, 12, 17, 25                                                                  | GND                                                                                        | Power  |          | Power supply ground.                                                                                                |
| 3                                                                                 | LVC MOS_CLK                                                                                | Input  | Pulldown | Single-ended clock input. LVC MOS/LVTTL interface levels.                                                           |
| 4                                                                                 | CLK_SEL                                                                                    | Input  | Pulldown | Clock select pin. When HIGH, selects LVC MOS_CLK. When LOW, selects crystal inputs. LVC MOS/LVTTL interface levels. |
| 5,<br>6                                                                           | XTAL_IN,<br>XTAL_OUT                                                                       | Input  |          | Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.                                         |
| 7                                                                                 | V <sub>DD</sub>                                                                            | Power  |          | Positive supply pin.                                                                                                |
| 8, 16, 21, 29                                                                     | V <sub>DDO</sub>                                                                           | Power  |          | Output supply pins.                                                                                                 |
| 9, 10, 11,<br>13, 14, 15,<br>18, 19, 20, 22,<br>23, 24, 26, 27,<br>28, 30, 31, 32 | Q17, Q16, Q15,<br>Q14, Q13, Q12,<br>Q11, Q10, Q9, Q8,<br>Q7, Q6, Q5, Q4,<br>Q3, Q2, Q1, Q0 | Output |          | Single-ended clock outputs. LVC MOS/LVTTL interface levels.                                                         |

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

| Symbol                | Parameter                                  | Test Conditions           | Minimum | Typical | Maximum | Units |
|-----------------------|--------------------------------------------|---------------------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance                          |                           |         | 4       |         | pF    |
| C <sub>PD</sub>       | Power Dissipation Capacitance (per output) | V <sub>DDO</sub> = 3.465V |         | 9       |         | pF    |
|                       |                                            | V <sub>DDO</sub> = 2.625V |         | 8       |         | pF    |
|                       |                                            | V <sub>DDO</sub> = 2V     |         | 8       |         | pF    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor                    |                           |         | 51      |         | kΩ    |
| R <sub>OUT</sub>      | Output Impedance                           | V <sub>DDO</sub> = 3.465V | 18      | 19      | 20      | Ω     |
|                       |                                            | V <sub>DDO</sub> = 2.625V | 20      | 22      | 24      | Ω     |
|                       |                                            | V <sub>DDO</sub> = 2V     | 25      | 29      | 34      | Ω     |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item                                     | Rating                                     |
|------------------------------------------|--------------------------------------------|
| Supply Voltage, $V_{DD}$                 | 4.6V                                       |
| Inputs, $V_I$<br>XTAL_IN<br>Other Inputs | 0V to $V_{DD}$<br>-0.5V to $V_{DD} + 0.5V$ |
| Outputs, $V_O$                           | -0.5V to $V_{DDO} + 0.5V$                  |
| Package Thermal Impedance, $\theta_{JA}$ | 53.5°C/W (0 mps)                           |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C                             |

## DC Electrical Characteristics

**Table 3A. Power Supply DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

| Symbol    | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-------------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Positive Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDO}$ | Output Supply Voltage   |                 | 3.135   | 3.3     | 3.465   | V     |
| $I_{DD}$  | Power Supply Current    |                 |         |         | 24      | mA    |
| $I_{DDO}$ | Output Supply Current   | No Load         |         |         | 27      | mA    |

**Table 3B. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

| Symbol    | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-------------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Positive Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDO}$ | Output Supply Voltage   |                 | 2.375   | 2.5     | 2.625   | V     |
| $I_{DD}$  | Power Supply Current    |                 |         |         | 24      | mA    |
| $I_{DDO}$ | Output Supply Current   | No Load         |         |         | 26      | mA    |

**Table 3C. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

| Symbol    | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-------------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Positive Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDO}$ | Output Supply Voltage   |                 | 1.6     | 1.8     | 2.0     | V     |
| $I_{DD}$  | Power Supply Current    |                 |         |         | 24      | mA    |
| $I_{DDO}$ | Output Supply Current   | No Load         |         |         | 29      | mA    |

**Table 3D. Power Supply DC Characteristics,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol    | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-------------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Positive Supply Voltage |                 | 2.375   | 2.5     | 2.625   | V     |
| $V_{DDO}$ | Output Supply Voltage   |                 | 2.375   | 2.5     | 2.625   | V     |
| $I_{DD}$  | Power Supply Current    |                 |         |         | 23      | mA    |
| $I_{DDO}$ | Output Supply Current   | No Load         |         |         | 25      | mA    |

**Table 3E. Power Supply DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol    | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-------------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Positive Supply Voltage |                 | 2.375   | 2.5     | 2.625   | V     |
| $V_{DDO}$ | Output Supply Voltage   |                 | 1.6     | 1.8     | 2.0     | V     |
| $I_{DD}$  | Power Supply Current    |                 |         |         | 23      | mA    |
| $I_{DDO}$ | Output Supply Current   | No Load         |         |         | 24      | mA    |

**Table 3F. LVCMOS/LVTTL DC Characteristics,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol   | Parameter           | Test Conditions                                          | Minimum         | Typical | Maximum        | Units         |
|----------|---------------------|----------------------------------------------------------|-----------------|---------|----------------|---------------|
| $V_{IH}$ | Input High Voltage  | $V_{DD} = 3.465V$                                        | 2               |         | $V_{DD} + 0.3$ | V             |
|          |                     | $V_{DD} = 2.5V$                                          | 1.7             |         | $V_{DD} + 0.3$ | V             |
| $V_{IL}$ | Input Low Voltage   | $V_{DD} = 3.465V$                                        | -0.3            |         | 0.8            | V             |
|          |                     | $V_{DD} = 2.5V$                                          | -0.3            |         | 0.7            | V             |
| $I_{IH}$ | Input High Current  | CLK_SEL, LVCMOS_CLK<br>$V_{DD} = V_{IN} = 3.465V$        |                 |         | 150            | $\mu\text{A}$ |
| $I_{IL}$ | Input Low Current   | CLK_SEL, LVCMOS_CLK<br>$V_{DD} = 3.465V$ , $V_{IN} = 0V$ | -5              |         |                | $\mu\text{A}$ |
| $V_{OH}$ | Output High Voltage | $V_{DDO} = 3.465V$                                       | 2.6             |         |                | V             |
|          |                     | $V_{DDO} = 2.625V$                                       | 1.8             |         |                | V             |
|          |                     | $V_{DDO} = 2V$                                           | $V_{DDO} - 0.3$ |         |                | V             |
| $V_{OL}$ | Output Low Voltage  | $V_{DDO} = 3.465$ or $2.625V$                            |                 |         | 0.5            | V             |
|          |                     | $V_{DDO} = 2V$                                           |                 |         | 0.35           | V             |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . See Parameter Measurement Information section. *Load Test Circuit diagrams.*

**Table 4. Crystal Characteristics**

| Parameter                          | Test Conditions | Minimum     | Typical | Maximum | Units    |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation                |                 | Fundamental |         |         |          |
| Frequency                          |                 | 10          |         | 40      | MHz      |
| Equivalent Series Resistance (ESR) |                 |             |         | 50      | $\Omega$ |
| Shunt Capacitance                  |                 |             |         | 7       | pF       |

## AC Electrical Characteristics

**Table 5A. AC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

| Symbol               | Parameter                                                             | Test Conditions                                 | Minimum | Typical | Maximum | Units |
|----------------------|-----------------------------------------------------------------------|-------------------------------------------------|---------|---------|---------|-------|
| $f_{OUT}$            | Output Frequency                                                      |                                                 |         |         | 200     | MHz   |
| $t_{PLH}$            | Propagation Delay, Low to High;<br>NOTE 1                             |                                                 | 1.85    |         | 3.0     | ns    |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter, (Random);<br>NOTE 2                                 | 25MHz,<br>Integration Range: 1kHz to 1MHz       |         | 0.449   |         | ps    |
| $f_{jit}$            | Additive Phase Jitter, RMS; refer<br>to Additive Phase Jitter Section | 155.52MHz,<br>Integration Range: 12kHz to 20MHz |         | 0.145   |         | ps    |
| $t_{sk(o)}$          | Output Skew; NOTE 3, 6                                                |                                                 |         |         | 75      | ps    |
| $t_{sk(pp)}$         | Part-to-Part Skew; NOTE 4, 6                                          |                                                 |         |         | 800     | ps    |
| $t_R / t_F$          | Output Rise/Fall Time; NOTE 5                                         | 20% to 80%                                      | 300     |         | 700     | ps    |
| odc                  | Output Duty Cycle                                                     | $f_{OUT} \leq 150\text{MHz}$                    | 45      |         | 55      | %     |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at  $f_{OUT}$  unless noted otherwise.

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: Refer to the Phase Noise Plot following this section.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 4: Defined as the skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

**Table 5B. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol               | Parameter                                                          | Test Conditions                                 | Minimum | Typical | Maximum | Units |
|----------------------|--------------------------------------------------------------------|-------------------------------------------------|---------|---------|---------|-------|
| $f_{OUT}$            | Output Frequency                                                   |                                                 |         |         | 200     | MHz   |
| $t_{PLH}$            | Propagation Delay, Low to High; NOTE 1                             |                                                 | 2       |         | 3       | ns    |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter, (Random); NOTE 2                                 | 25MHz,<br>Integration Range: 1kHz to 1MHz       |         | 0.465   |         | ps    |
| $f_{jit}$            | Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section | 155.52MHz,<br>Integration Range: 12kHz to 20MHz |         | 0.161   |         | ps    |
| $t_{sk(o)}$          | Output Skew; NOTE 3, 6                                             |                                                 |         |         | 75      | ps    |
| $t_{sk(pp)}$         | Part-to-Part Skew; NOTE 4, 6                                       |                                                 |         |         | 1       | ns    |
| $t_R / t_F$          | Output Rise/Fall Time; NOTE 5                                      | 20% to 80%                                      | 300     |         | 700     | ps    |
| odc                  | Output Duty Cycle                                                  | $f_{OUT} \leq 150\text{MHz}$                    | 45      |         | 55      | %     |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at  $f_{OUT}$  unless noted otherwise.

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: Refer to the Phase Noise Plot following this section.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 4: Defined as the skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

**Table 5C. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol               | Parameter                                                          | Test Conditions                                 | Minimum | Typical | Maximum | Units |
|----------------------|--------------------------------------------------------------------|-------------------------------------------------|---------|---------|---------|-------|
| $f_{OUT}$            | Output Frequency                                                   |                                                 |         |         | 200     | MHz   |
| $t_{PLH}$            | Propagation Delay, Low to High; NOTE 1                             |                                                 | 1.65    |         | 4.3     | ns    |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter, (Random); NOTE 2                                 | 25MHz,<br>Integration Range: 1kHz to 1MHz       |         | 0.595   |         | ps    |
| $f_{jit}$            | Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section | 155.52MHz,<br>Integration Range: 12kHz to 20MHz |         | 0.228   |         | ps    |
| $t_{sk(o)}$          | Output Skew; NOTE 3, 6                                             |                                                 |         |         | 75      | ps    |
| $t_{sk(pp)}$         | Part-to-Part Skew; NOTE 4, 6                                       |                                                 |         |         | 1       | ns    |
| $t_R / t_F$          | Output Rise/Fall Time; NOTE 5                                      | 20% to 80%                                      | 200     |         | 800     | ps    |
| odc                  | Output Duty Cycle                                                  | $f_{OUT} \leq 150\text{MHz}$                    | 40      |         | 60      | %     |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at  $f_{OUT}$  unless noted otherwise.

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: Refer to the Phase Noise Plot following this section.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 4: Defined as the skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

**Table 5D. AC Characteristics,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol               | Parameter                                                          | Test Conditions                                 | Minimum | Typical | Maximum | Units |
|----------------------|--------------------------------------------------------------------|-------------------------------------------------|---------|---------|---------|-------|
| $f_{OUT}$            | Output Frequency                                                   |                                                 |         |         | 200     | MHz   |
| $t_{PLH}$            | Propagation Delay, Low to High; NOTE 1                             |                                                 | 2       |         | 3       | ns    |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter, (Random); NOTE 2                                 | 25MHz,<br>Integration Range: 1kHz to 1MHz       |         | 0.478   |         | ps    |
| $f_{jit}$            | Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section | 155.52MHz,<br>Integration Range: 12kHz to 20MHz |         | 0.157   |         | ps    |
| $t_{sk(o)}$          | Output Skew; NOTE 3, 6                                             |                                                 |         |         | 75      | ps    |
| $t_{sk(pp)}$         | Part-to-Part Skew; NOTE 4, 6                                       |                                                 |         |         | 1       | ns    |
| $t_R / t_F$          | Output Rise/Fall Time; NOTE 5                                      | 20% to 80%                                      | 300     |         | 700     | ps    |
| odc                  | Output Duty Cycle                                                  | $f_{OUT} \leq 150\text{MHz}$                    | 45      |         | 55      | %     |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at  $f_{OUT}$  unless noted otherwise.

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: Refer to the Phase Noise Plot following this section.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 4: Defined as the skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

**Table 5E. AC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol               | Parameter                                                          | Test Conditions                                 | Minimum | Typical | Maximum | Units |
|----------------------|--------------------------------------------------------------------|-------------------------------------------------|---------|---------|---------|-------|
| $f_{OUT}$            | Output Frequency                                                   |                                                 |         |         | 200     | MHz   |
| $t_{PLH}$            | Propagation Delay, Low to High; NOTE 1                             |                                                 | 1.75    |         | 3.85    | ns    |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter, (Random); NOTE 2                                 | 25MHz,<br>Integration Range: 1kHz to 1MHz       |         | 0.591   |         | ps    |
| $f_{jit}$            | Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section | 155.52MHz,<br>Integration Range: 12kHz to 20MHz |         | 0.175   |         | ps    |
| $t_{sk(o)}$          | Output Skew; NOTE 3, 6                                             |                                                 |         |         | 75      | ps    |
| $t_{sk(pp)}$         | Part-to-Part Skew; NOTE 4, 6                                       |                                                 |         |         | 1.15    | ns    |
| $t_R / t_F$          | Output Rise/Fall Time; NOTE 5                                      | 20% to 80%                                      | 200     |         | 800     | ps    |
| odc                  | Output Duty Cycle                                                  | $f_{OUT} \leq 150\text{MHz}$                    | 45      |         | 55      | %     |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at  $f_{OUT}$  unless noted otherwise.

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: Refer to the Phase Noise Plot following this section.

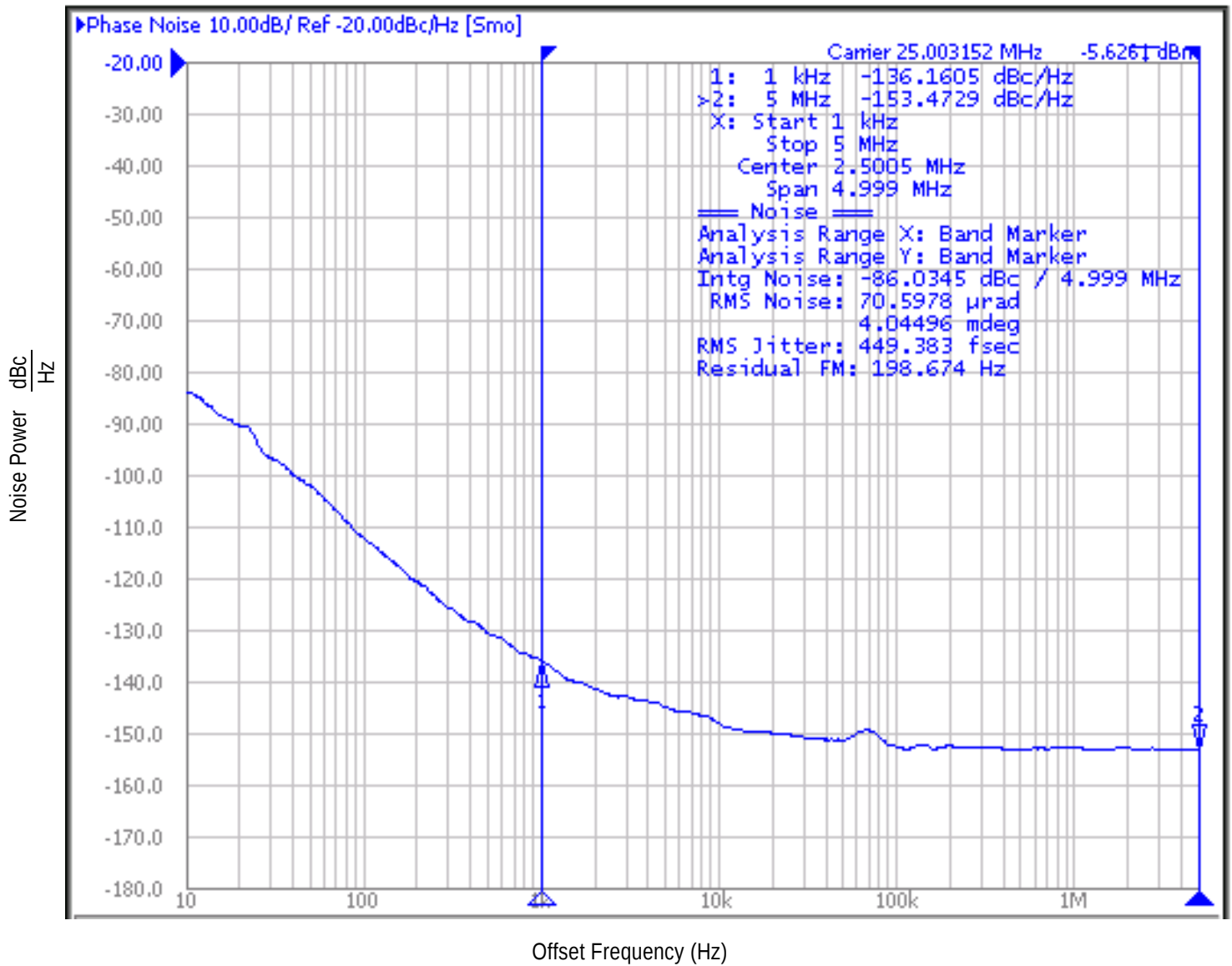
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 4: Defined as the skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

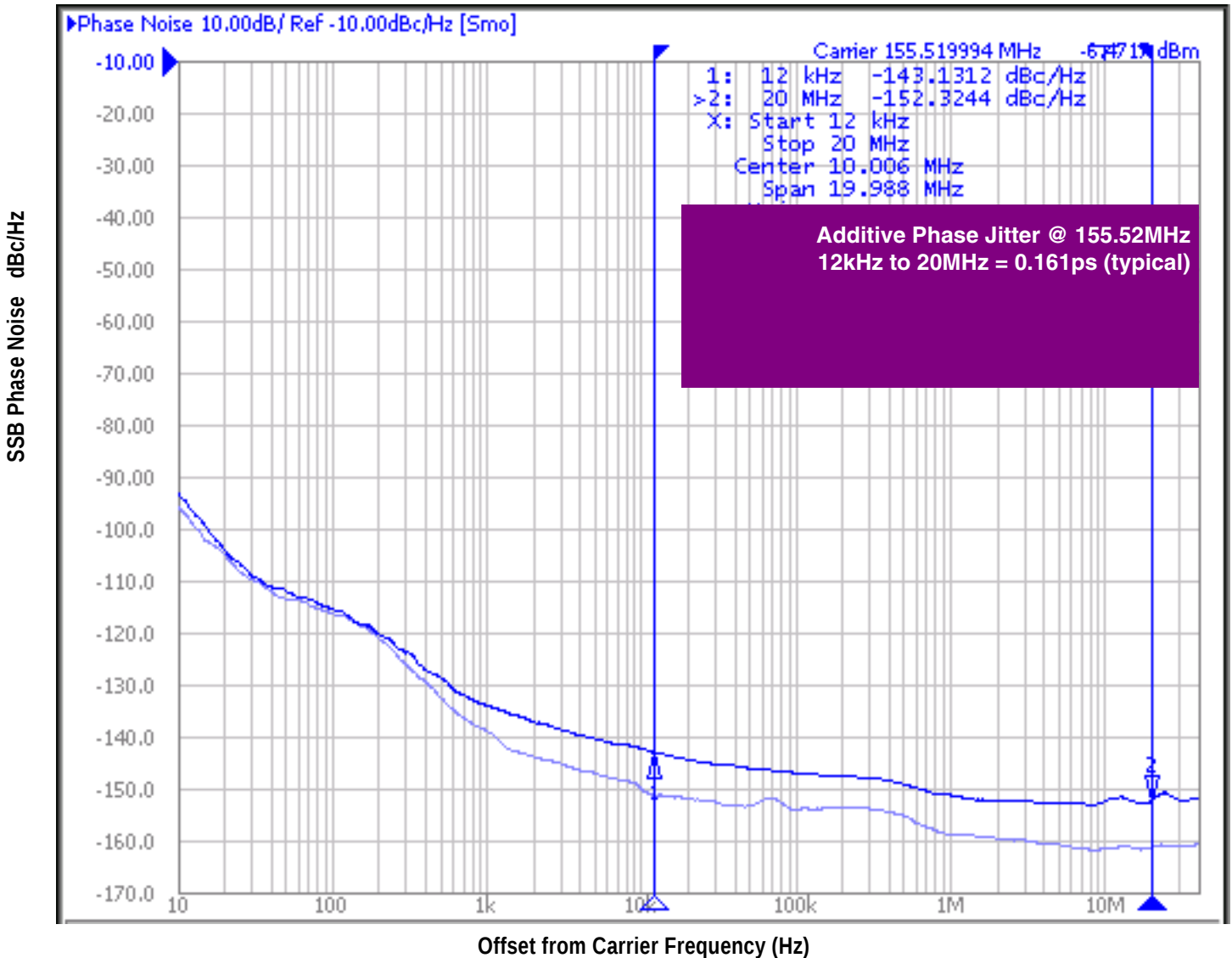
## Typical Phase Noise at 25MHz Crystal (3.3V core/3.3V output)



## Additive Phase Jitter (2.5V output)

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the

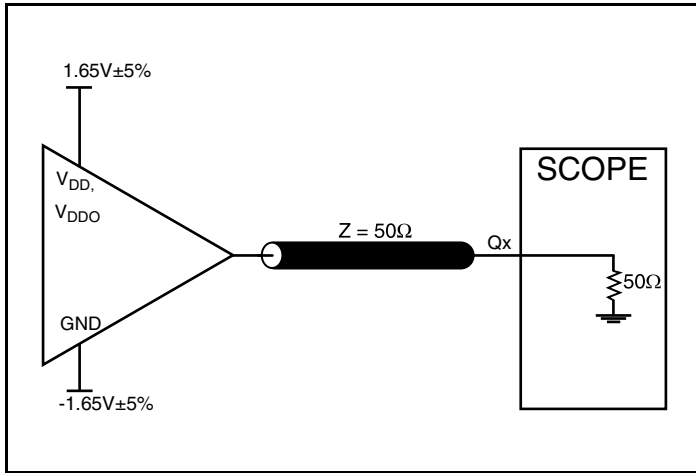
fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



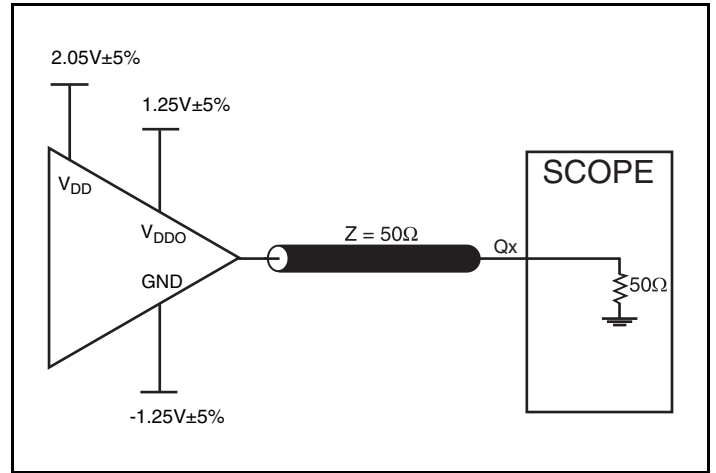
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator "IFR2042 10kHz – 56.4GHz Low Noise Signal Generator as external input to an Agilent 8133A 3GHz Pulse Generator".

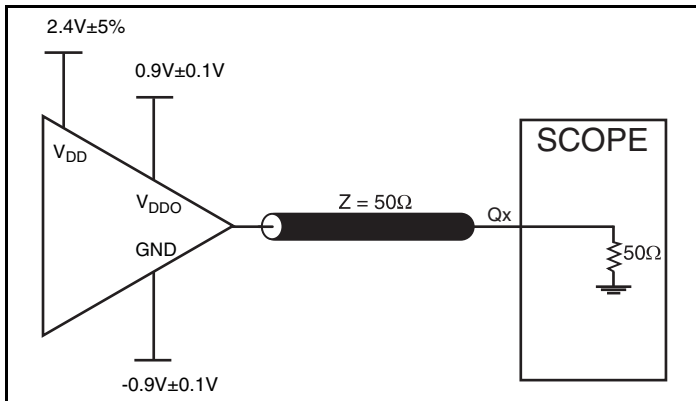
## Parameter Measurement Information



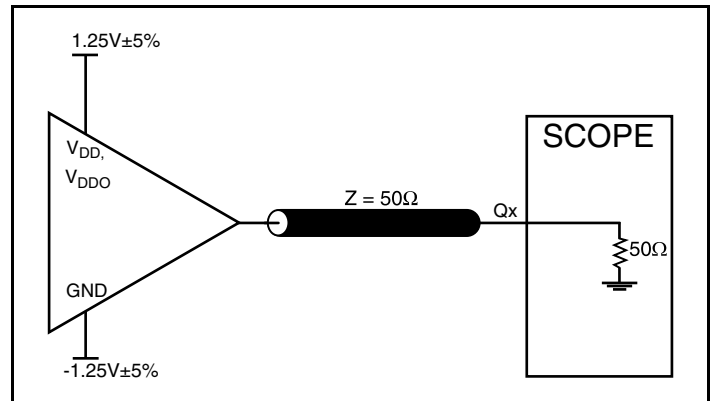
3.3V Core/3.3V Output Load AC Test Circuit



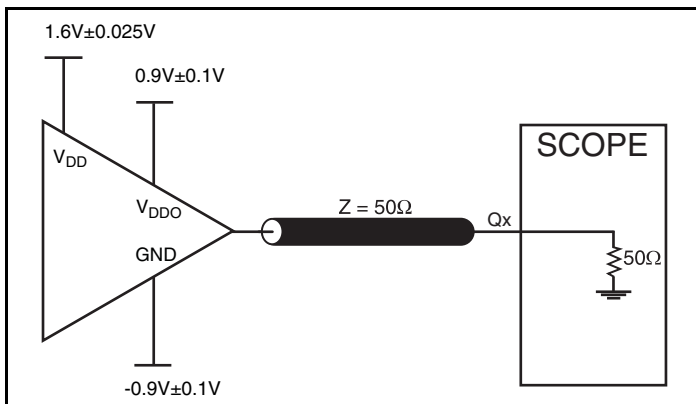
3.3V Core/2.5V Output Load AC Test Circuit



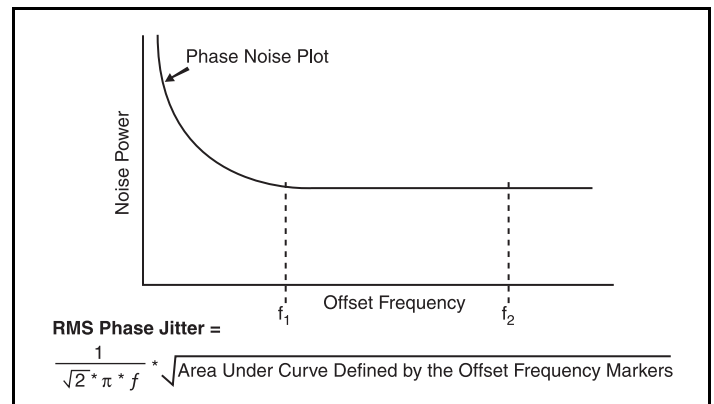
3.3V Core/1.8V Output Load AC Test Circuit



2.5V/2.5V Output Load AC Test Circuit

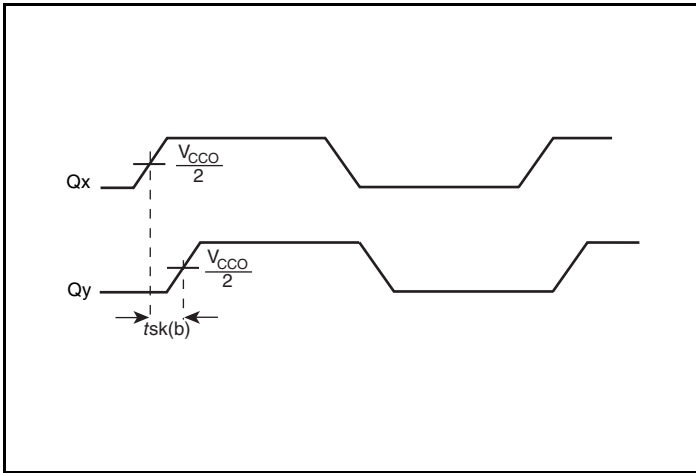


2.5V/1.8V Output Load AC Test Circuit

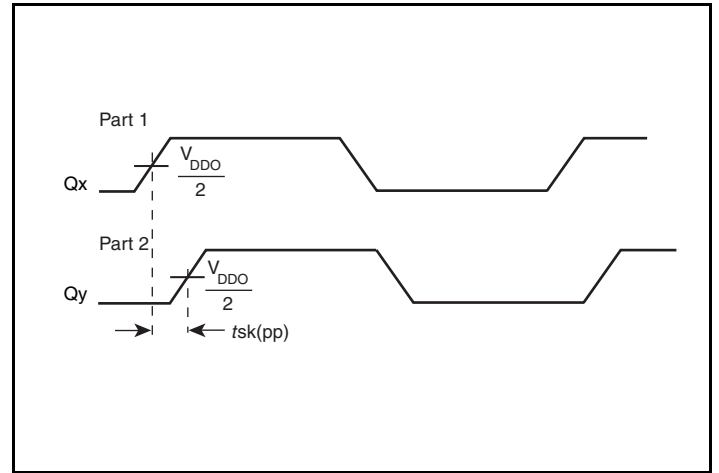


RMS Phase Jitter

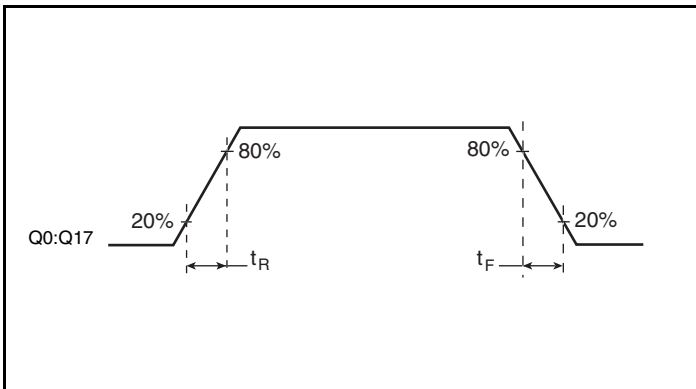
## Parameter Measurement Information, continued



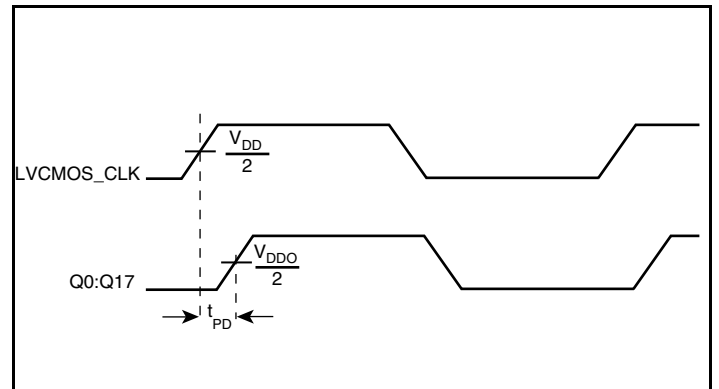
**Output Skew**



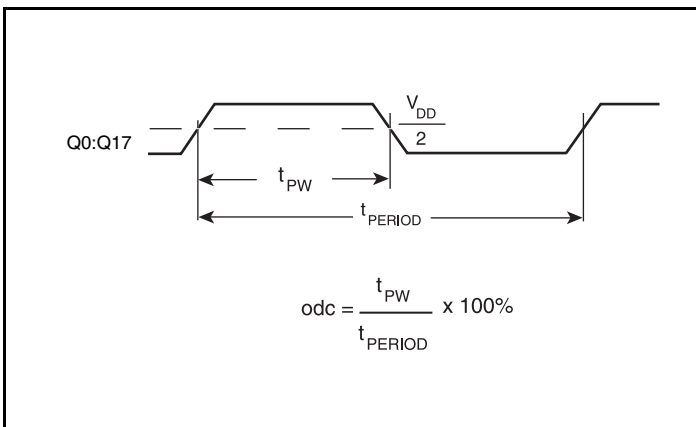
**Part-to-Part Skew**



**Output Rise/Fall Time**



**Propagation Delay**

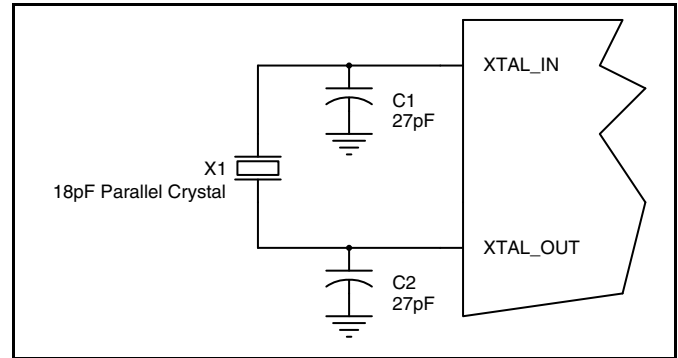


**Output Duty Cycle/Pulse Width/Period**

## Applications Information

### Crystal Input Interface

The 83918 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

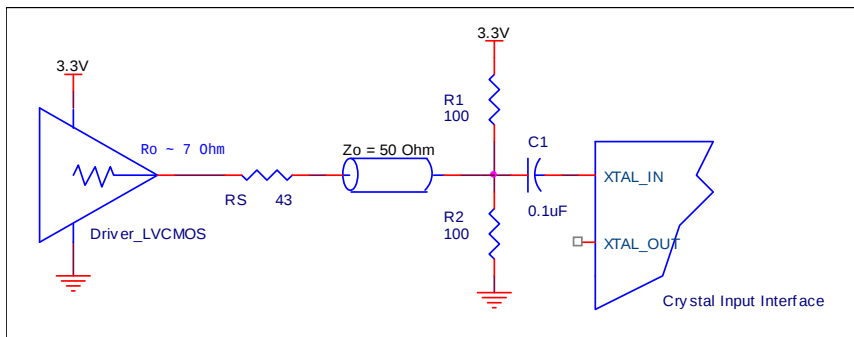


**Figure 1. Crystal Input Interface**

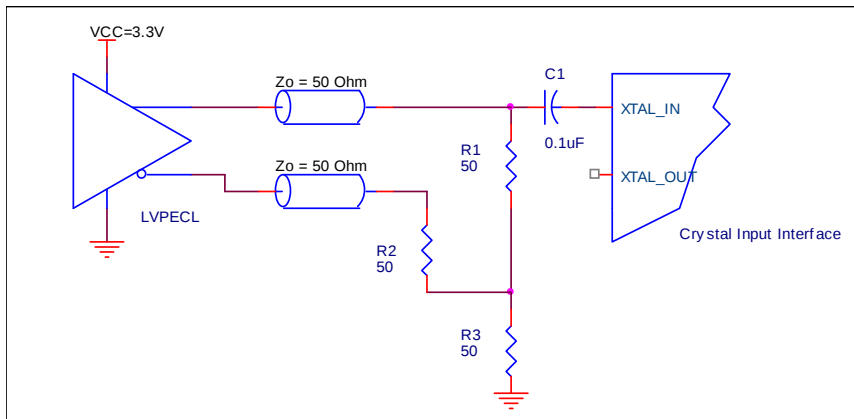
### Overdriving the XTAL Interface

The XTAL\_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 2A*. The XTAL\_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition,

matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.



**Figure 2A. General Diagram for LVCMOS Driver to XTAL Input Interface**



**Figure 2B. General Diagram for LVPECL Driver to XTAL Input Interface**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from XTAL\_IN to ground.

#### LVC MOS\_CLK Input

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from the LVC MOS\_CLK to ground.

#### LVC MOS Control Pin

The control pin has an internal pulldown; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

### Outputs:

#### LVC MOS Outputs

All unused LVC MOS outputs can be left floating. We recommend that there is no trace attached.

## Power Considerations

This section provides information on power dissipation and junction temperature for the 83918. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 83918 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD} + I_{DDO}) = 3.465V * (24mA + 27mA) = \mathbf{176.7mW}$

### Dynamic Power Dissipation at 200MHz

$$\text{Power (200MHz)} = C_{PD} * \text{Frequency} * (V_{DD})^2 * \text{number of outputs} = 9pF * 200MHz * (3.465V)^2 * 18 = \mathbf{389mW}$$

### Total Power Dissipation

- Total Power**  
= Power (core)<sub>MAX</sub> + Power (200MHz)  
= 176.7mW + 389mW  
= **565.7mW**

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd_{total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd_{total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 53.5°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.566W * 53.5^\circ\text{C/W} = 115.3^\circ\text{C}. \text{ This is well below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 6. Thermal Resistance  $\theta_{JA}$  for 32 Lead LQFP, Forced Convection**

| $\theta_{JA}$ by Velocity                   |          |          |          |
|---------------------------------------------|----------|----------|----------|
| Meters per Second                           | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards | 53.5°C/W | 48.0°C/W | 44.0°C/W |

## Reliability Information

**Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 32 Lead LQFP**

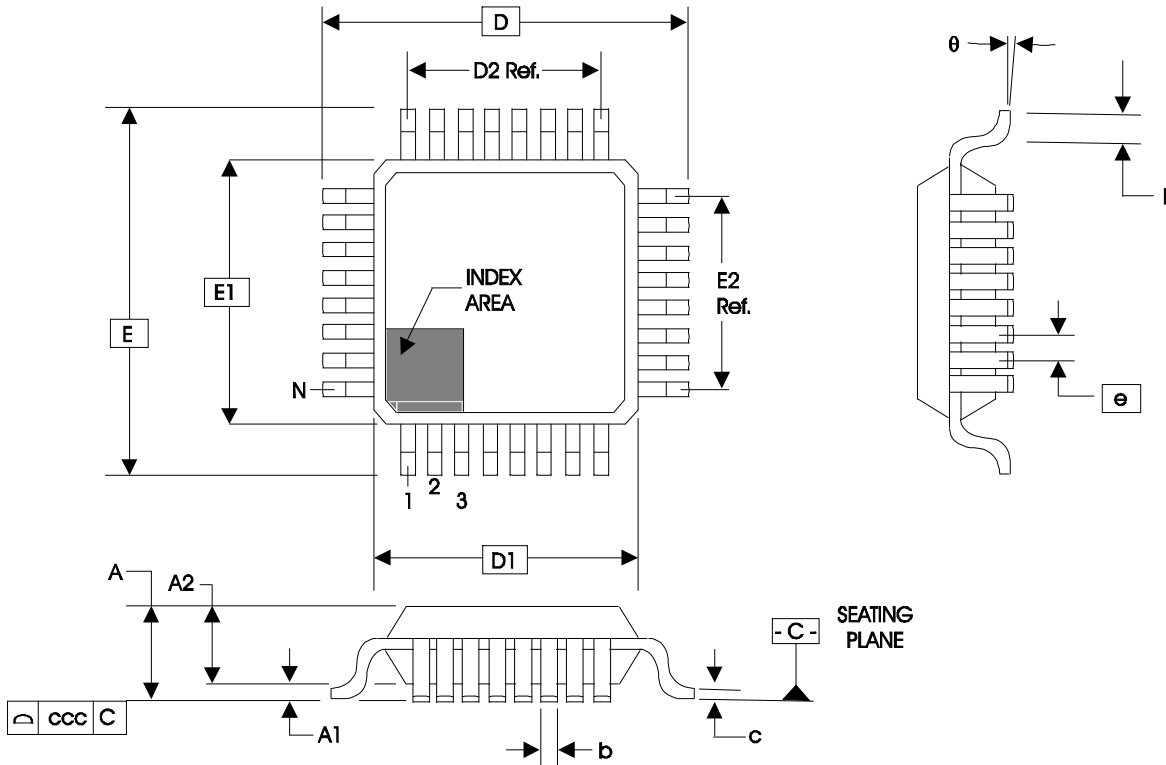
| $\theta_{JA}$ vs. Air Flow                  |          |          |          |
|---------------------------------------------|----------|----------|----------|
| Meters per Second                           | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards | 53.5°C/W | 48.0°C/W | 44.0°C/W |

## Transistor Count

The transistor count for 83918 is: 909

## Package Outline and Package Dimensions

### Package Outline - Y Suffix for 32 Lead LQFP



**Table 8. Package Dimensions for 32 Lead LQFP**

| JEDEC Variation: BBC - HD<br>All Dimensions in Millimeters |            |         |         |
|------------------------------------------------------------|------------|---------|---------|
| Symbol                                                     | Minimum    | Nominal | Maximum |
| N                                                          | 32         |         |         |
| A                                                          |            |         | 1.60    |
| A1                                                         | 0.05       | 0.10    | 0.15    |
| A2                                                         | 1.35       | 1.40    | 1.45    |
| b                                                          | 0.30       | 0.37    | 0.45    |
| c                                                          | 0.09       |         | 0.20    |
| D & E                                                      | 9.00 Basic |         |         |
| D1 & E1                                                    | 7.00 Basic |         |         |
| D2 & E2                                                    | 5.60 Ref.  |         |         |
| e                                                          | 0.80 Basic |         |         |
| L                                                          | 0.45       | 0.60    | 0.75    |
| θ                                                          | 0°         |         | 7°      |
| ccc                                                        |            |         | 0.10    |

Reference Document: JEDEC Publication 95, MS-026

## Ordering Information

Table 9. Ordering Information

| Part/Order Number | Marking      | Package                  | Shipping Packaging | Temperature   |
|-------------------|--------------|--------------------------|--------------------|---------------|
| 83918AYILF        | ICS83918AYIL | "Lead-Free" 32 Lead LQFP | Tray               | -40°C to 85°C |
| 83918AYILFT       | ICS83918AYIL | "Lead-Free" 32 Lead LQFP | Tape & Reel        | -40°C to 85°C |

## Revision History Sheet

| Rev | Table                     | Page       | Description of Change                                                                                                                                            | Date    |
|-----|---------------------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| B   | T5A, T5B, T5D, T5E<br>T5D | 5 - 7<br>7 | AC Characteristic Tables - added Test Conditions to Output Duty Cycle.<br>2.5 AC Characteristics Table - changed Part-to-Part skew from 1.1ns max to 1.0 ns max. | 8/17/10 |
| B   | T9                        | 17         | Ordering Information - Removed leaded devices.<br>Updated data sheet format.                                                                                     | 3/25/15 |
| B   | T9                        | 17         | Ordering Information - Deleted LF note below table.<br>Updated header and footer.                                                                                | 3/17/16 |

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