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Jameco Part Number 1614856

FEATURES

- Two LVCMOS/LVTTL outputs @ 3.3V, 17Ω typical output impedance
 - Selectable crystal oscillator interface or LVCMOS single-ended input
 - Supports the following output frequencies: 156.25MHz, 125MHz and 62.5MHz
 - Output frequency range: 56MHz - 175MHz
 - VCO range: 560MHz - 700MHz
 - Output skew: 12ps (maximum)
 - RMS phase jitter at 156.25MHz (1.875MHz - 20MHz): 0.47ps (typical)
- | <u>Offset</u> | <u>Noise Power</u> |
|---------------|--------------------|
| 100Hz | -97.4 dBc/Hz |
| 1kHz | -120.2 dBc/Hz |
| 10kHz | -127.6 dBc/Hz |
| 100kHz | -126.1 dBc/Hz |
- Power supply modes:
Core/Output
3.3V/3.3V
3.3V/2.5V
2.5V/2.5V
 - -40°C to 85°C ambient operating temperature
 - Available in both standard (RoHS 5) and lead-free RoHS (6) packages

Offset	Noise Power
100Hz	-97.4 dBc/Hz
1kHz	-120.2 dBc/Hz
10kHz	-127.6 dBc/Hz
100kHz	-126.1 dBc/Hz

Inputs				Output Frequency (25MHz Ref.)
F_SEL1	F_SEL0	M Divider Value	N Divider Value	
0	0	25	4	156.25
0	1	25	5	125
1	0	25	10	62.5
1	1	25	5	125

The diagram illustrates the PLL and Frequency Divider circuit. It includes the following components and connections:

- Inputs:**
 - OE:** Pullup
 - F_SEL1:0:** Pullup:Pullup (with a break symbol)
 - nPLL_SEL:** Pulldown
 - nXTAL_SEL:** Pulldown
 - XTAL_IN:** Connected to a 25MHz crystal oscillator (OSC).
 - XTAL_OUT:** Connected to the OSC.
 - TEST_CLK:** Pulldown
 - MR:** Pulldown
- Internal Blocks:**
 - Multiplexer 1:** Selects between XTAL_IN (input 0) and TEST_CLK (input 1) based on nXTAL_SEL.
 - Phase Detector:** Receives the selected input and the output of the VCO.
 - VCO (Voltage-Controlled Oscillator):** Receives the output of the Phase Detector and the output of the M divider.
 - M Divider:** A fixed divider with M = 25.
 - Multiplexer 2:** Selects between the output of the VCO (input 1) and the output of the M divider (input 0) based on F_SEL1:0.
 - F Divider:** A frequency divider that takes the output of Multiplexer 2 and divides it by N, where N is determined by F_SEL1:0.
- Outputs:**
 - Q0:** The output of the F divider for N = 4.
 - Q1:** The output of the F divider for N = 5.
- F Divider Table:**

F_SEL1:0	N
00	÷4
01	÷5
10	÷10
11	÷5

F_SEL0	1	16	F_SEL1
nXTAL_SEL	2	15	GND
TEST_CLK	3	14	GND
OE	4	13	Q0
MR	5	12	Q1
nPLL_SEL	6	11	V _{DDO}
V _{DDA}	7	10	XTAL_IN
V _{DD}	8	9	XTAL_OUT

ICS840002I-01

16-Lead TSSOP

4.4mm x 5.0mm x 0.92mm
package body

G Package

Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 16	F_SELO, F_SEL1	Input	Pullup	Frequency select pin. LVC MOS/LVTTL interface levels.
2	nXTAL_SEL	Input	Pulldown	Selects between the crystal or TEST_CLK inputs as the PLL reference source. When HIGH, selects TEST_CLK. When LOW, selects XTAL input. LVC MOS/LVTTL interface levels.
3	TEST_CLK	Input	Pulldown	Single-ended LVC MOS/LVTTL clock input.
4	OE	Input	Pullup	Output enable pin. When HIGH, the outputs are active. When LOW, the outputs are in a high impedance state. LVC MOS/LVTTL interface levels.
5	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing active outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVC MOS/LVTTL interface levels.
6	nPLL_SEL	Input	Pulldown	PLL Bypass. When LOW, the output is driven from the VCO output. When HIGH, the PLL is bypassed and the output frequency = reference clock frequency/N output divider. LVC MOS/LVTTL interface levels.
7	V _{DDA}	Power		Analog supply pin.
8	V _{DD}	Power		Core supply pin.
9, 10	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface.
11	V _{DDO}	Power		Output supply pin.
12, 13	Q1, Q0	Output		Single-ended clock outputs. LVC MOS/LVTTL interface levels.
14, 15	GND	Power		Power supply ground.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
C _{PD}	Power Dissipation Capacitance			8		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ
R _{OUT}	Output Impedance	3.3V±5%	14	17	21	Ω
		2.5V±5%	16	21	25	Ω

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, V_O	-0.5V to $V_{DD} + 0.5V$
Package Thermal Impedance, θ_{JA}	89°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{DD}	Power Supply Current				100	mA
I_{DDA}	Analog Supply Current				12	mA
I_{DDO}	Output Supply Current				5	mA

TABLE 3B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				95	mA
I_{DDA}	Analog Supply Current				12	mA
I_{DDO}	Output Supply Current				5	mA

TABLE 3C. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, OR $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		$V_{DD} = 3.3V$	2		$V_{DD} + 0.3$	V
			$V_{DD} = 2.5V$	1.7		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		$V_{DD} = 3.3V$	-0.3		0.8	V
			$V_{DD} = 2.5V$	-0.3		0.7	V
I_{IH}	Input High Current	OE, F_SEL0, F_SEL1	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			5	μA
		nPLL_SEL, MR, nXTAL_SEL, TEST_CLK	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			150	μA
I_{IL}	Input Low Current	OE, F_SEL0, F_SEL1	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150			μA
		nPLL_SEL, MR, nXTAL_SEL, TEST_CLK	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5			μA
V_{OH}	Output High Voltage; NOTE 1		$V_{DDO} = 3.3V \pm 5\%$	2.6			V
			$V_{DDO} = 2.5V \pm 5\%$	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		$V_{DDO} = 3.3V$ or $2.5V \pm 5\%$			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information, Output Load Test Circuit.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00	140		175	MHz
		F_SEL[1:0] = 01	112		140	MHz
		F_SEL[1:0] = 10 or 11	56		70	MHz
$t_{sk(o)}$	Output Skew; NOTE 1, 3				12	ps
$f_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 2	156.25MHz (1.875MHz - 20MHz)		0.47		ps
		125MHz (1.875MHz - 20MHz)		0.57		ps
		62.5MHz (1.875MHz - 20MHz)		0.51		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		46		54	%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.

Measured at $V_{DDO}/2$.

NOTE 2: Please refer to the Phase Noise Plot.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00	140		175	MHz
		F_SEL[1:0] = 01	112		140	MHz
		F_SEL[1:0] = 10 or 11	56		68	MHz
tsk(o)	Output Skew; NOTE 1, 3				12	ps
fjit($\emptyset$)	RMS Phase Jitter (Random); NOTE 2	156.25MHz (1.875MHz - 20MHz)		0.47		ps
		125MHz (1.875MHz - 20MHz)		0.55		ps
		62.5MHz (1.875MHz - 20MHz)		0.49		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		46		54	%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.

Measured at $V_{DDO}/2$.

NOTE 2: Please refer to the Phase Noise Plot.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5C. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00	140		175	MHz
		F_SEL[1:0] = 01	112		140	MHz
		F_SEL[1:0] = 10 or 11	56		68	MHz
tsk(o)	Output Skew; NOTE 1, 3				12	ps
fjit($\emptyset$)	RMS Phase Jitter (Random); NOTE 2	156.25MHz (1.875MHz - 20MHz)		0.49		ps
		125MHz (1.875MHz - 20MHz)		0.56		ps
		62.5MHz (1.875MHz - 20MHz)		0.52		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		46		54	%

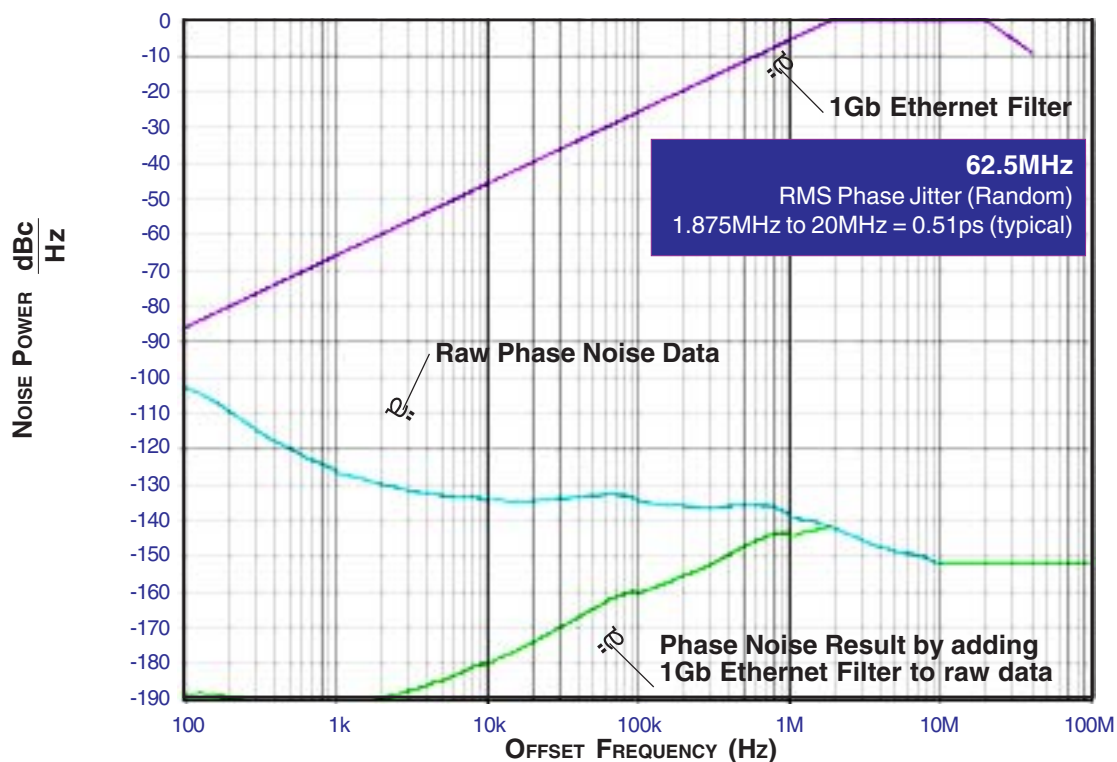
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.

Measured at $V_{DDO}/2$.

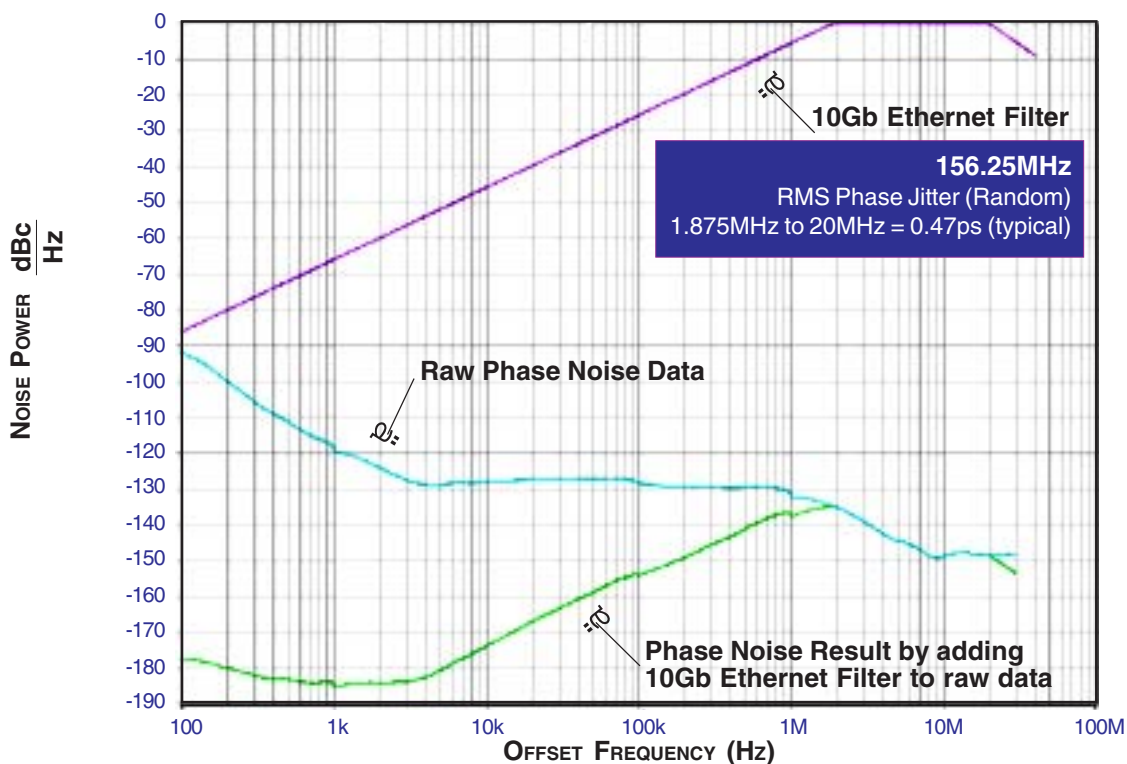
NOTE 2: Please refer to the Phase Noise Plot.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TYPICAL PHASE NOISE AT 62.5MHz @3.3V



TYPICAL PHASE NOISE AT 156.25MHz @3.3V



1.65V $\pm$ 5%

V_{DD} , V_{DDA} , V_{DDO}

LVC MOS

GND

-1.65V $\pm$ 5%

$Z = 50\Omega$

Qx

SCOPE

50 Ω

Phase Noise Plot

Phase Noise Mask

Offset Frequency

f_1

f_2

RMS Jitter = $\sqrt{\text{Area Under the Masked Phase Noise Plot}}$

The diagram shows a clock signal (Clock) and two data outputs (Outputs). The clock signal is a square wave. The data outputs are shown as two trapezoidal pulses. The first output pulse has a rising edge that reaches 80% of its maximum value at a time t_R after the clock edge. The second output pulse has a falling edge that reaches 80% of its maximum value at a time t_F after the clock edge. The setup time t_{SU} is the time interval between the clock edge and the output reaching 80% of its maximum value. The hold time t_{HD} is the time interval between the output reaching 80% of its maximum value and the next clock edge.

Q0, Q1

Pulse Width

$\frac{V_{DDO}}{2}$

t PERIOD

$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

840002AGI-01

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS840002I-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} , V_{DDA} , and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10μF and a .01μF bypass capacitor should be connected to each V_{DDA} .

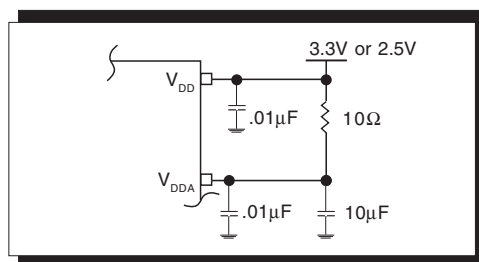


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS840002I-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2*

below were determined using a 25MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

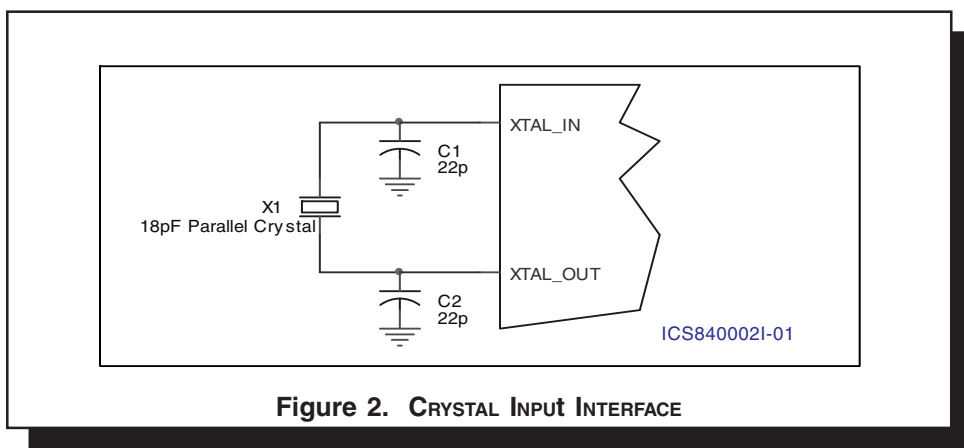


Figure 2. CRYSTAL INPUT INTERFACE

LAYOUT GUIDELINE

Figure 3 shows a schematic example of the ICS840002I-01. An example of LVCMOS termination is shown in this schematic. Additional LVCMOS termination approaches are shown in the LVCMOS Termination Application Note. In this example, an 18 pF parallel resonant 25MHz crystal is used. The C1=22pF and

C2=22pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. 1K Ω pullup or pulldown resistors can be used for the logic control input pins.

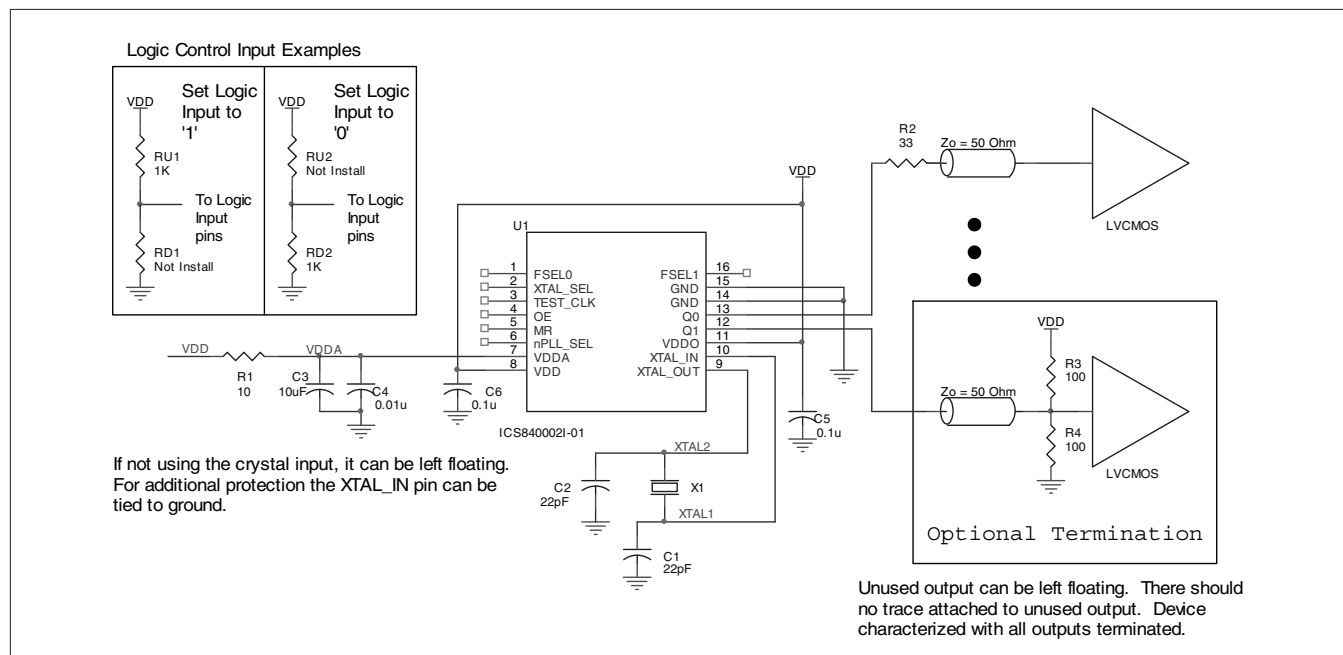


FIGURE 3. ICS840002I-01 SCHEMATIC EXAMPLE

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

TRANSISTOR COUNT

The transistor count for ICS840002I-01 is: 3356

PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

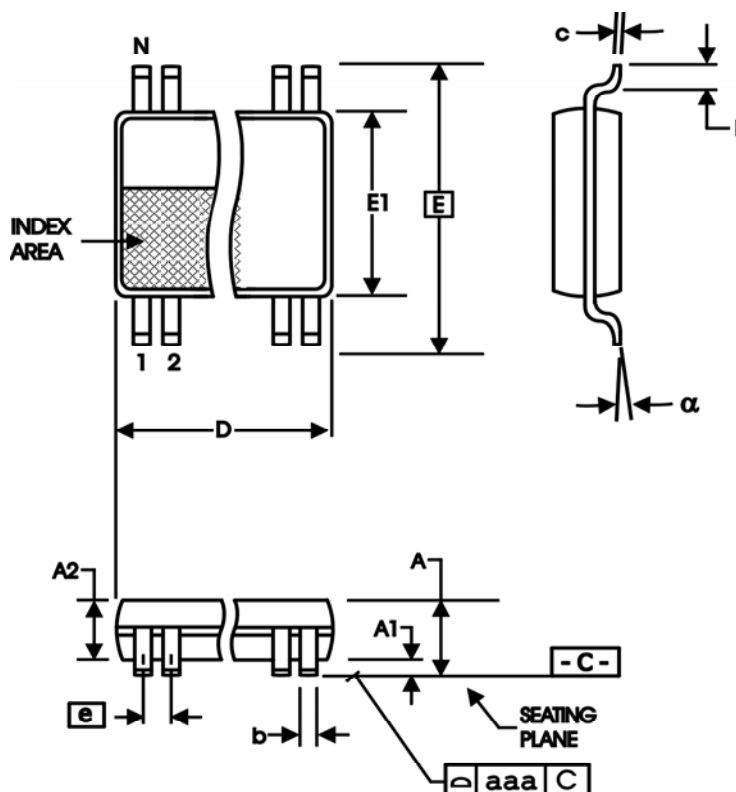


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS840002AGI-01	ICS840002AI01	16 Lead TSSOP	tube	-40°C to 85°C
ICS840002AGI-01T	ICS840002AI01	16 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS840002AGI-01LF	002AI01L	16 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS840002AGI-01LFT	002AI01L	16 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
A	T8	12	Ordering Information Table - Added Lead-Free part number, marking and note.	10/18/07