FemtoClock® Crystal-to-3.3V, 2.5V LVPECL Clock Generator

843022I-02

PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES NOVEMBER 2, 2016 **DATA SHEET**

General Description

The 843022I-02 is a Gigabit Ethernet Clock Generator. The 843022I-02 uses a 25MHz crystal to synthesize 125MHz or 62.5MHz. The 843022I-02 has excellent phase jitter performance, over the 12kHz – 20MHz integration range. The 843022I-02 is packaged in a small 16-pin VFQFN, making it ideal for use in systems with limited board space.

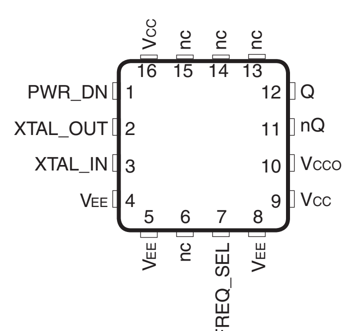
Features

- One differential 3.3V or 2.5V LVPECL output
- Crystal oscillator interface designed for 25MHz, 18pF parallel resonant crystal
- Output frequencies: 125MHz or 62.5MHz (selectable)
- RMS phase jitter @ 125MHz, using a 25MHz crystal (12kHz - 20MHz): 0.57ps (typical)
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) packaging
- For functional replacement part use 8T49N241

Function Table

Inputs	Output Frequencies (with a 25MHz crystal)
FREQ_SEL	
0	125MHz
1	62.5MHz

Pin Assignment



843022I-02
16-Lead VFQFN
3mm x 3mm x 0.925 package body
K Package
Top View

Block Diagram

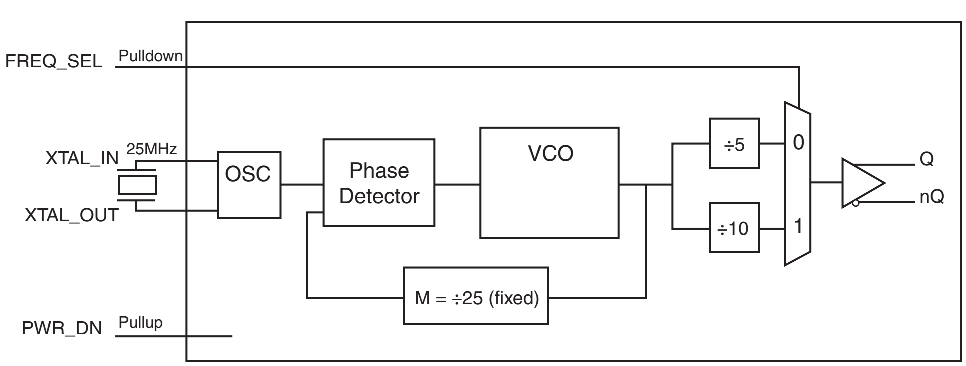


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TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	PWR_DN	Input	Pullup	Output state control pin. See Table 3. LVCMOS/LVTTL interface levels.
2, 3	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_in is the input, XTAL_OUT is the output.
4, 5, 8	V_{EE}	Power		Negative supply pins.
6, 13, 14, 15	nc	Unused		No connect.
7	FREQ_SEL	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
9, 16	V_{CC}	Power		Power supply pins.
10	V_{CCO}	Power		Output supply pin.
11, 12	nQ, Q	Output		Differential clock outputs. LVPECL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

TABLE 3. PWR_DN FUNCTION TABLE

PWR_DWN Input	Description
0	Output in high impedance
1	Output in normal operation

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	74.9°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCO}$ = 3.3V±5%, V_{EE} = 0V, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current	PWR_DN = 1			86	mA
		PWR_DN = 0			<1	mA

Table 4B. Power Supply DC Characteristics, $V_{CC} = V_{CCO}$ = 2.5V±5%, V_{EE} = 0V, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	2.5	2.625	V
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current	PWR_DN = 1			77	mA
		PWR_DN = 0			<1	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCO}$ = 3.3V±5% or 2.5V±5%, V_{EE} = 0V, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.465V	2		V_{CC} + 0.3	V
			V_{CC} = 2.625V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.465V	-0.3		0.8	V
			V_{CC} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	FREQ_SEL	$V_{CC} = V_{IN}$ = 3.465V or 2.625V			150	µA
		PWR_DN	$V_{CC} = V_{IN}$ = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	FREQ_SEL	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		PWR_DN	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA

TABLE 4D. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCO}$ = 3.3V±5% OR 2.5V±5%, V_{EE} = 0V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: It is not recommended to overdrive the crystal input with an external clock.

TABLE 6A. AC CHARACTERISTICS, $V_{CC} = V_{CCO}$ = 3.3V±5%, V_{EE} = 0V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL = 0		125		MHz
		F_SEL = 1		62.5		MHz
tjit(Ø)	RMS Phase Jitter; NOTE 1	125MHz, Integration Range: 12kHz - 20MHz		0.57		ps
		62.5MHz, Integration Range: 12kHz - 10MHz		0.52		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		47		53	%

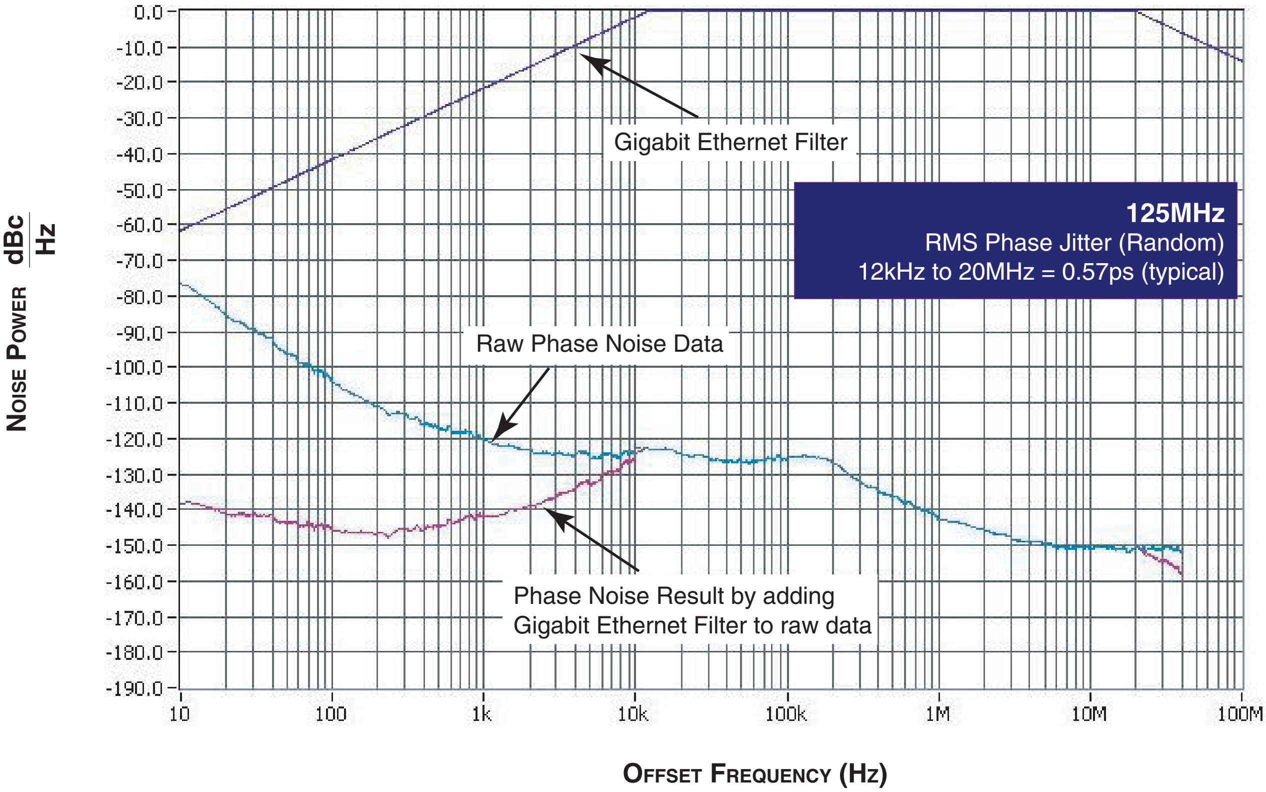
NOTE 1: Please refer to the Phase Noise Plot.

TABLE 6B. AC CHARACTERISTICS, $V_{CC} = V_{CCO}$ = 2.5V±5%, V_{EE} = 0V, TA = -40°C TO 85°C

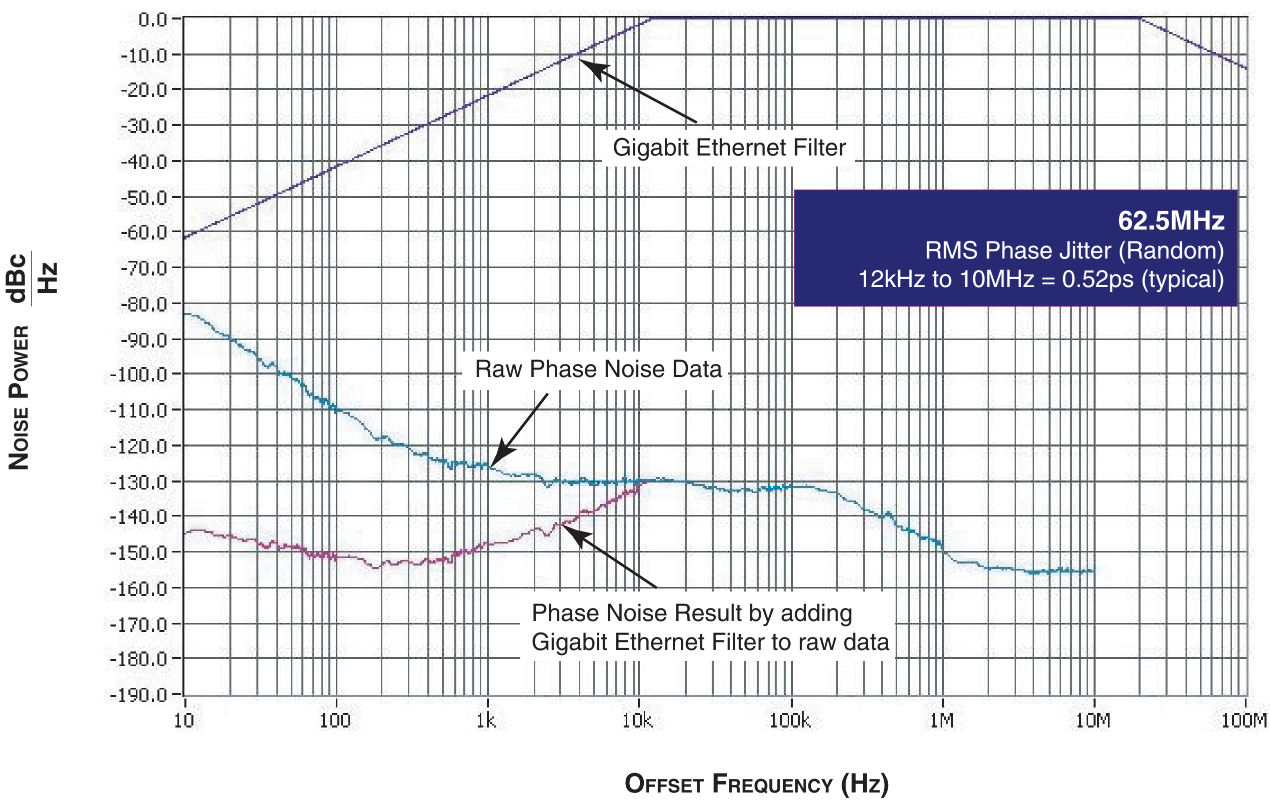
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL = 0		125		MHz
		F_SEL = 1		62.5		MHz
tjit(Ø)	RMS Phase Jitter; NOTE 1	125MHz, Integration Range: 12kHz - 20MHz		0.62		ps
		62.5MHz, Integration Range: 12kHz - 10MHz		0.60		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		47		53	%

NOTE 1: Please refer to the Phase Noise Plot.

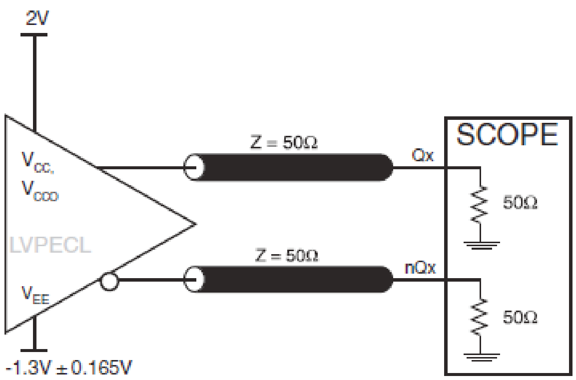
Typical Phase Noise at 125MHz (3.3V)



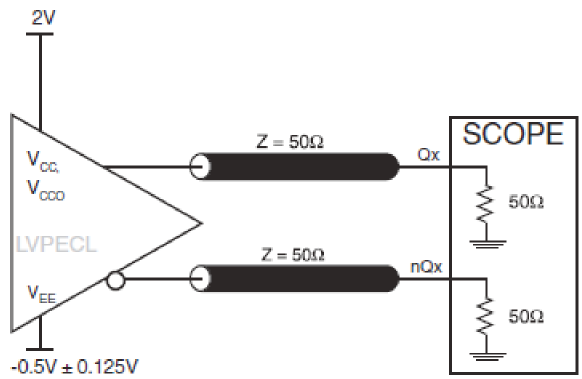
Typical Phase Noise at 62.5MHz (3.3V)



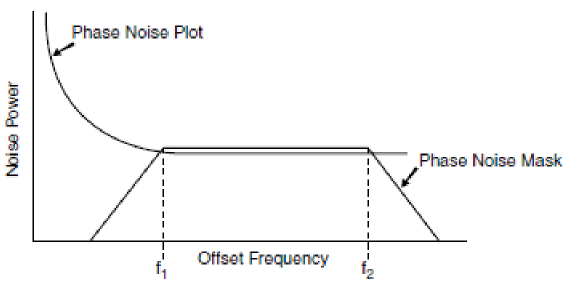
Parameter Measurement Information



3.3V Output Load AC Test Circuit

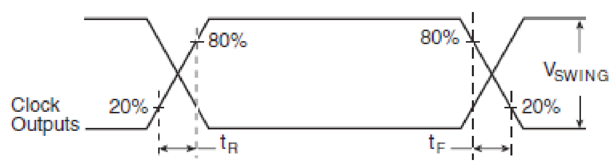


2.5V Output Load AC Test Circuit

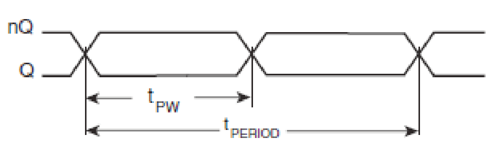


RMS Jitter = $\sqrt{\text{Area Under the Masked Phase Noise Plot}}$

RMS Phase Jitter



Output Rise/Fall Time



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Output Duty Cycle/Pulse Width/Period

Application Information

Crystal Input Interface

The 843022I-02 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

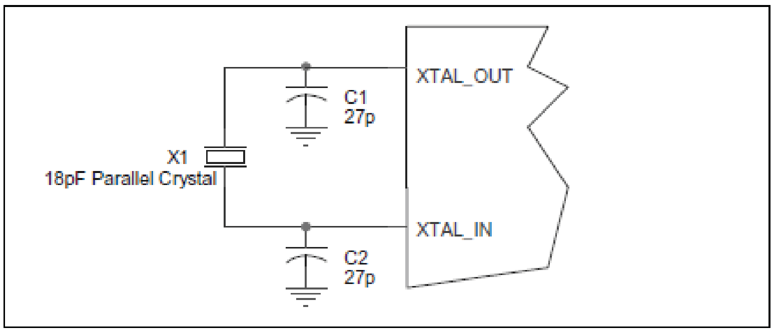


Figure 1. Crystal Input Interface

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

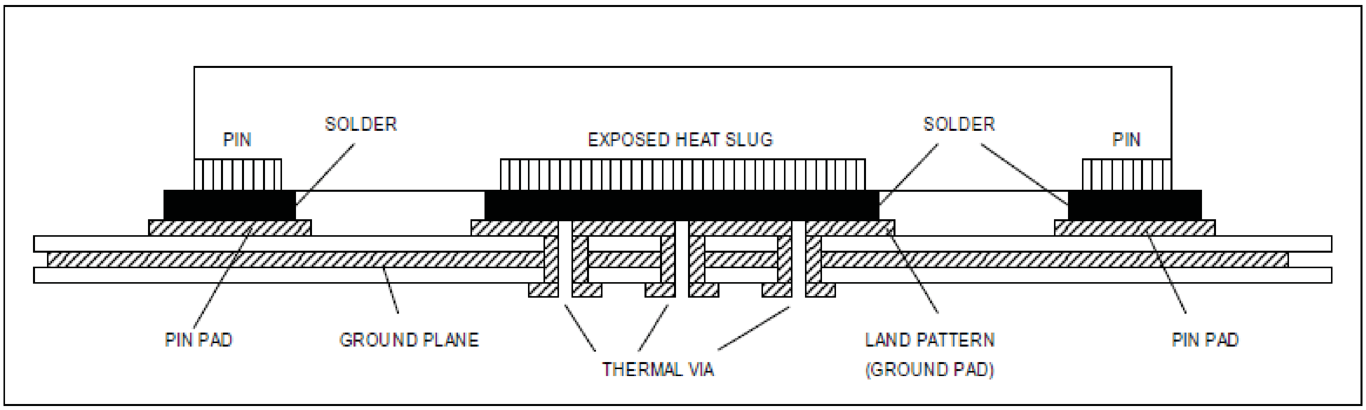


Figure 3. P.C.Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is typical for IA64/32 platforms. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

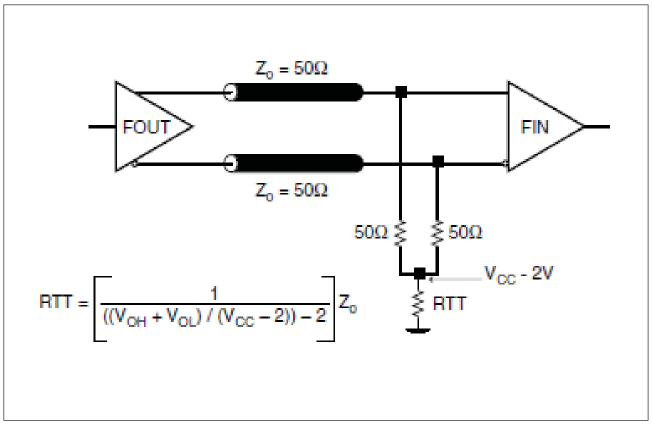


Figure 4A. LVPECL Output Termination

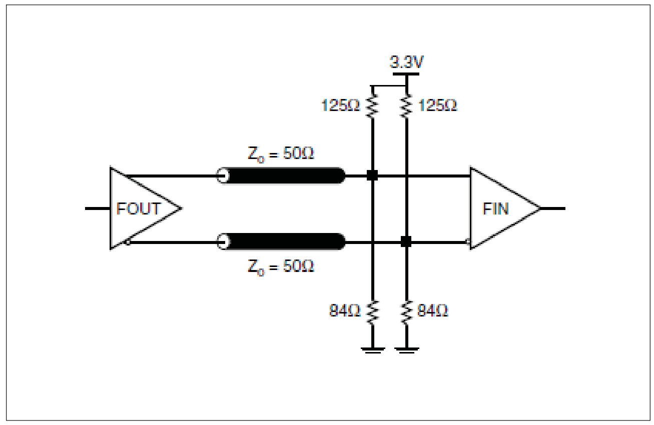


Figure 4B. LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

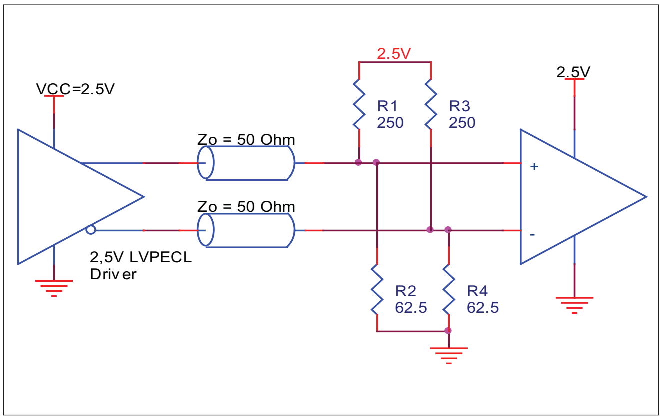


Figure 5A. 2.5V LVPECL Driver Termination Example

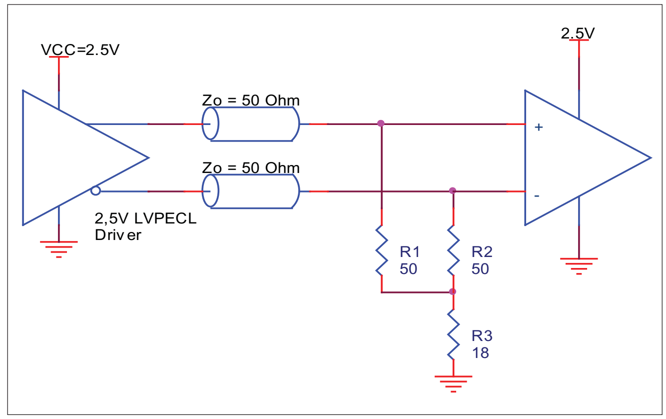


Figure 5B. 2.5V LVPECL Driver Termination Example

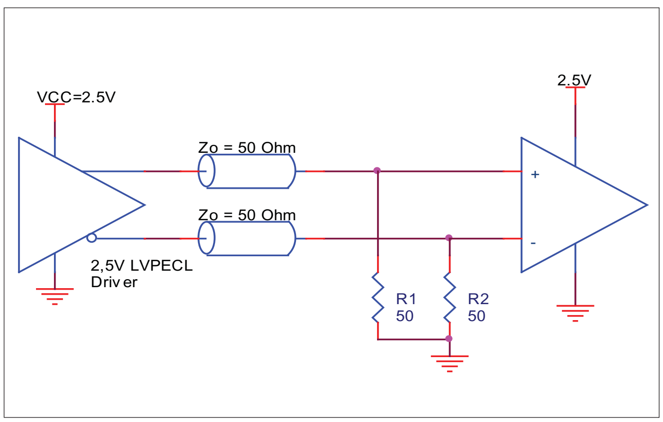


Figure 5C. 2.5V LVPECL Termination Example

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 843022I-02. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 843022I-02 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 86mA = **298mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**

Total Power $_{\_MAX}$ (3.465V, with all outputs switching) = 298mW + 30mW = **328mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.9°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.328W * 74.9°C/W = 109.6°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 16-PIN VFQFN, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.9°C/W	65.5°C/W	58.8°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6.*

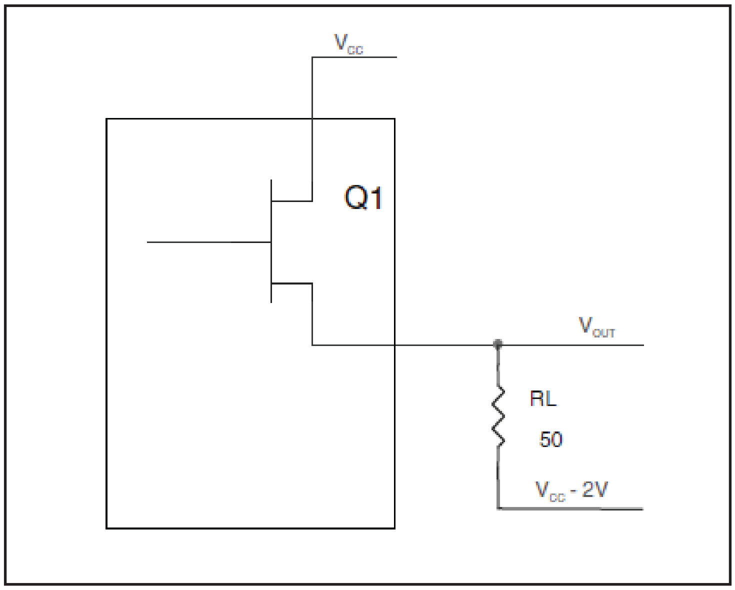


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

Pd_H = $[(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

Pd_L = $[(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for 16 Lead VFQFN

θ_{JA} at 0 Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.9°C/W	65.5°C/W	58.8°C/W

Transistor Count

The transistor count for 843022I-02 is: 1719

Package Outline - K Suffix for 16 Lead VFQFN

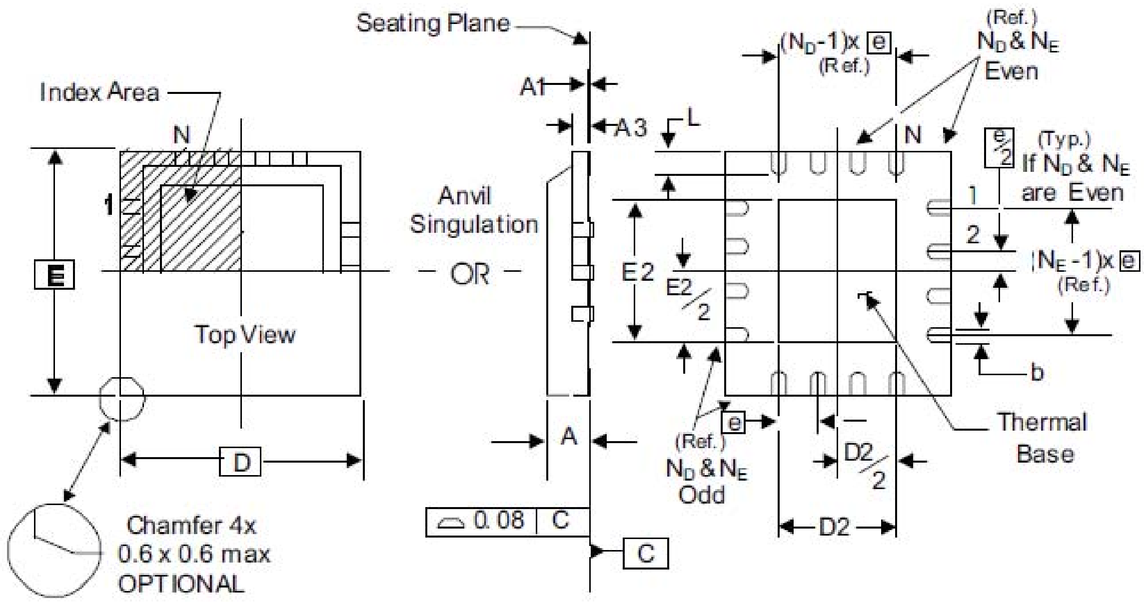


Table 9. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	16	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	4	
N_E	4	
D	3.0	
D2	1.0	1.80
E	3.0	
E2	1.0	1.80
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843022AKI-02LF	3I2L	16 Lead "Lead-Free" VFQFN	Tube	-40°C to 85°C
843022AKI-02LFT	3I2L	16 Lead "Lead-Free" VFQFN	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	 T10	8 15	Updated *Thermal Release Path* section. Ordering Information Table - corrected marking from 312L to 3I2L.	2/20/08
A	 T5 T7	1 4 7 12	Deleted HiPerClockS references. Crystal Characteristics Table - added note. Deleted application note, LVCMOS to XTAL Interface. Deleted quantity from tape and reel.	10/22/12
A		1	Product Discontinuation Notice - Last time buy expires November 2, 2016. PDN# CQ-15-05. Updated data sheet format.	11/4/15

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