FemtoClock™ Crystal-to-LVDS 150MHz Clock Generator

DATA SHEET

General Description

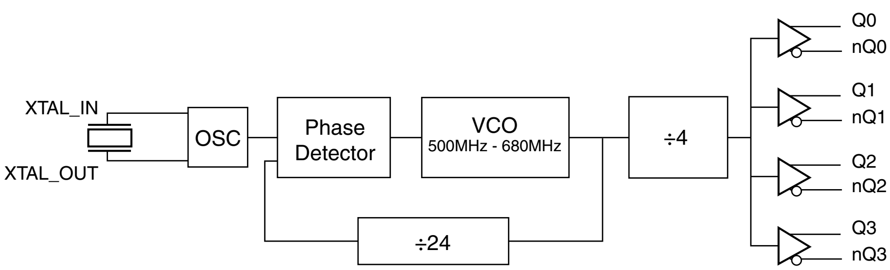
ICS HiPerClockS™

The ICS844244I-04 is a Serial ATA (SATA)/Serial Attached SCSI (SAS) Clock Generator. For SATA/SAS applications, a 25MHz crystal is used to produce 150MHz. The ICS844244I-04 has excellent <1ps phase jitter performance, over the 12kHz - 20MHz integration range. The ICS844244I-04 is packaged in a small 16-pin TSSOP, making it ideal for use in systems with limited board space.

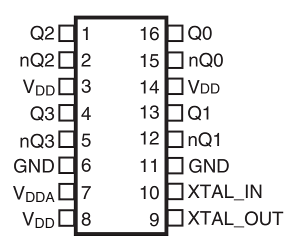
Features

- Four differential LVDS output pairs
- Crystal oscillator interface, 18pF parallel resonant crystal (20.833MHz – 28.3MHz)
- Output frequency range: 125MHz – 170MHz
- VCO range: 500MHz – 680MHz
- RMS phase jitter at 150MHz, using a 25MHz crystal (12kHz – 20MHz): 0.9ps (typical) @ 3.3V
- Full 3.3V or 2.5V output supply modes
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS844244I-04
16 Lead TSSOP
4.4mm x 5.0mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type	Description
1, 2	Q2, nQ2	Output	Differential clock output pair. LVDS interface levels.
3, 8, 14	V_{DD}	Power	Core supply pins.
4, 5	Q3, nQ3	Output	Differential clock output pair. LVDS interface levels.
6, 11	GND	Power	Power supply ground.
7	V_{DDA}	Power	Analog supply pin.
9, 10	XTAL_OUT, XTAL_IN	Input	Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
12, 13	nQ1, Q1	Output	Differential clock output pair. LVDS interface levels.
15, 16	nQ0, Q0	Output	Differential clock output pair. LVDS interface levels.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, I_O Continuos Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	92.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 2A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.10	3.3	V_{DD}	V
I_{DD}	Power Supply Current				121	mA
I_{DDA}	Analog Supply Current				10	mA

Table 2B. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.10	2.5	V_{DD}	V
I_{DD}	Power Supply Current				115	mA
I_{DDA}	Analog Supply Current				10	mA

Table 2C. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	V_{DD} = 3.3V ± 5%	2		V_{DD} + 0.3	V
		V_{DD} = 2.5V ± 5%	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	V_{DD} = 3.3V ± 5%	-0.3		0.8	V
		V_{DD} = 2.5V ± 5%	-0.3		0.7	V

Table 2D. LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		240		460	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.17		1.52	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 2E. LVDS DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		240		460	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.10		1.40	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 3. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		20.833	25	28.3	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

AC Electrical Characteristics

Table 4A. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		125	150	170	MHz
*t*jit(Ø)	RMS Phase Jitter, Random; NOTE 1	150MHz, Integration Range: 12kHz – 20MHz		0.9		ps
*t*sk(o)	Output Skew; NOTE 2, 3				65	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		650	ps
odc	Output Duty Cycle		48		52	%

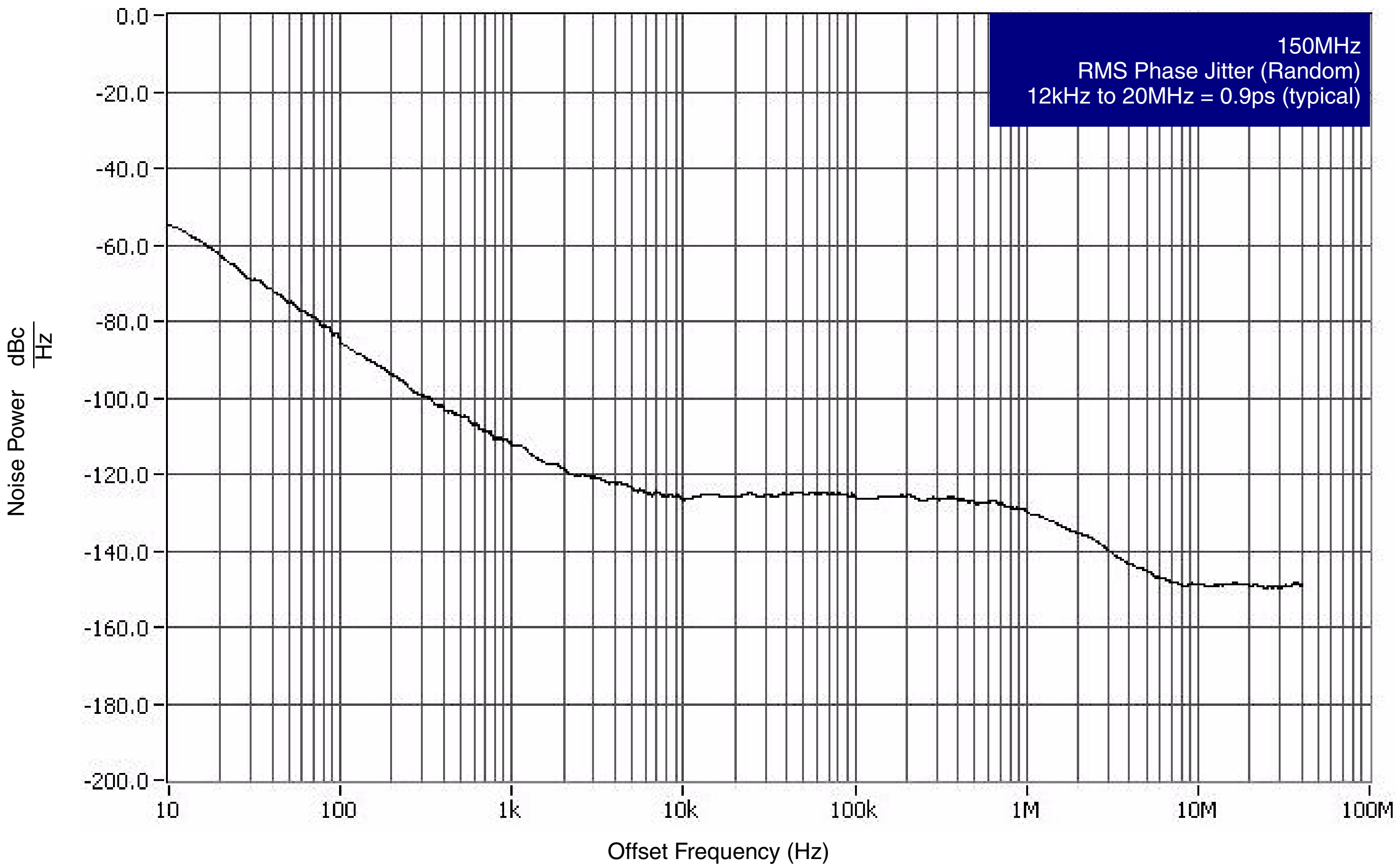
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using a 25MHz crystal, f_{OUT} @ 150MHz.
NOTE 1: Refer to Phase Noise Plots.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

Table 4B. AC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°

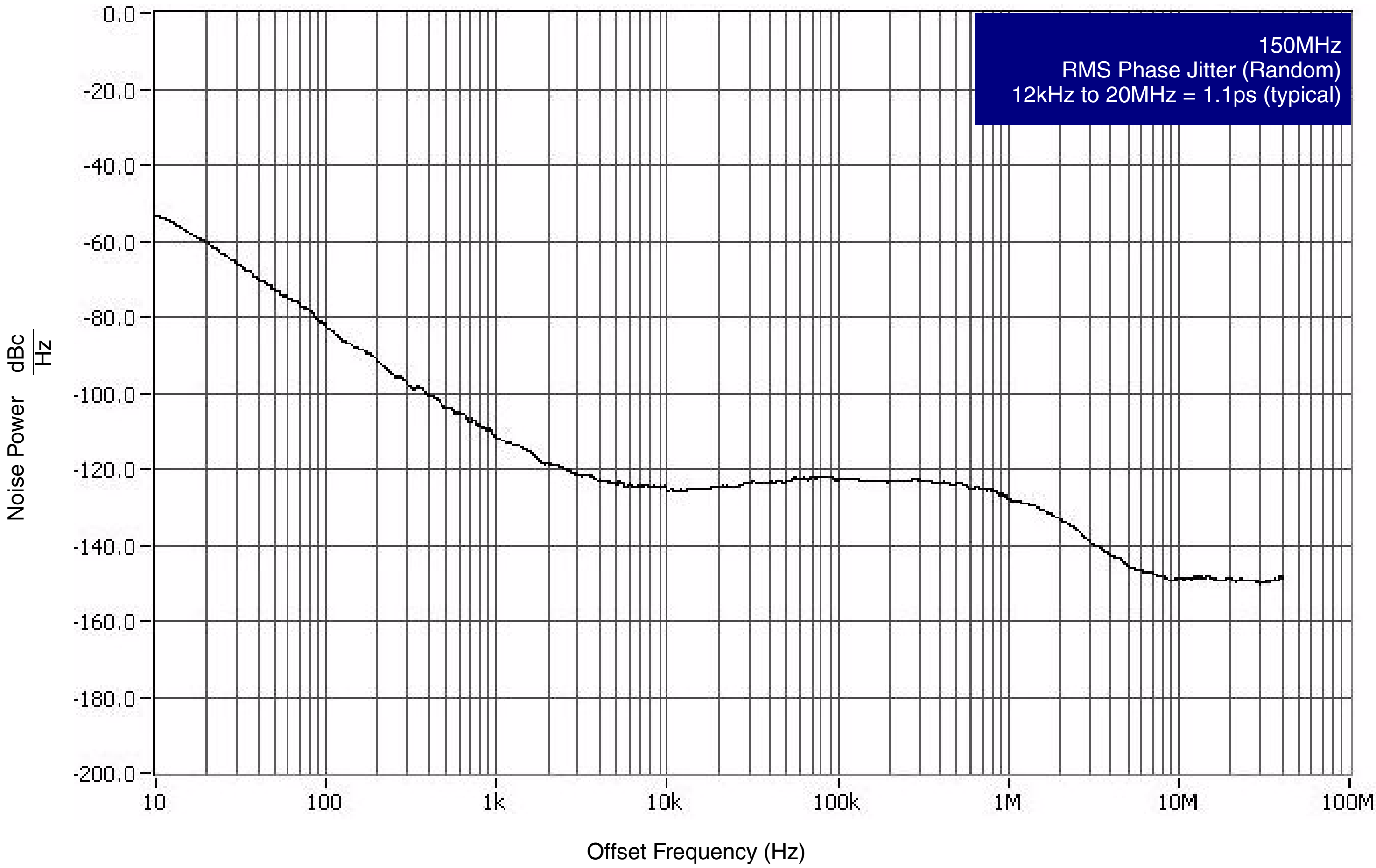
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		125	150	170	MHz
*t*jit(Ø)	RMS Phase Jitter, Random; NOTE 1	150MHz, Integration Range: 12kHz – 20MHz		1.1		ps
*t*sk(o)	Output Skew; NOTE 2, 3				65	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		650	ps
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using a 25MHz crystal, f_{OUT} @ 150MHz.
NOTE 1: Refer to Phase Noise Plots.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

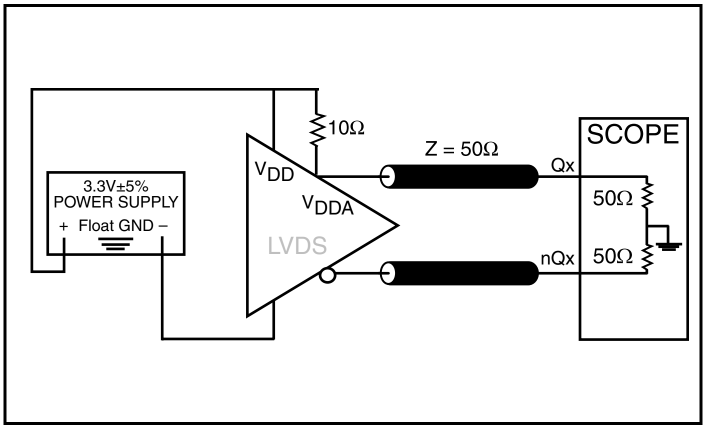
Typical Phase Noise at 150MHz (3.3V)



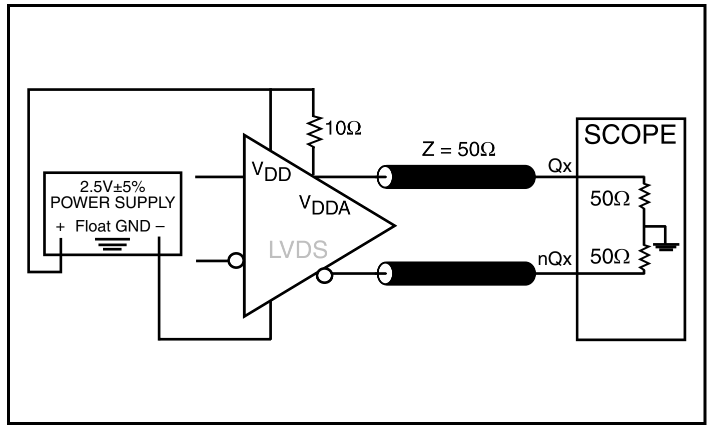
Typical Phase Noise at 150MHz (2.5V)



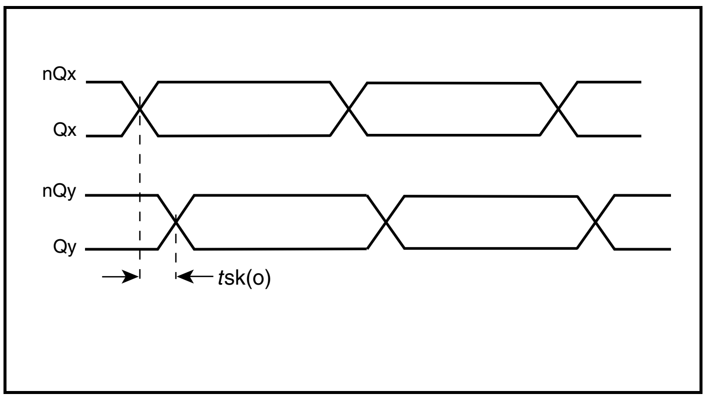
Parameter Measurement Information



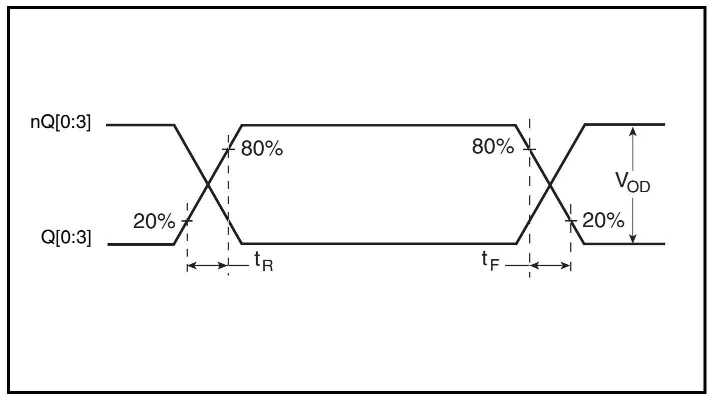
3.3V LVDS Output Load AC Test Circuit



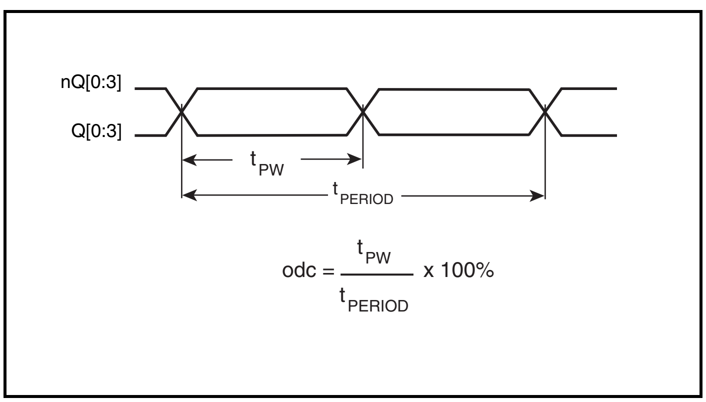
2.5V LVDS Output Load AC Test Circuit



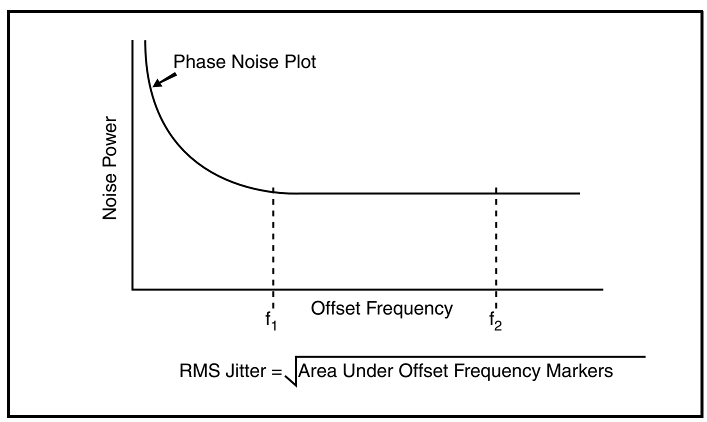
Output Skew



Output Rise/Fall Time

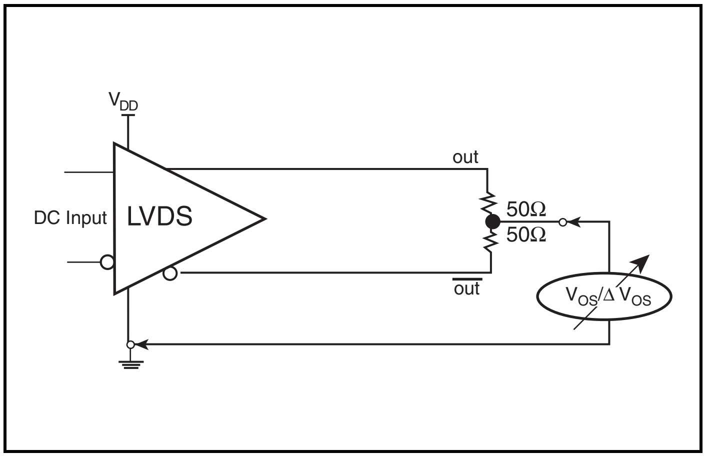


Output Duty Cycle/Pulse Width/Period

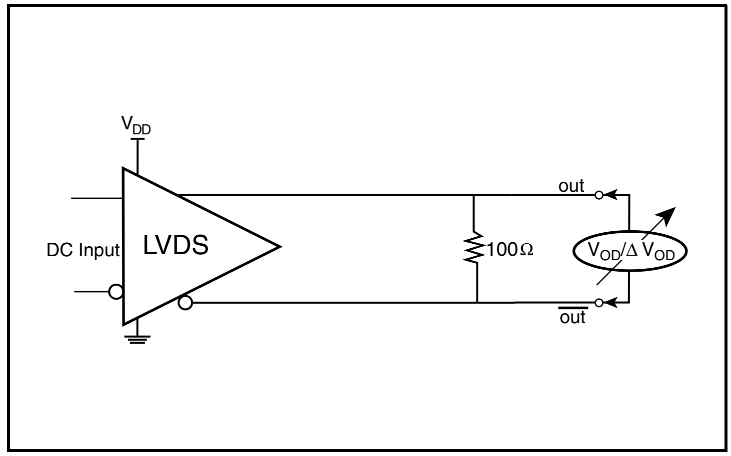


RMS Phase Jitter

Parameter Measurement Information, continued



Offset Voltage Setup



Differential Output Voltage Setup

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS844244I-04 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

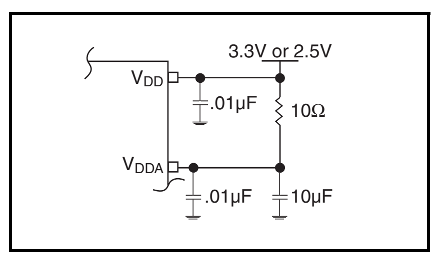


Figure 1. Power Supply Filtering

Crystal Input Interface

The ICS844244I-04 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

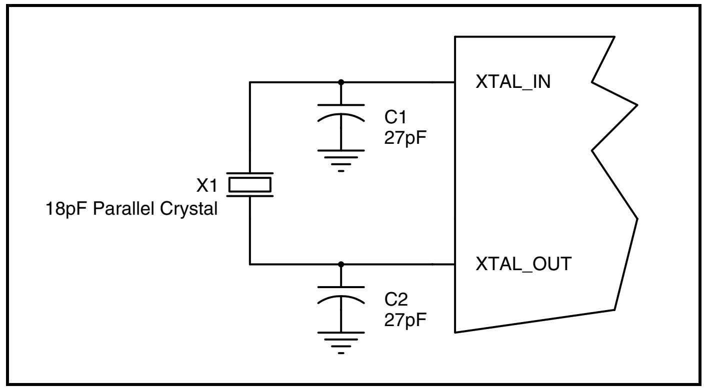


Figure 2. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3A.* The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

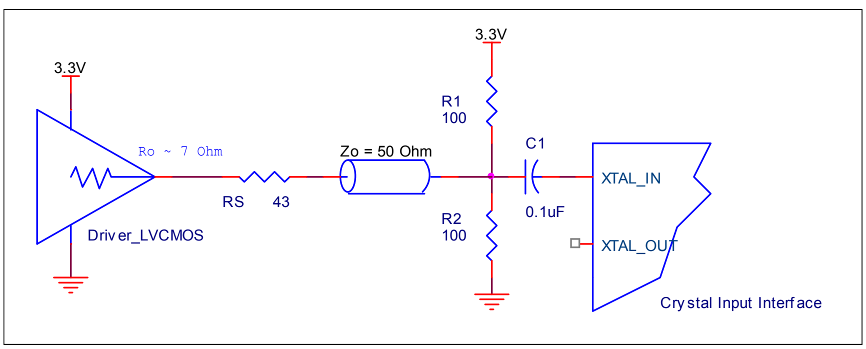


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

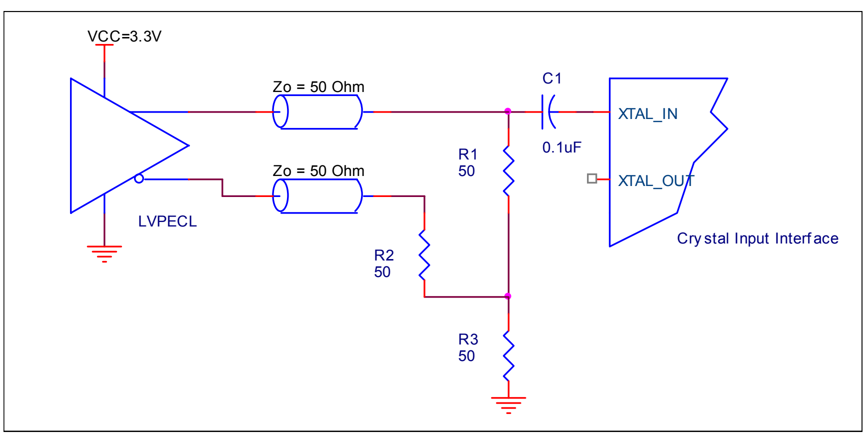


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

Recommendations for Unused Output Pins

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

3.3V, 2.5V LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

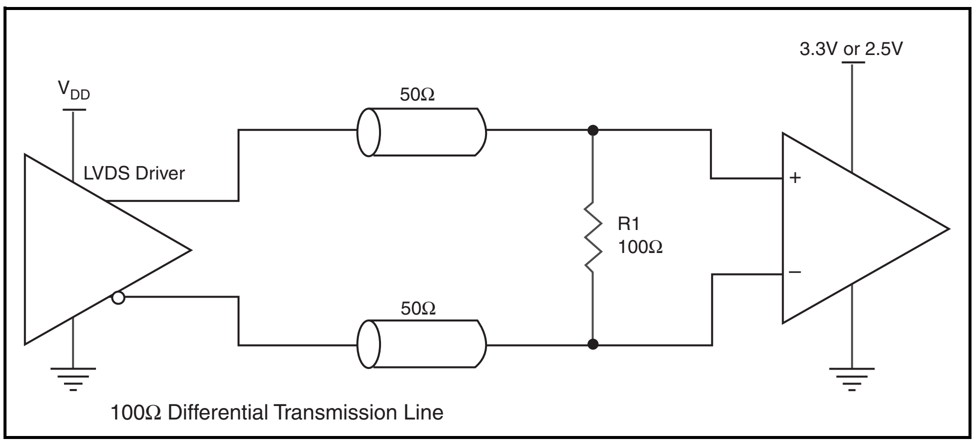


Figure 4. Typical LVDS Driver Termination

Application Schematic Example

Figure 5 shows an example of ICS844244I-04 application schematic. In this example, the device is operated at V_{DD} = 3.3V. The decoupling capacitor should be located as close as possible to the power pin. The 18pF parallel resonant 25MHz crystal is used. The C1 = 27pF and C2 = 27pF are recommended for frequency accuracy. For different board layouts, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. For the LVDS output drivers, place a 100Ω resistor as close to the receiver as possible.

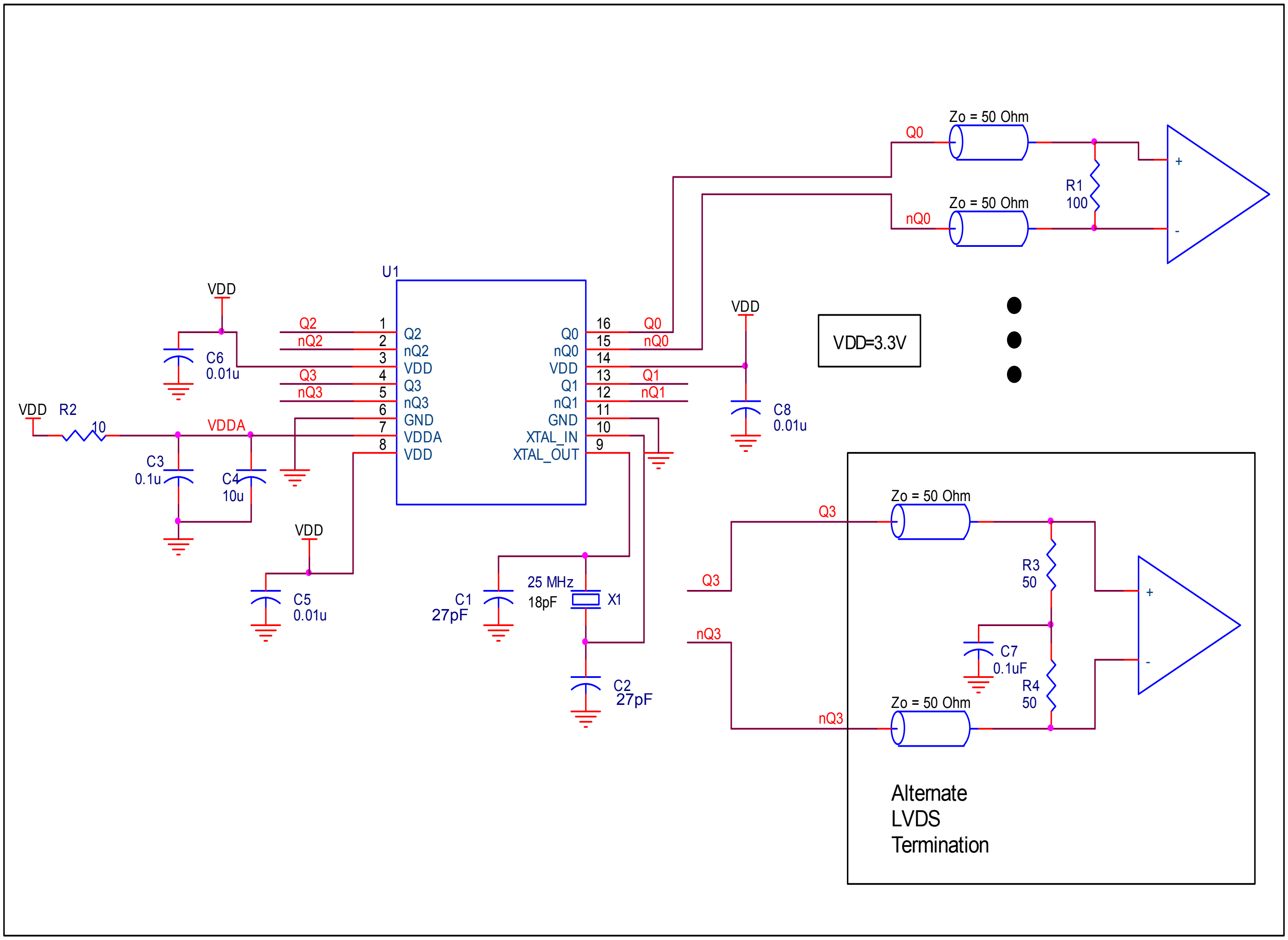


Figure 5. ICS844244I-04 Application Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS844244I-04.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS844244I-04 is the sum of the core power plus the analog power plus the power dissipation in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.465V * (121mA + 10mA) = **453.9mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 88°C/W per Table 5 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.4539W * 88°C/W = 124.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 5. Thermal Resistance θ_{JA} for 16 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	92.4°C/W	88.0°C/W	85.9°C/W

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 16 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	92.4°C/W	88.0°C/W	85.9°C/W

Transistor Count

The transistor count for ICS844244I-04 is: 1990

Package Outline and Package Dimensions

Package Outline - G Suffix for 8 Lead TSSOP

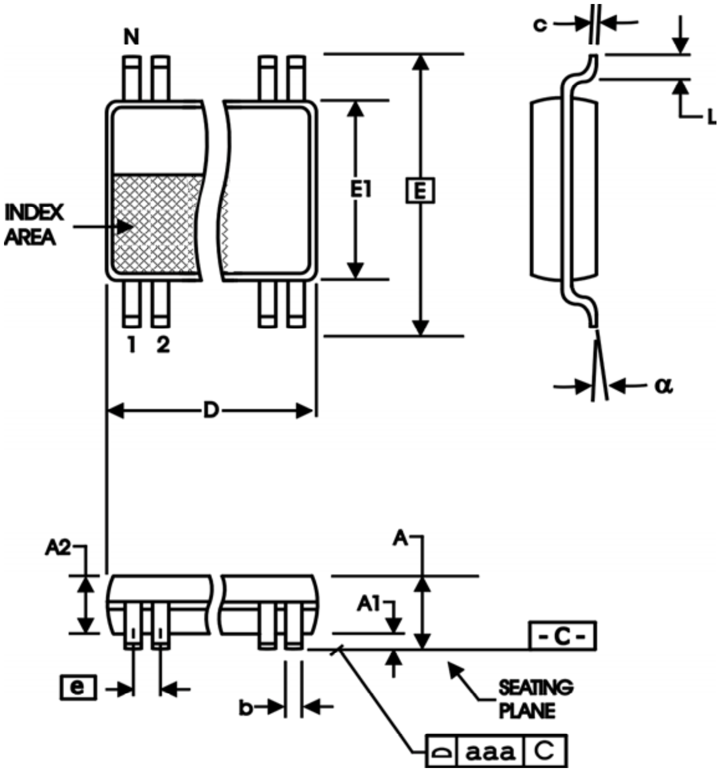


Table 7. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 89. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844244AGI-04	4244AI04	16 Lead TSSOP	Tube	-40°C to 85°C
844244AGI-04T	4244AI04	16 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C
844244AGI-04LF	244AI04L	“Lead-Free” 16 Lead TSSOP	Tube	-40°C to 85°C
844244AGI-04LFT	244AI04L	“Lead-Free” 16 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

www.IDT.com

6024 Silver Creek Valley Road
San Jose, California 95138

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

Technical Support
netcom@idt.com
+480-763-2056