Jameco Part Number 1654065

ICS85311
LOW SKEW, 1-TO-2 DIFFERENTIAL-TO-2.5V/3.3V ECL/LVPECL FANOUT BUFFER

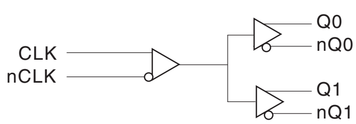
GENERAL DESCRIPTION

The ICS85311 is a low skew, high performance 1-to-2 Differential-to-2.5V/3.3V ECL/LVPECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The CLK, nCLK pair can accept most standard differential input levels. The ICS85311 is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS85311 ideal for those clock distribution applications demanding well defined performance and repeatability.

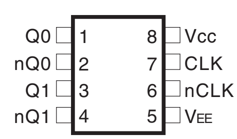
FEATURES

- Two differential 2.5V/3.3V LVPECL / ECL outputs
- One CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 1GHz
- Translates any single ended input signal to 3.3V LVPECL levels with resistor bias on nCLK input
- Output skew: 15ps (maximum)
- Part-to-part skew: 100ps (maximum)
- Propagation delay: 1.4ns (maximum)
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.465V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -2.375V to -3.465V
- 0°C to 70°C ambient operating temperature
- Available in both, Standard and RoHS/Lead-Free compliant packages
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS85311
8-Lead SOIC
3.90mm x 4.90mm x 1.37mm package body
M Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVPECL interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. LVPECL interface levels.
5	V_{EE}	Power		Negative supply pin.
6	nCLK	Input	Pullup	Inverting differential clock input.
7	CLK	Input	Pulldown	Non-inverting differential clock input.
8	V_{CC}	Power		Positive supply pin.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	112°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 3.3V±5% OR 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{CC}	Positive Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				25	mA

TABLE 3B. DIFFERENTIAL DC CHARACTERISTICS, V_{CC} = 3.3V±5% OR 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{CC} = V_{IN}$ = 3.465V or 2.625V			150	µA
		nCLK	$V_{CC} = V_{IN}$ = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	CLK	V_{CC} = 3.465V or 2625V, V_{IN} = 0V	-5			µA
		nCLK	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltag for CLK, nCLK is V_{CC} + 0.3V.

TABLE 3C. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5% OR 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.65		1.0	V

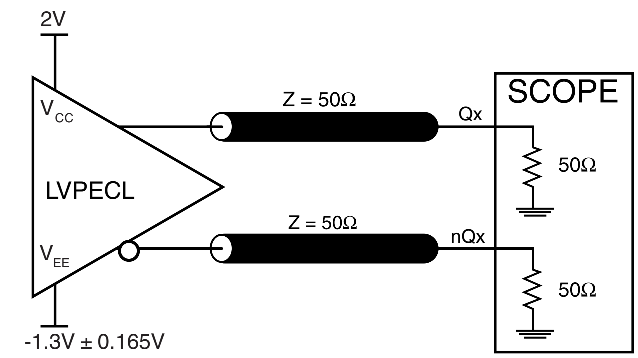
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 4. AC CHARACTERISTICS, V_{CC} = 3.3V±5% OR 2.5V±5%, TA = 0°C TO 70°C

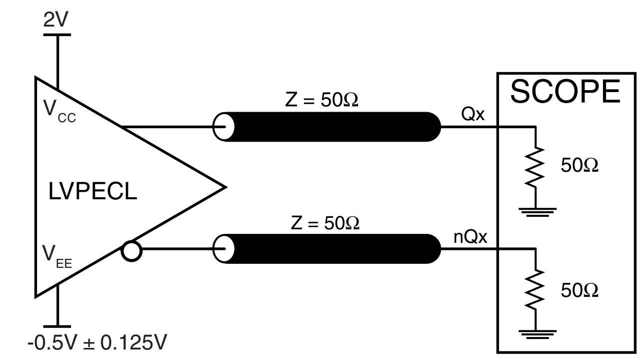
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				1	GHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 1GHz	0.9		1.4	ns
$t$sk(o)	Output Skew; NOTE 2, 4				15	ps
$t$sk(pp)	Part-to-Part Skew; NOTE 3, 4				100	ps
t_R	Output Rise Time	20% to 80% @ 50MHz	300		700	ps
t_F	Output Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		48		52	%

All parameters measured at 500MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

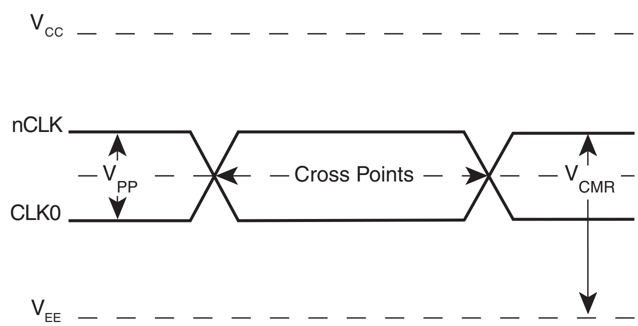
PARAMETER MEASUREMENT INFORMATION



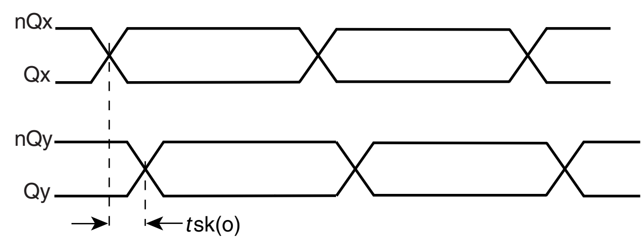
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



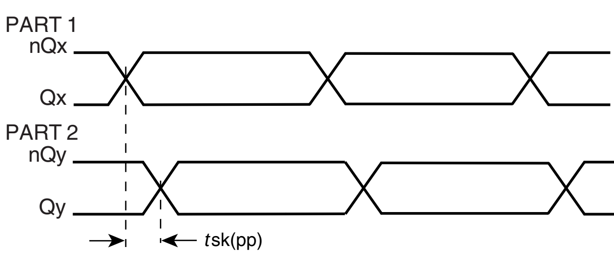
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



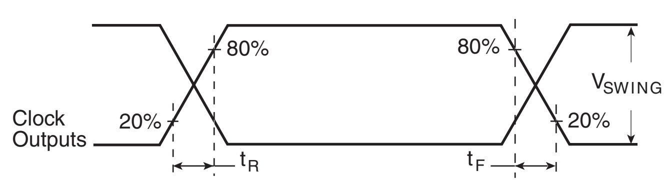
DIFFERENTIAL INPUT LEVEL



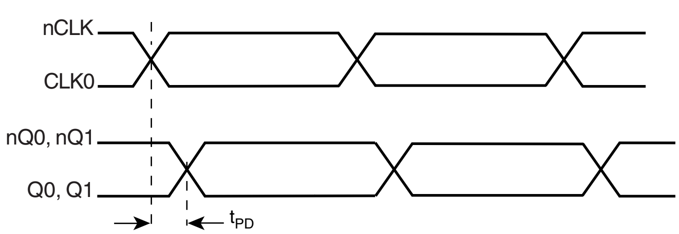
OUTPUT SKEW



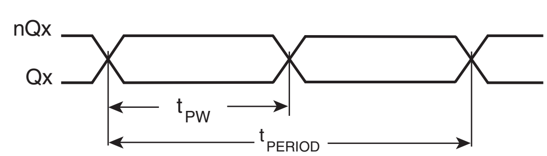
PART-TO-PART SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Output Duty Cycle/Pulse Width/PERIOD

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ~ $V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

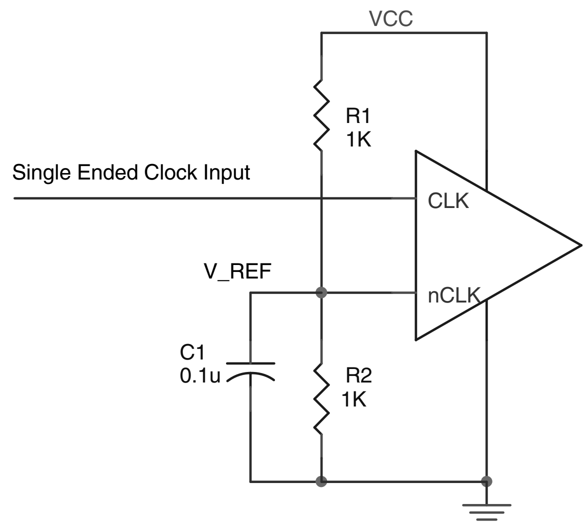


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

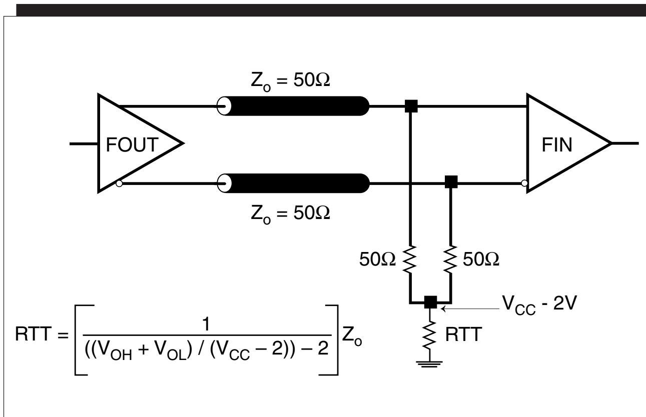


FIGURE 2A. LVPECL OUTPUT TERMINATION

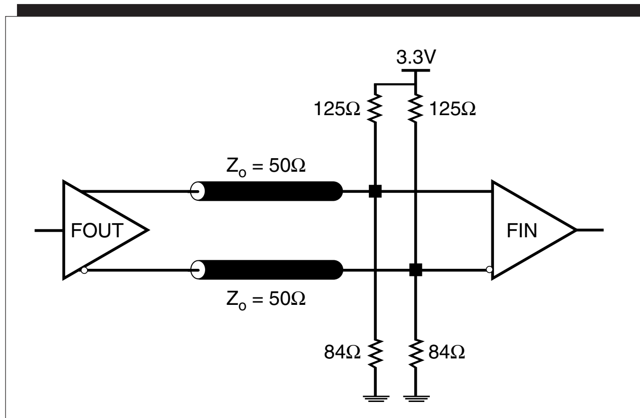


FIGURE 2B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 3A and *Figure 3B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 3B can be eliminated and the termination is shown in *Figure 3C.*

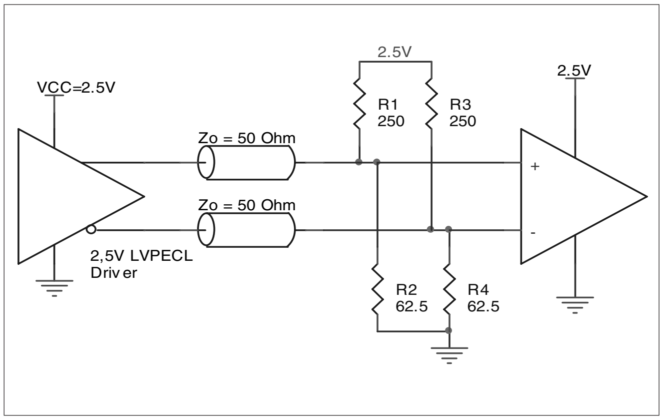


FIGURE 3A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

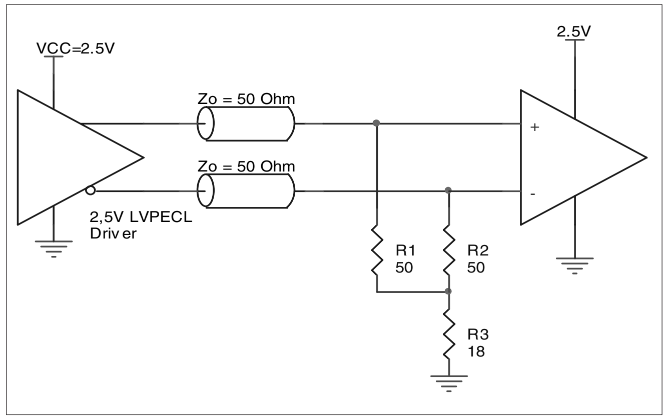


FIGURE 3B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

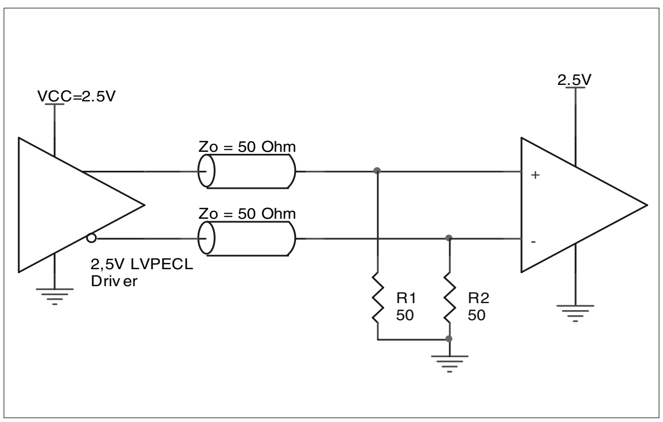


FIGURE 3C. 2.5V LVPECL TERMINATION EXAMPLE

RECOMMENDATIONS FOR UNUSED OUTPUT PINS

OUTPUTS:

LVPECL OUTPUTS:

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 4A to 4E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 4A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

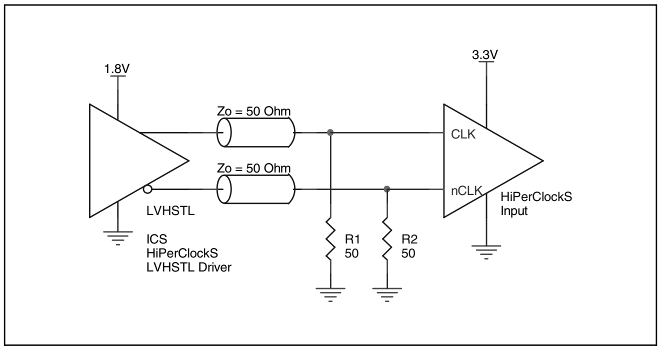


FIGURE 4A. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

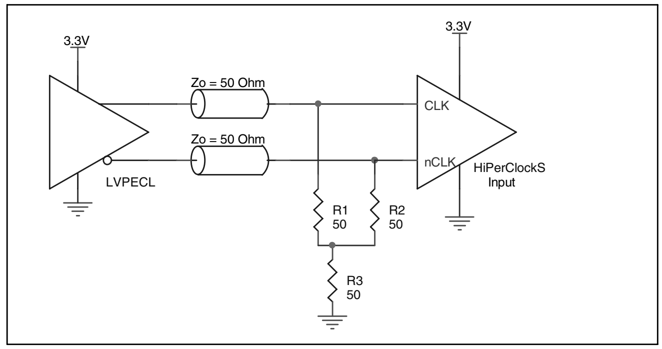


FIGURE 4B. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

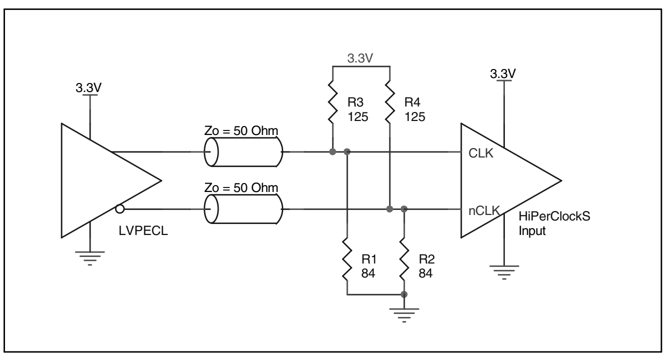


FIGURE 4C. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

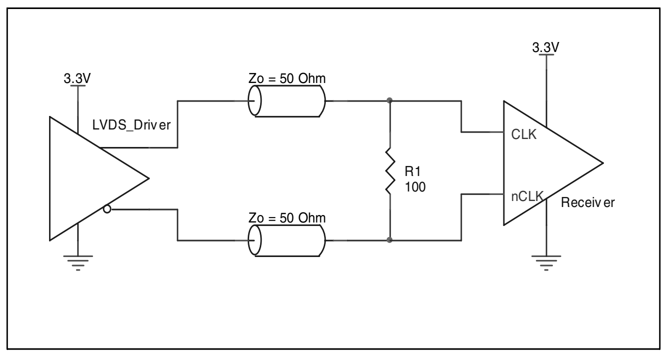


FIGURE 4D. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

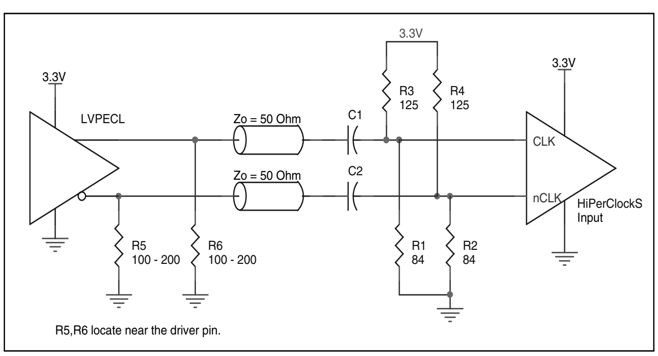


FIGURE 4E. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS85311.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS85311 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 25mA = **86.6mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30mW = **60mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 86.6mW + 60mW = **146.6mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature
θ_{JA} = Junction-to-Ambient Thermal Resistance
Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 103.3°C/W per Table 5 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.147W * 103.3°C/W = 85.2°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 5. THERMAL RESISTANCE θ_{JA} FOR 8-PIN SOIC, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5.*

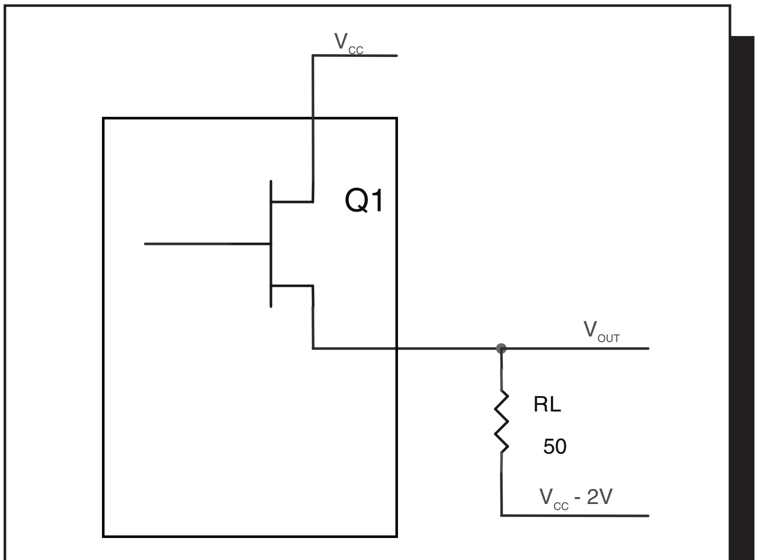


FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.9V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.7V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS85311 is: 225

PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD SOIC

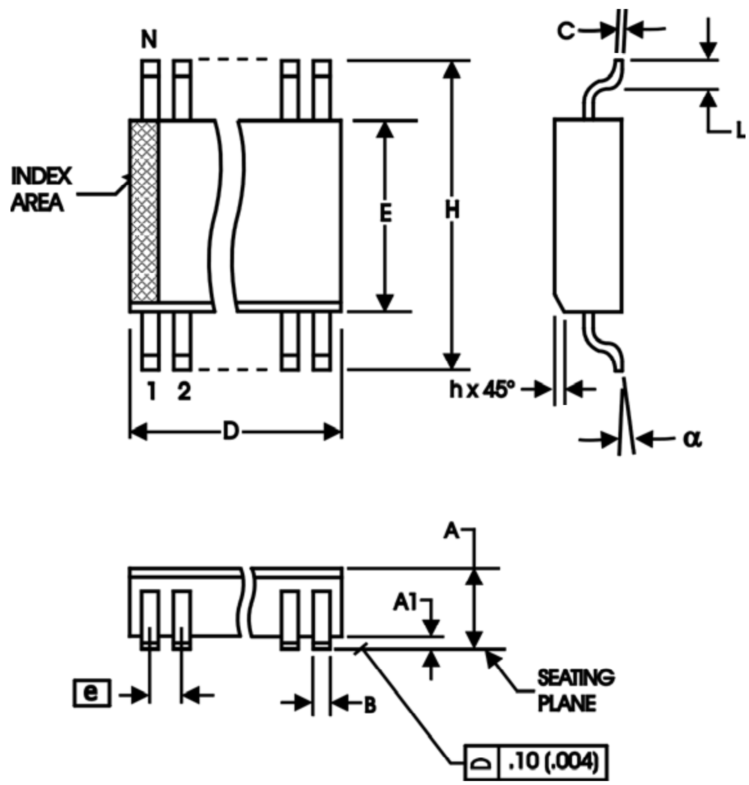


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUN	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS85311AM	85311AM	8 lead SOIC	tube	0°C to 70°C
ICS85311AMT	85311AM	8 lead SOIC	2500 tape & reel	0°C to 70°C
ICS85311AMLF	85311ALF	8 lead "Lead Free" SOIC	tube	0°C to 70°C
ICS85311AMLFT	85311ALF	8 lead "Lead Free" SOIC	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET

Rev	Table	Page	Description of Change	Date
A		8	Added Termination for LVPECL Outputs section.	5/30/02
A		5 7	3.3V Output Load Test Circuit Diagram - corrected V_{EE} equation to read -1.3V ± 0.165V from ± 0.135V. Updated Output Rise/Fall Time Diagram.	9/23/02
B	 T2 T8	1 2 3 3 5 6 7 8 13	Add Lead-Free bullet in Features section. Pin Characteristics table - changed CIN 4pF max. to 4pF typical. Absolute Maximum Ratings, updated Outputs rating. Combined 3.3V & 2.5V Power tables and Differential DC Characteristics tables. Updated Parameter Measurement Information. Updated Single Ended Signal Driving Differential Input diagram. Added Termination for 2.5V LVPECL Output section. Added Differential Clock Input Interface section. Ordering Information table - added Lead Free part number.	6/17/04
B	T8	7 13	Added Recommendations for Unused Input and Output Pins. Ordering Information Table - corrected Lead-Free marking and added Lead-Free Note.	7/28/05
C	T3C	3 9 - 10	LVPECL DC Characteristics Table -corrected V_{OH} max. from V_{CC} - 1.0V to V_{CCO} - 0.9V; and V_{SWING} max. from 0.9V to 1.0V. Power Considerations - corrected power dissipation to reflect V_{OH} max in Table 3C.	4/11/07