LOW SKEW, 1-TO-8, CRYSTAL OSCILLATOR/
LVCMOS-TO-3.3V LVPECL FANOUT BUFFER

ICS8538-31

General Description

ICS HiPerClockS™

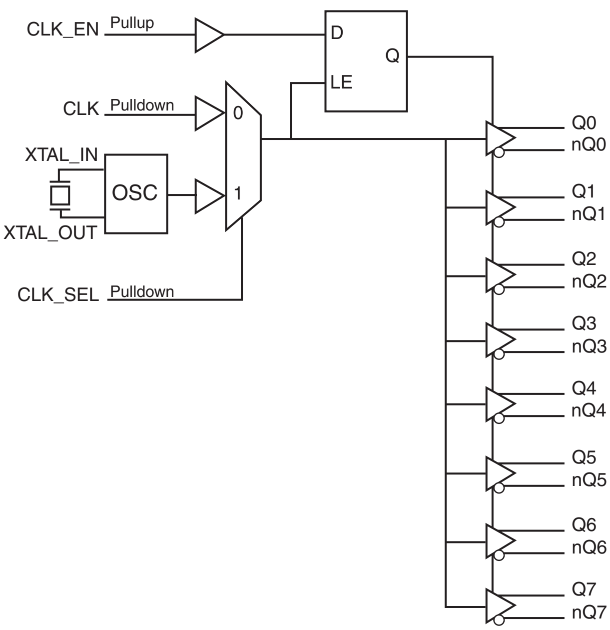
The ICS8538-31 is a low skew, high performance 1-to-8 Crystal Oscillator/LVCMOS-to-3.3V LVPECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS8538-31 has selectable single ended clock or crystal inputs. The single ended clock input accepts LVCMOS or LVTTL input levels and translate them to 3.3V LVPECL levels. The output enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8538-31 ideal for those applications demanding well defined performance and repeatability.

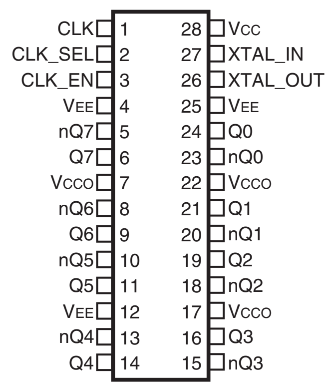
Features

- Eight differential 3.3V LVPECL outputs
- Selectable LVCMOS/LVTTL clock or crystal inputs
- CLK can accept the following input levels: LVCMOS, LVTTL
- Maximum output frequency: 266MHz
- Crystal frequency range: 14MHz - 40MHz
- Output skew: 50ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 2.2ns (maximum)
- 3.3V operating supply mode
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



28-Lead TSSOP, 173MIL
4.4mm x 9.7mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	CLK	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
2	CLK_SEL	Input	Pulldown	
3	CLK_EN	Input	Pullup	
4, 12, 25	V_{EE}	Power		Negative supply pins.
5, 6	nQ7, Q7	Output		Differential output pair. LVPECL interface levels.
7, 17, 22	V_{CCO}	Power		Output supply pins.
8, 9	nQ6, Q6	Output		Differential output pair. LVPECL interface levels.
10, 11	nQ5, Q5	Output		Differential output pair. LVPECL interface levels.
13, 14	nQ4, Q4	Output		Differential output pair. LVPECL interface levels.
15, 16	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.
18, 19	nQ2, Q2	Output		Differential output pair. LVPECL interface levels.
20, 21	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
23, 24	nQ0, Q0	Output		Differential output pair. LVPECL interface levels.
26, 27	XTAL_OUT XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
28	V_{CC}	Power		Positive supply pin.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Control Input Function Table

Inputs			Outputs	
CLK_EN	**CLK_SEL**	**Selected Source**	**Q0:Q7**	**nQ0:nQ7**
0	0	CLK	Disabled; Low	Disabled; High
0	1	XTAL_IN, XTAL_OUT	Disabled; Low	Disabled; High
1	0	CLK	Enabled	Enabled
1	1	XTAL_IN, XTAL_OUT	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock or crystal oscillator edge as shown in Figure 1. In the active mode, the state of the outputs are a function of the CLK input as described in Table 3B.

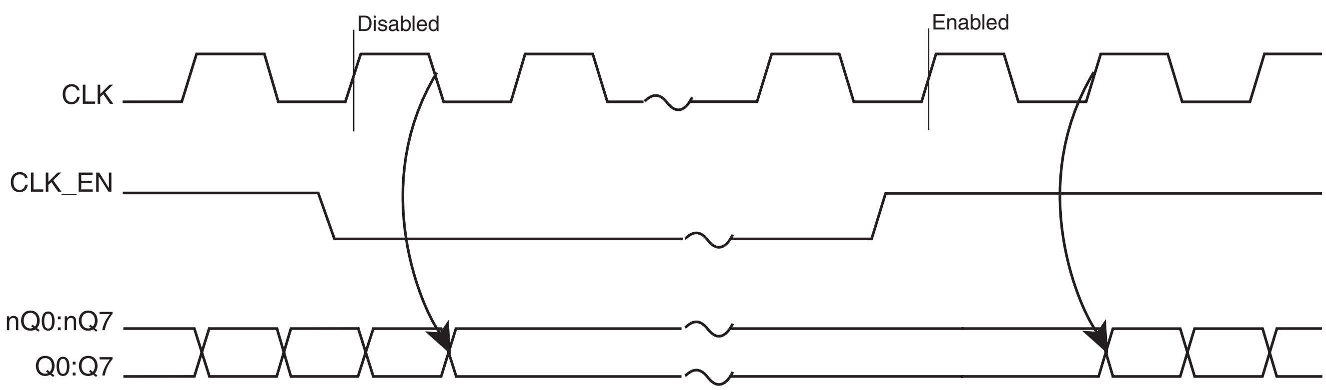


Figure 1. CLK_EN Timing Diagram

Table 3B. Clock Input Function Table

Inputs	Outputs	
CLK	**Q0:Q7**	**nQ0:nQ7**
0	LOW	HIGH
1	HIGH	LOW

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC}+ 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	49.8°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				110	mA
I_{CCO}	Output Supply Current				50	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK, CLK_SEL	$V_{CC} = V_{IN} = 3.465V$			150	µA
		CLK_EN	$V_{CC} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	CLK, CLK_SEL	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			µA
		CLK_EN	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA

Table 4C. LVPECL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Current; NOTE 1		V_{CCO} – 1.4		V_{CCO} – 0.9	µA
V_{OL}	Output Low Current; NOTE 1		V_{CCO}– 2.0		V_{CCO} – 1.7	µA
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} – 2V.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		14		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

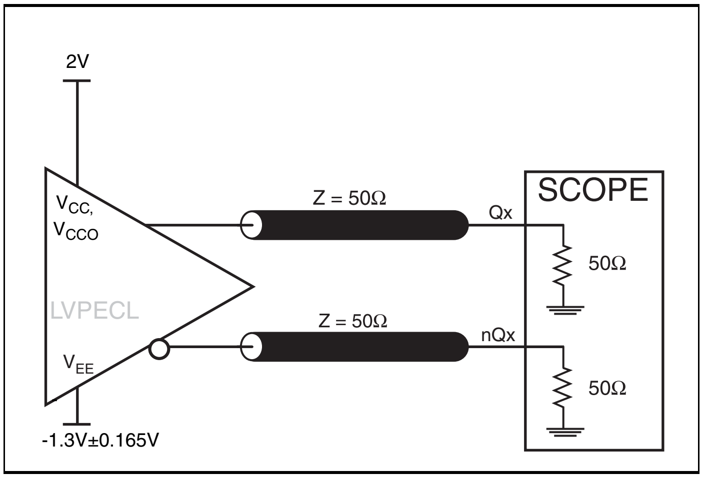
AC Electrical Characteristics

Table 6. AC Characteristics, $V_{CC} = V_{CCO} = 3.3V\pm5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

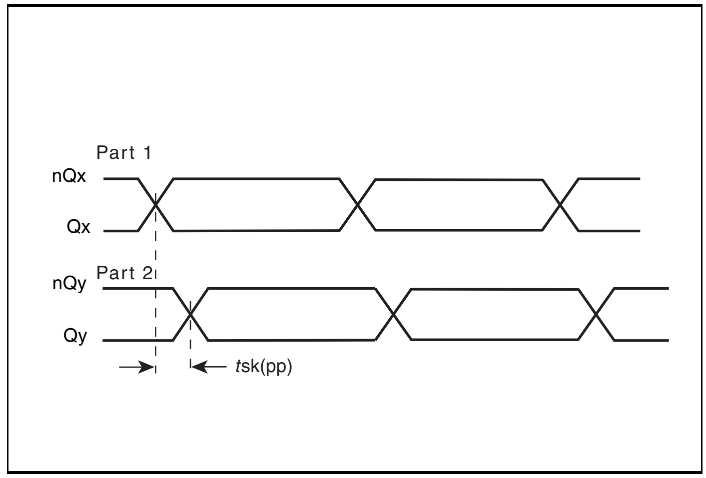
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				266	MHz
t_{PD}	Propagation Delay; NOTE 1				2.2	ns
*t*sk(o)	Output Skew; NOTE 2, 4				50	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				250	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		45		55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from $V_{CC}/2$ input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

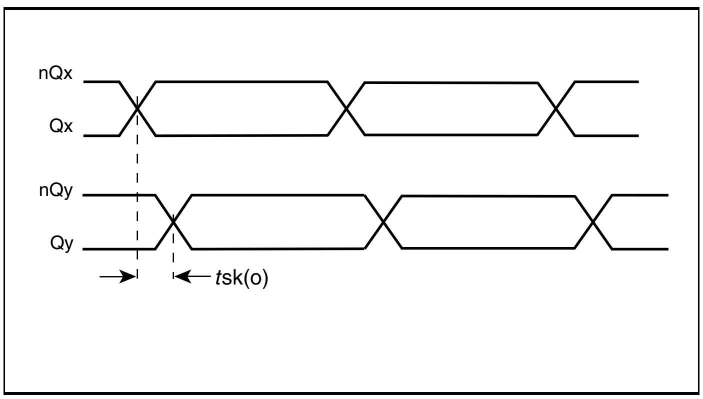
Parameter Measurement Information



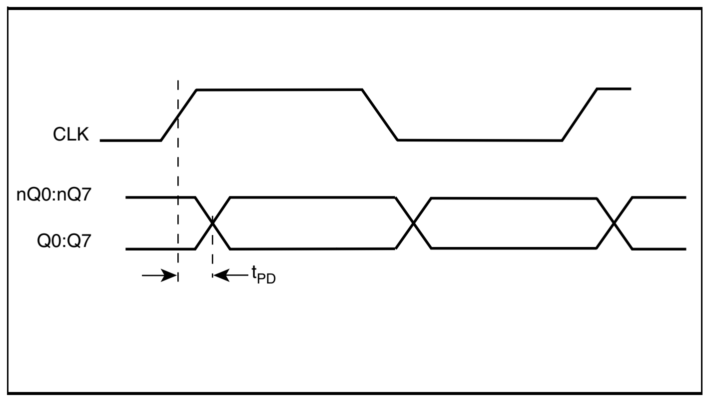
3.3/3.3V LVPECL Output Load AC Test Circuit



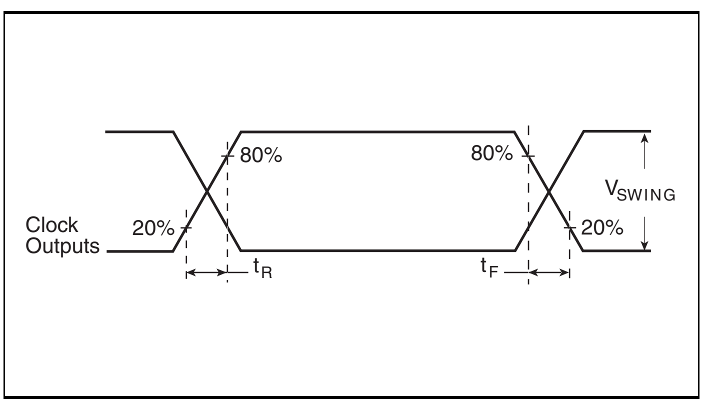
Part-to-Part Skew



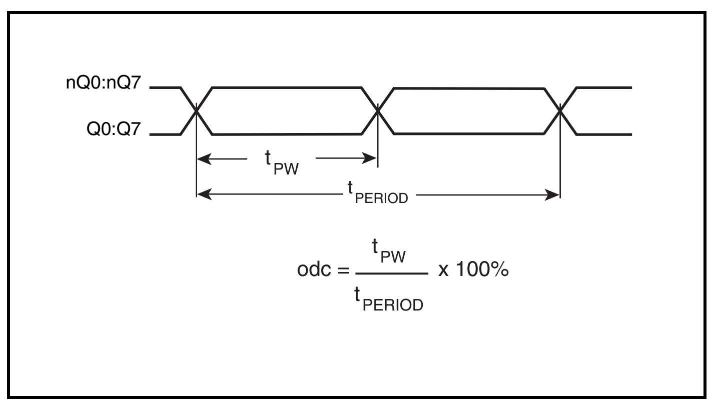
Output Skew



Propagation Delay



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Application Information

Crystal Input Interface

The ICS8538-31 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. These same capacitor values will tune any 18pF parallel resonant crystal over the frequency range and other parameters specified in this data sheet. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

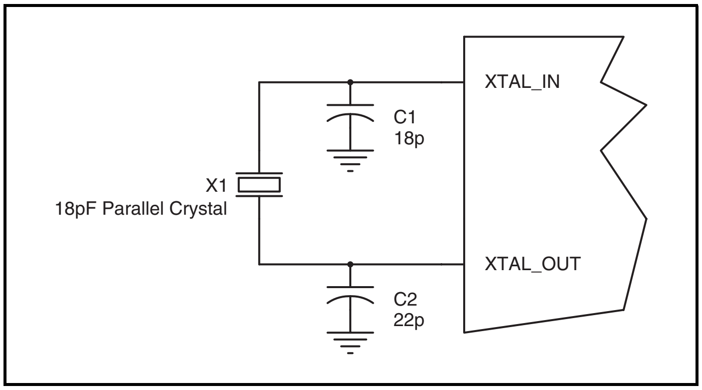


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

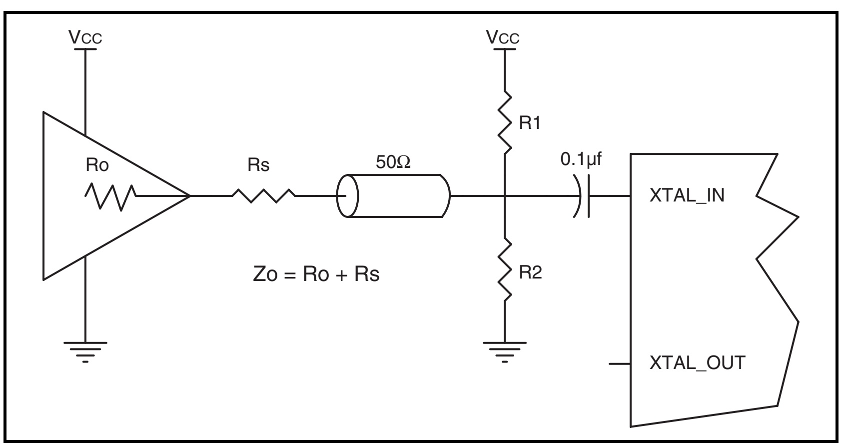


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK Input

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

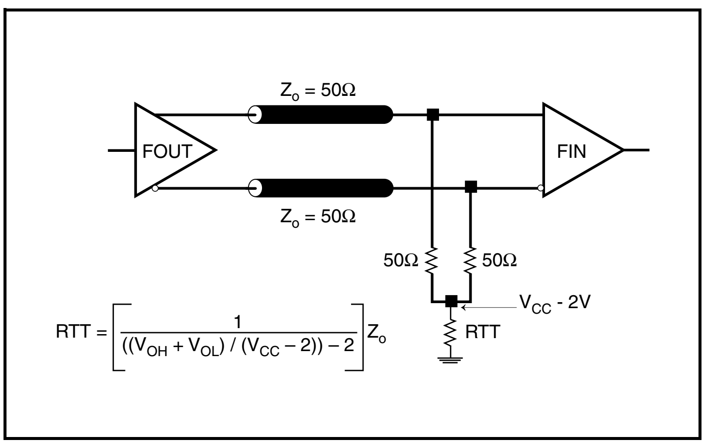


Figure 4A. 3.3V LVPECL Output Termination

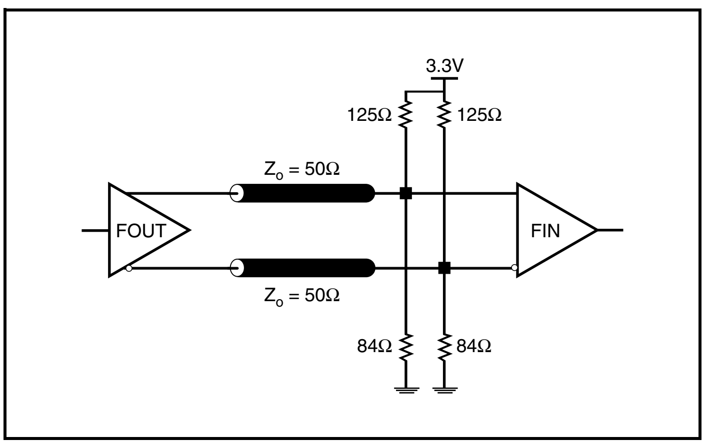


Figure 4B. 3.3V LVPECL Output Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8538-31.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8538-31 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 110mA = **381.15mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 8 * 30mW = **240mW**

Total Power$_{\_MAX}$ (3.3V, with all outputs switching) = 381.15mW + 240mW = **621.15mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 49.8°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.621W * 49.8°C/W = 100.9°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 7. Thermal Resistance θ_{JA} for 28 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	82.9°C/W	68.7°C/W	60.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	49.8°C/W	43.9°C/W	41.2°C/W

NOTE: Most modern PCB design use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5.*

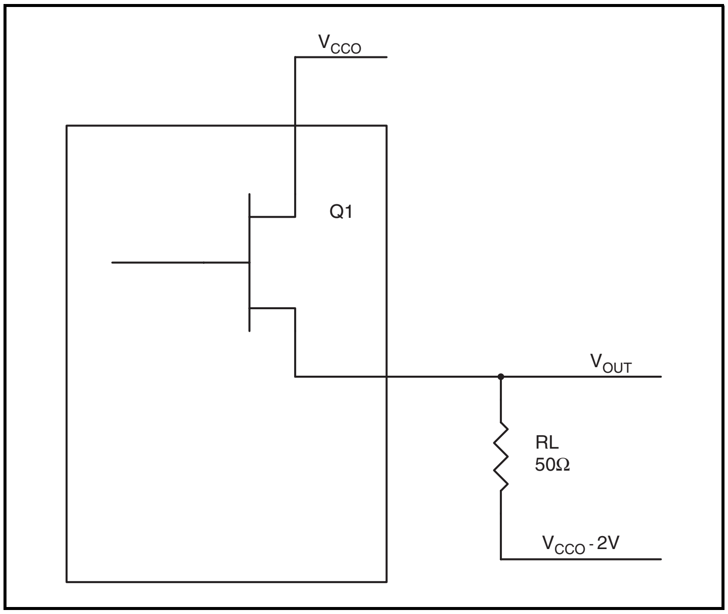


Figure 5. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} – 0.9V}$
  $(V_{CCO\_MAX} – V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CO\_MAX} – 1.7V}$
  $(V_{CCO\_MAX} – V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

Pd_H = $[(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) =$ $[(2V – 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

Pd_L = $[(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) =$ $[(2V – 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 282 Lead TSSOP

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	82.9°C/W	68.7°C/W	60.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	49.8°C/W	43.9°C/W	41.2°C/W

NOTE: Most modern PCB design use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for ICS8430-62 is: 4258

Package Outline and Package Dimension

Package Outline - G Suffix for 28 Lead TSSOP

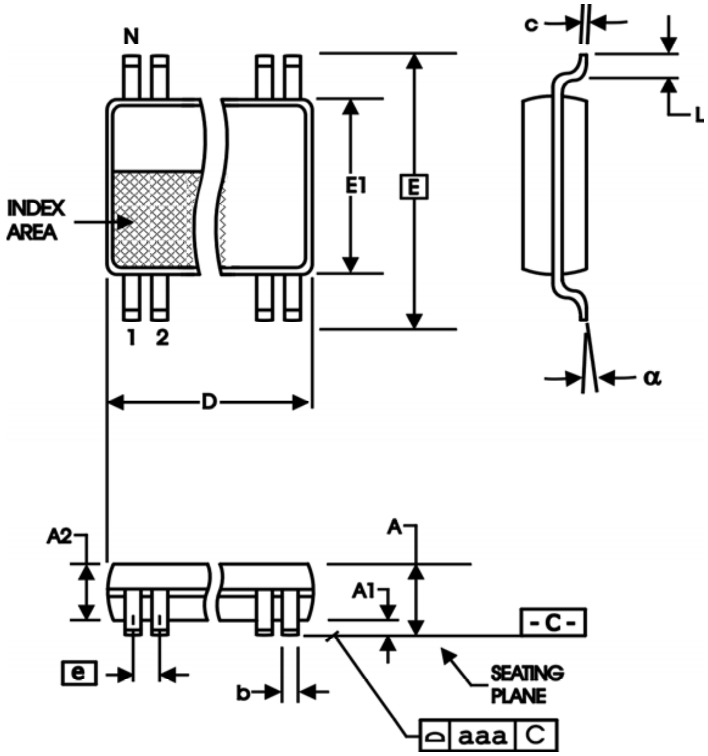


Table 9. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	28	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	9.60	9.80
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS8538BG-31	ICS8538BG-31	28 Lead TSSOP	Tube	0°C to 70°C
ICS8538BG-31T	ICS8538BG-31	28 Lead TSSOP	1000 Tape & Reel	0°C to 70°C
ICS8538BG-31LF	ICS8538BG-31LF	“Lead-Free” 28 Lead TSSOP	Tube	0°C to 70°C
ICS8538BG-31LFT	ICS8538BG-31LF	“Lead-Free” 28 Lead TSSOP	1000 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T10	13	Ordering Information table - added Lead-Free marking.	1/18/08
B	T6	5 9	AC Characteristics Table - changed Output Rise/Fall parameters from 500ps min. to 200ps min., and 850ps max. to 700ps max. Power Considerations - updated Junction Temperature equation with worst case thermal resistance of 0 lfpm at 49.8°C/W.	2/5/08

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