Low Skew, 1-to-5 Differential-to-HSTL Zero Delay Buffer

ICS8624

DATA SHEET

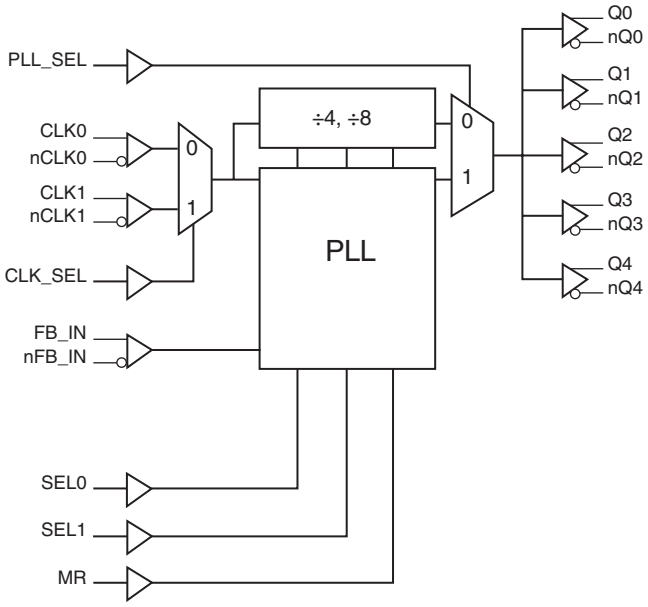
General Description

The ICS8624 is a high performance, 1-to-5 Differential-to-HSTL zero delay buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS8624 has two selectable clock input pairs. The CLK0, nCLK0 and CLK1, nCLK1 pair can accept most standard differential input levels. The VCO operates at a frequency range of 250MHz to 700MHz. Utilizing one of the outputs as feedback to the PLL, output frequencies up to 700MHz can be regenerated with zero delay with respect to the input. Dual reference clock inputs support redundant clock or multiple reference applications.

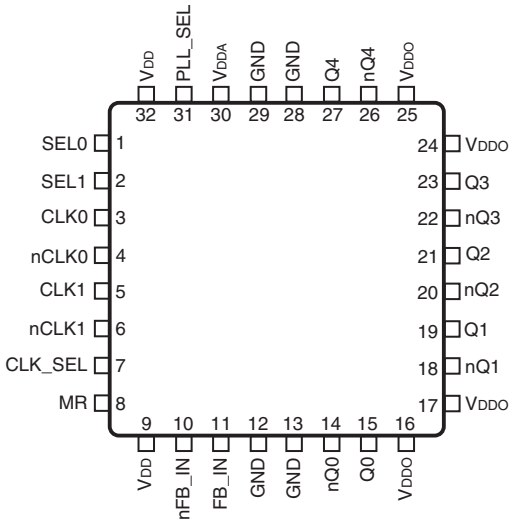
Features

- Fully integrated PLL
- Five differential HSTL output pairs
- Selectable differential CLKx/nCLKx input pairs
- CLKx/nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, HSTL, HCSL, SSTL
- Output frequency range: 31.25MHz to 700MHz
- Input frequency range: 31.25MHz to 700MHz
- VCO range: 250MHz to 700MHz
- External feedback for “zero delay” clock regeneration
- Cycle-to-cycle jitter: 25ps (maximum)
- Output skew: 25ps (maximum)
- Static phase offset: ±100ps
- 3.3V core, 1.8V output operating supply
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS8624

32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	SEL0, SEL1	Input	Pulldown	Determines the input and output frequency range noted in Table 3A. LVCMOS / LVTTL interface levels.
3	CLK0	Input	Pulldown	Non-inverting differential clock input.
4	nCLK0	Input	Pullup	Inverting differential clock input.
5	CLK1	Input	Pulldown	Non-inverting differential clock input.
6	nCLK1	Input	Pullup	Inverting differential clock input.
7	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1, nCLK1. When LOW, selects CLK0, nCLK0. LVCMOS/LVTTL interface levels.
8	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
9, 32	V_{DD}	Power		Core supply pins.
10	nFB_IN	Input	Pullup	Inverting differential feedback input to phase detector for regenerating clocks with “Zero Delay.”
11	FB_IN	Input	Pulldown	Non-inverted differential feedback input to phase detector for regenerating clocks with “Zero Delay.”
12, 13, 28, 29	GND	Power		Power supply ground.
14, 15	nQ0, Q0	Output		Differential output pair. HSTL interface levels.
16, 17, 24, 25	V_{DDO}	Power		Output supply pins.
18, 19	nQ1, Q1	Output		Differential output pair. HSTL interface levels.
20, 21	nQ2, Q2	Output		Differential output pair. HSTL interface levels.
22, 23	nQ3, Q3	Output		Differential output pair. HSTL interface levels.
26, 27	nQ4, Q4	Output		Differential output pair. HSTL interface levels.
30	V_{DDA}	Power		Analog supply pin.
31	PLL_SEL	Input	Pullup	PLL select. Selects between the PLL and reference clock as the input to the dividers. When LOW, selects reference clock. When HIGH, selects PLL. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Control Input Function Table

Inputs			Outputs PLL_SEL = 1 PLL Enable Mode
SEL1	**SEL0**	**Reference Frequency Range (MHz)***	**Q[0:4], nQ[0:4]**
0	0	250 - 700	÷1
0	1	125 - 350	÷1
1	0	62.5 - 175	÷1
1	1	31.25 - 87.5	÷1

*NOTE: VCO frequency range for all configurations above is 250MHz to 700MHz.

Table 3B. PLL Bypass Function Table

Inputs		Outputs PLL_SEL = 0 PLL Bypass Mode
SEL1	**SEL0**	**Q[0:4], nQ[0:4]**
0	0	÷4
0	1	÷4
1	0	÷4
1	1	÷8

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.5V to 2V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.5	1.8	2.0	V
I_{DD}	Power Supply Current				120	mA
I_{DDA}	Analog Supply Current				15	mA
I_{DDO}	Output Supply Current			0		mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ± 0.2V, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK_SEL, SEL[0:1], MR	V_{DD} = V_{IN} = 3.465V			150	µA
		PLL_SEL	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	CLK_SEL, SEL[0:1], MR	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		PLL_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ± 0.2V, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	FB_IN, CLK0, CLK1	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nFB_IN, nCLK0, nCLK1	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	FB_IN, CLK0, CLK1	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nFB_IN, nCLK0, nCLK1	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.1		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4D. HSTL DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ± 0.2V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		1.0		1.4	V
V_{OL}	Output Low Voltage; NOTE 1		0		0.4	V
V_{OX}	Output Crossover Voltage; NOTE 2		40		60	%
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.1	V

NOTE 1: Outputs terminated with 50Ω to ground.
NOTE 2: Defined with respect to output voltage swing at a given condition.

Table 5. Input Frequency Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ± 0.2V, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
F_{IN}	Input Frequency	CLK0, nCLK0, CLK1, nCLK1	PLL_SEL = 1	31.25		700	MHz
			PLL_SEL = 0			700	MHz

AC Electrical Characteristics

Table 6A. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ± 0.2V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				700	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 700MHz	3.2		4.4	ns
t(Ø)	Static Phase Offset; NOTE 2, 5	PLL_SEL = 3.3V	-100		100	ps
*t*sk(o)	Output Skew; NOTE 3, 5				25	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 5, 6				25	ps
*t*jit(θ)	Phase Jitter; NOTE 4, 5, 6				±50	ps
t_L	PLL Lock Time				1	ms
t_R / t_F	Output Rise/Fall Time	20% to 80% @ 50MHz	300		700	ps
t_{PW}	Output Pulse Width		$t_{cycle}/2$ - 85	$t_{cycle}/2$	$t_{cycle}/2$ + 85	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as the time difference between the input reference clock and the averaged feedback input signal across all conditions, when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 4: Phase jitter is dependent on the input source used.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 6: Characterized at VCO frequency of 622MHz.

Table 6B. AC Characteristics, V_{DD} = 3.3V ± 10%, V_{DDO} = 1.8V ± 0.2V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1				35	ps

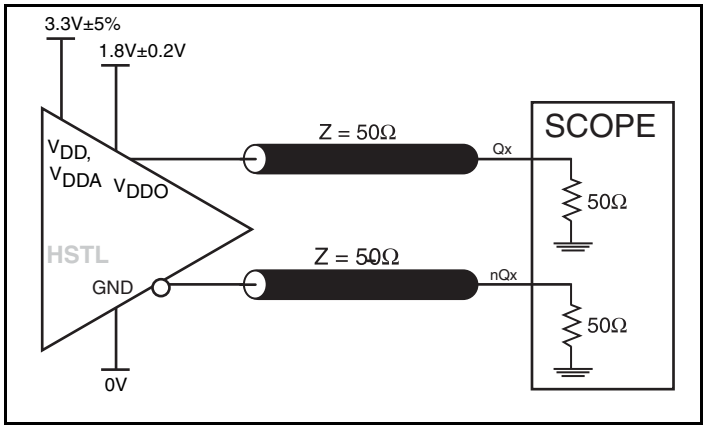
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

Table 6C. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.5V to 1.6V, T_A = 0°C to 70°C

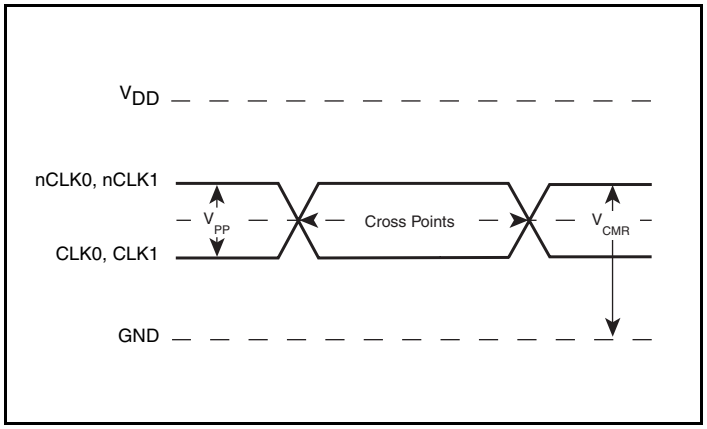
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				700	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 700MHz	3.2		4.4	ns
t(Ø)	Static Phase Offset; NOTE 2, 5	PLL_SEL = 3.3V	-100		150	ps
*t*sk(o)	Output Skew; NOTE 3, 5				35	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 5, 6				25	ps
*t*jit(θ)	Phase Jitter; NOTE 4, 5, 6				±50	ps
t_L	PLL Lock Time				1	ms
t_R / t_F	Output Rise/Fall Time	20% to 80% @ 50MHz	300		700	ps
t_{PW}	Output Pulse Width		$t_{cycle}/2$ - 95	$t_{cycle}/2$	$t_{cycle}/2$ + 95	ps

For NOTES, see Table 6A above.

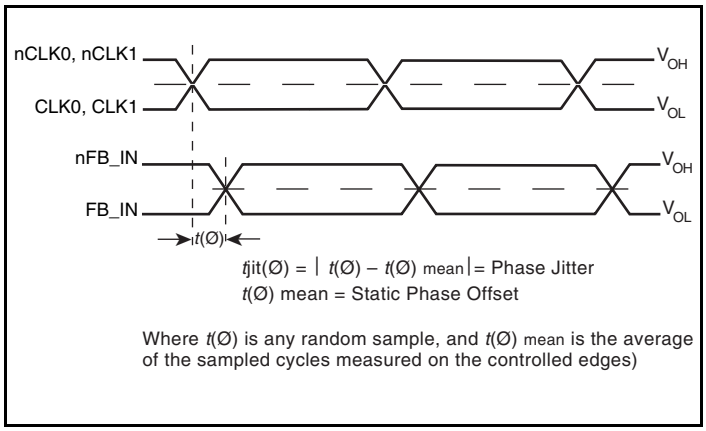
Parameter Measurement Information



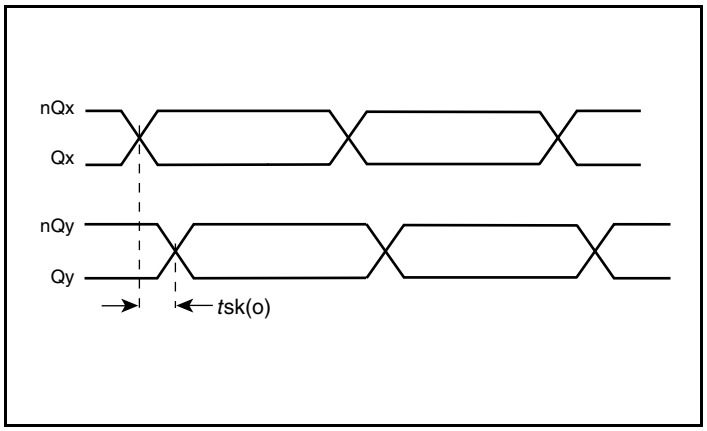
3.3V Core/1.8V Output Load AC Test Circuit



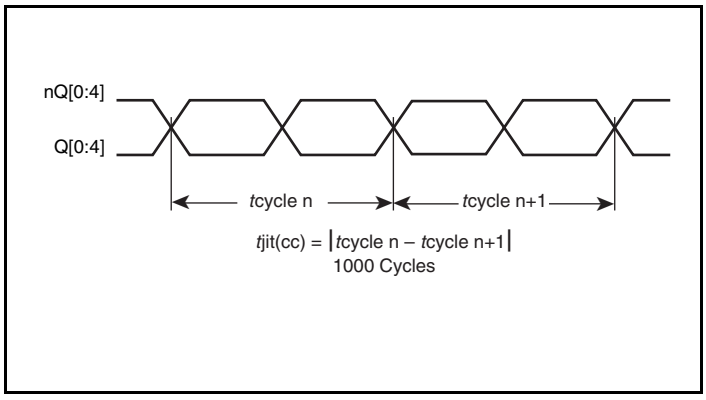
Differential Input Level



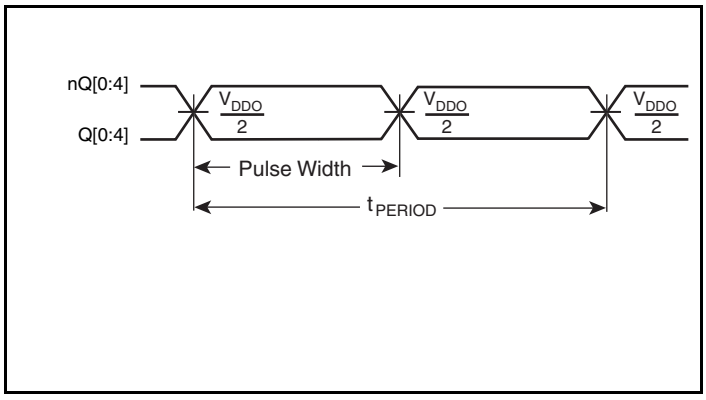
Phase Jitter and Static Phase Offset



Output Skew

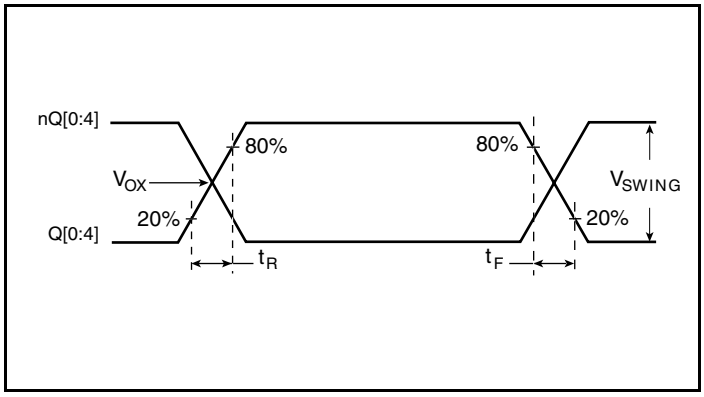


Cycle-to-Cycle Jitter

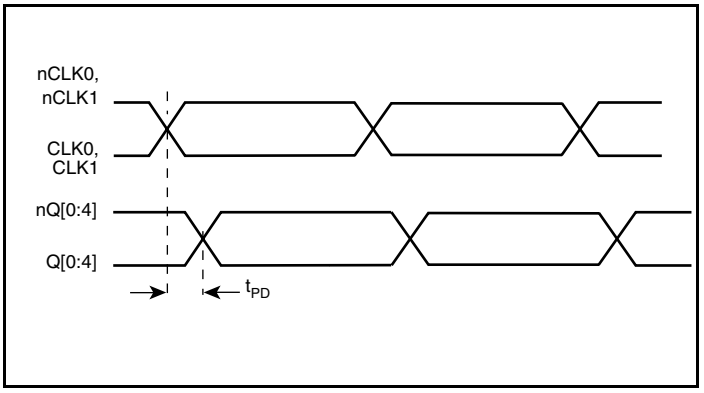


Output Pulse Width/Period

Parameter Measurement Information, continued



Output Rise/Fall Time



Propagation Delay

Application Information

Power Supply Filtering Technique

To achieve optimum jitter performance, power supply isolation is required. To achieve optimum jitter performance, power supply isolation is required. The ICS8624 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

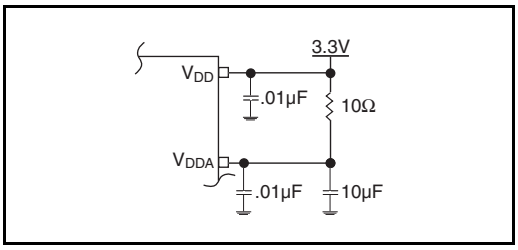


Figure 1. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Outputs:

HSTL Outputs

All unused HSTL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

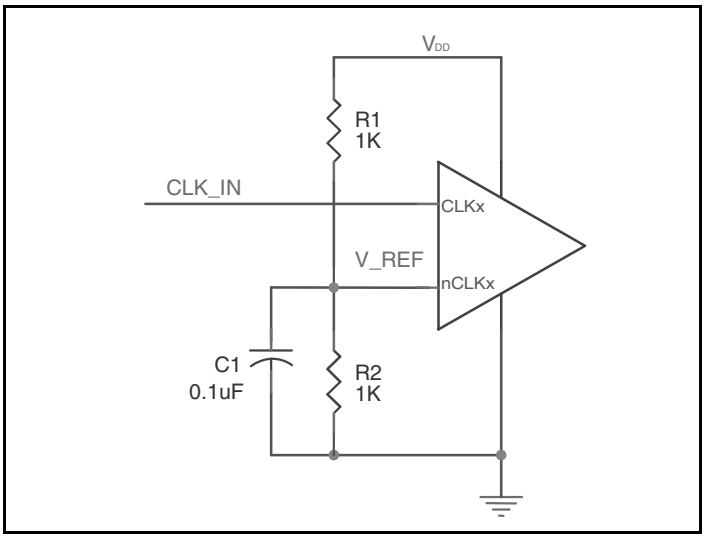


Figure 2. Single-Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

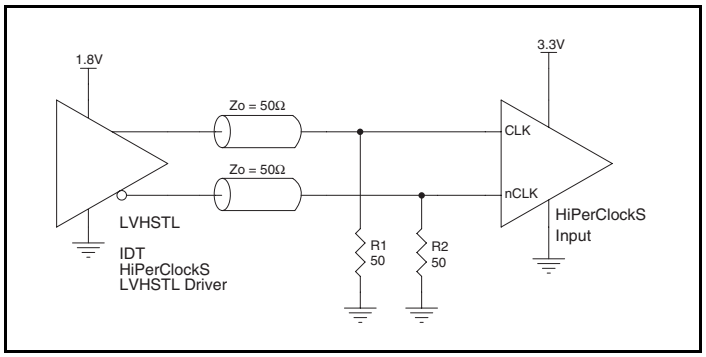


Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

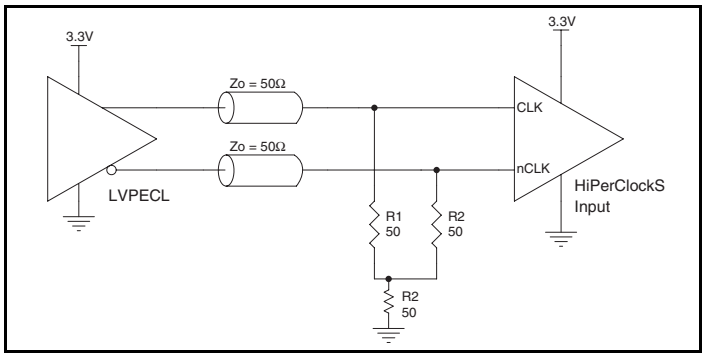


Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

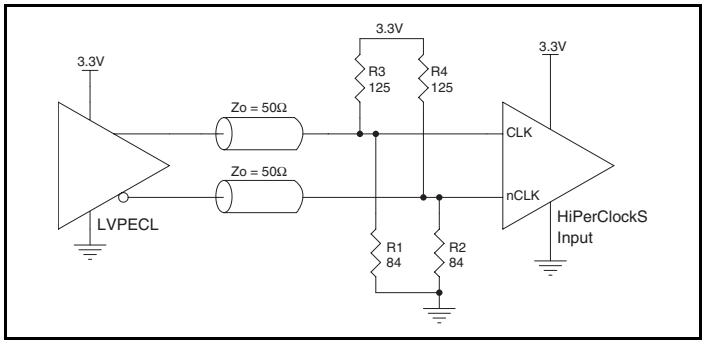


Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

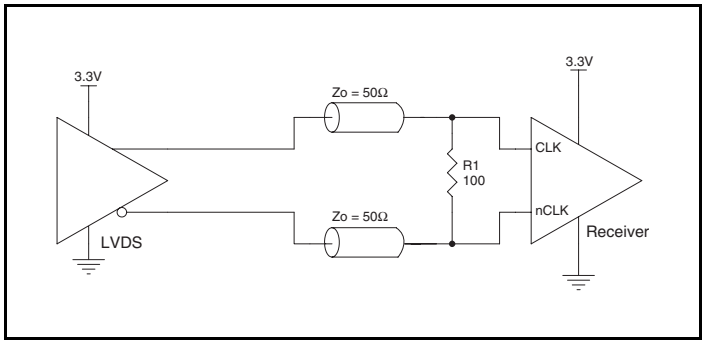


Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

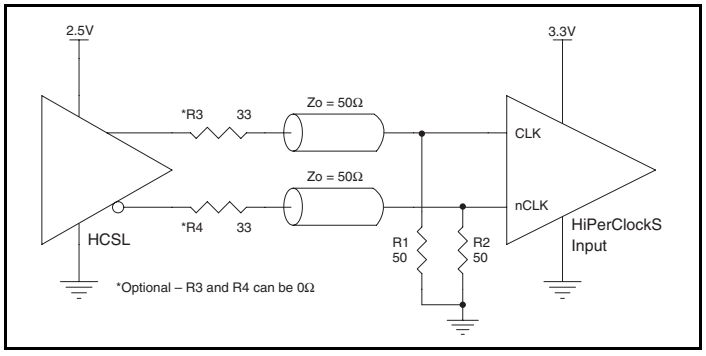


Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

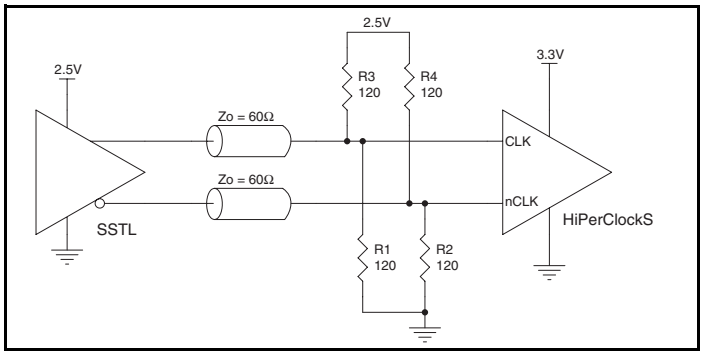


Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

Schematic Example

The schematic of the ICS8624 layout example is shown in *Figure 4A.* The ICS8624 recommended PCB board layout for this example is shown in *Figure 4B.* This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stack up of the P.C. board.

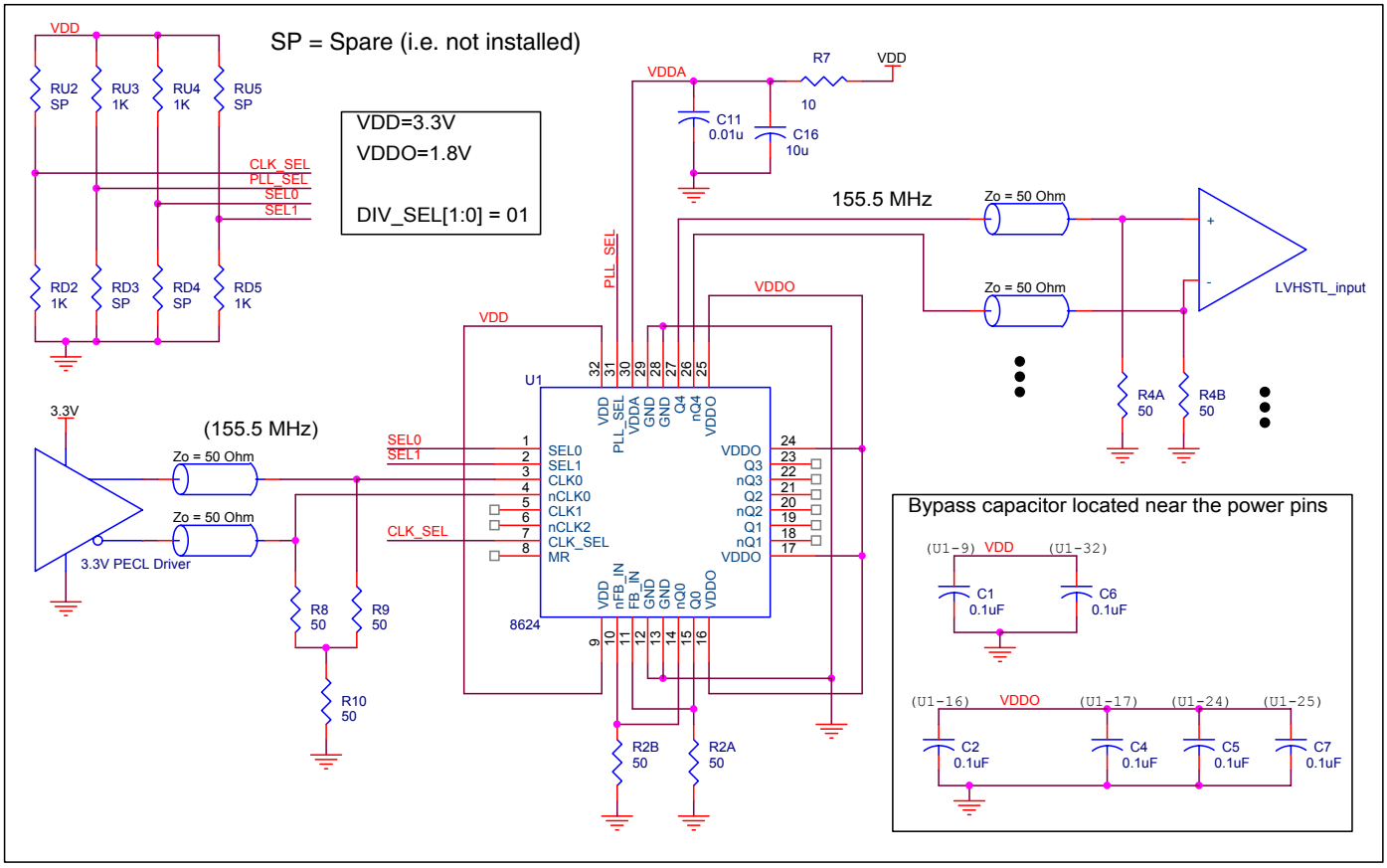


Figure 4A. ICS8624 HSTL Zero Delay Buffer Schematic Example

The following component footprints are used in this layout example: All the resistors and capacitors are size 0603.

Power and Grounding

Place the decoupling capacitors C1, C6, C2, C4, and C5, as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the V_{DDA} pin as possible.

Clock Traces and Termination

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.

The matching termination resistors should be located as close to the receiver input pins as possible.

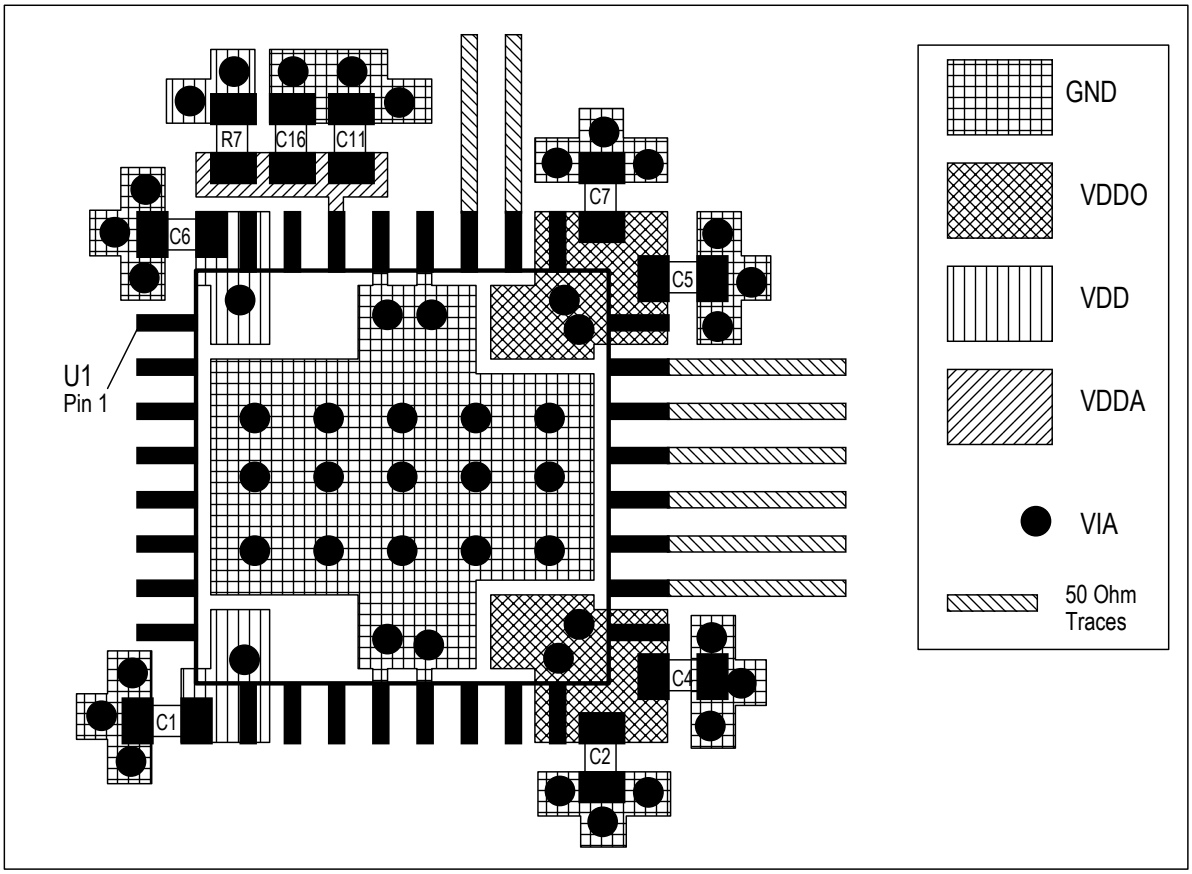


Figure 4B. PCB Board Layout for ICS8624

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8624.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8624 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$= 3.465V * (120mA + 15mA) = **467.775mW**
- Power $(outputs)_{MAX}$ = **32.8mW/Loaded Output pair**
  If all outputs are loaded, the total power is 5 * 32.8mW = **164mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 467.775mW + 164mW = **631.775mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 47.9°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.632W * 47.9°C/W = 100.3°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32 Lead LQFP, Forced Convection

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the HSTL output pairs.

HSTL output driver circuit and termination are shown in *Figure 5.*

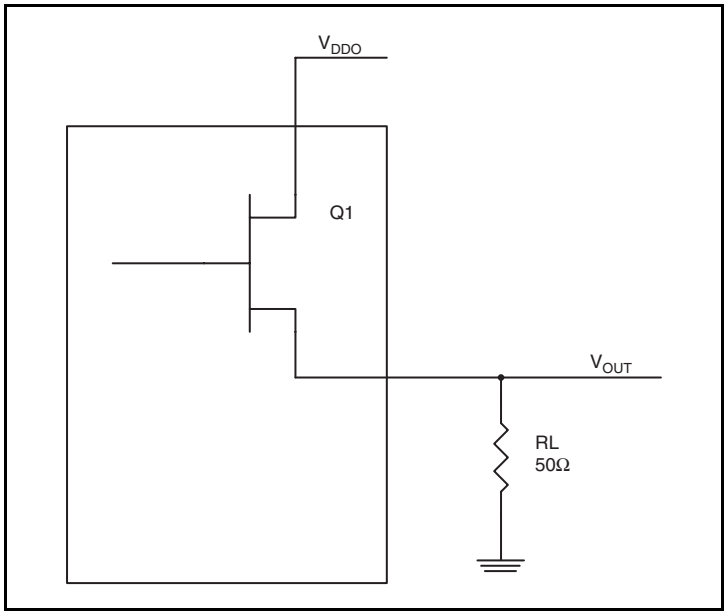


Figure 5. HSTL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = (V_{OH\_MAX}/R_L) * (V_{DDO\_MAX} - V_{OH\_MAX})$

$Pd\_L = (V_{OL\_MAX}/R_L) * (V_{DDO\_MAX} - V_{OL\_MAX})$

Pd_H = (1V/50Ω) * (2V – 1V) = **20mW**

Pd_L = (0.4V/50Ω) * (2V – 0.4V) = **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32.8mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 32 Lead LQFP

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

Transistor Count

The transistor count for ICS8624 is: 1565

Package Outline and Dimensions

Package Outline - Y Suffix for 32 Lead LQFP

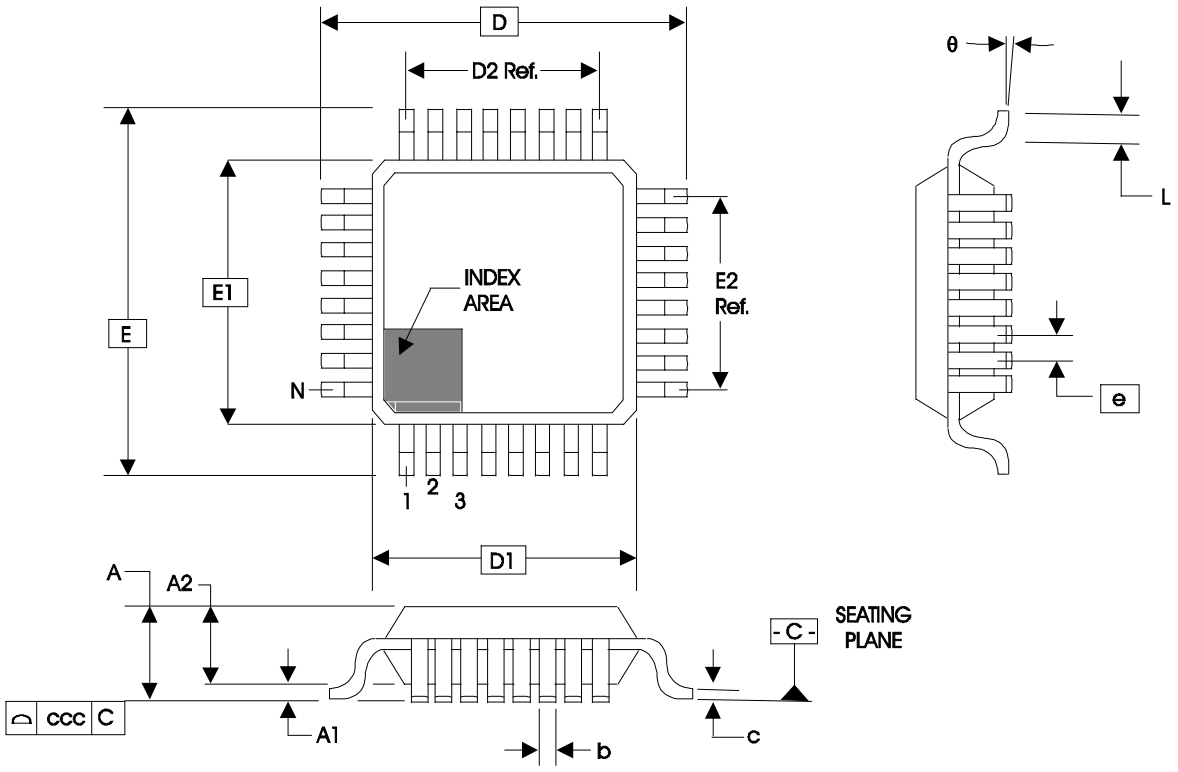


Table 9. Package Dimensions for 32 Lead LQFP

JEDEC Variation: BBA All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
D2 & E2		5.60 Ref.	
e		0.80 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8624BY	ICS8624BY	32 Lead LQFP	Tray	0°C to 70°C
8624BYT	ICS8624BY	32 Lead LQFP	1000 Tape & Reel	0°C to 70°C
8624BYLF	ICS8624BYLF	“Lead-Free” 32 Lead LQFP	Tray	0°C to 70°C
8624BYLFT	ICS8624BYLF	“Lead-Free” 32 Lead LQFP	1000 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		8 10	Switched labels on Figure 8, odc & t_{PERIOD} diagram. Revised label on Figure 11 to read ICS8624 LVHSTL... from ICS8634 LVDS...	10/30/01
A		1	Revised Block Diagram.	10/31/01
A		7 - 8 11 - 12	Updated Phase Jitter Diagram and Output Rise & Fall Time Diagram. Revised Figures 3A & 3B.	8/13/02
B	T1 T4A T4C	2 4 4 9	Pin Description table - revised MR & V_{DD} descriptions. Power Supply table - revised V_{DD} parameter description to correspond with the Pin Description table. Differential DC Charc. table - changed V_{PP} limit from 0.15V minimum to 0.1V minimum. Revised Single Ended Signal diagram. Updated format.	2/12/03
C	T2 T4D T6B	3 4 5 5	Pin Characteristics Table - changed C_{IN} 4pF max. to 4pF typical. Absolute Maximum Ratings - updated Output rating. HSTL DC Characteristics Table - changed V_{OX} to 40% min. - 60% max. and added note. Added Table 6B AC Characteristics Table with $V_{DD} = V_{DDA} = 3.3V±10\%$. Changed LVHSTL to HSTL throughout the data sheet.	2/19/04
C	 T10	8 14	Added Differential Clock Input Interface section. Added ""Lead Free"" part number to Ordering Information table.	6/15/04
D	T6A T10	5 14	AC Characteristics Table -adjusted T_{PD} spec from 3.4ns Min. to 3.2ns Min. and deleted the typical spec. Ordering Information Table - added Lead-Free note.	6/27/05
E	T4A T4C T6A T6C	4 5 6 6 9 10 13 17	Power Supply DC Characteristics Table - changed V_{DDO} min. from 1.6V to 1.5V. Updated Table Header to match change. Differential DC Characteristics Table - updated NOTES 1 & 2. Added Thermal note. Added 1.5V to 1.6V AC Characteristics Table. Added *Recommendations for Unused Input & Output Pins* section. Updated *Differential Clock Input Interface* section. Power Considerations - updated Power Dissipation calculation. Ordering Information Table - deleted “ICS” prefix from Part/Order Number column. Converted datasheet format.	10/6/09

www.IDT.com

6024 Silver Creek Valley Road
San Jose, California 95138

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

Technical Support
netcom@idt.com
+480-763-2056