

General Description

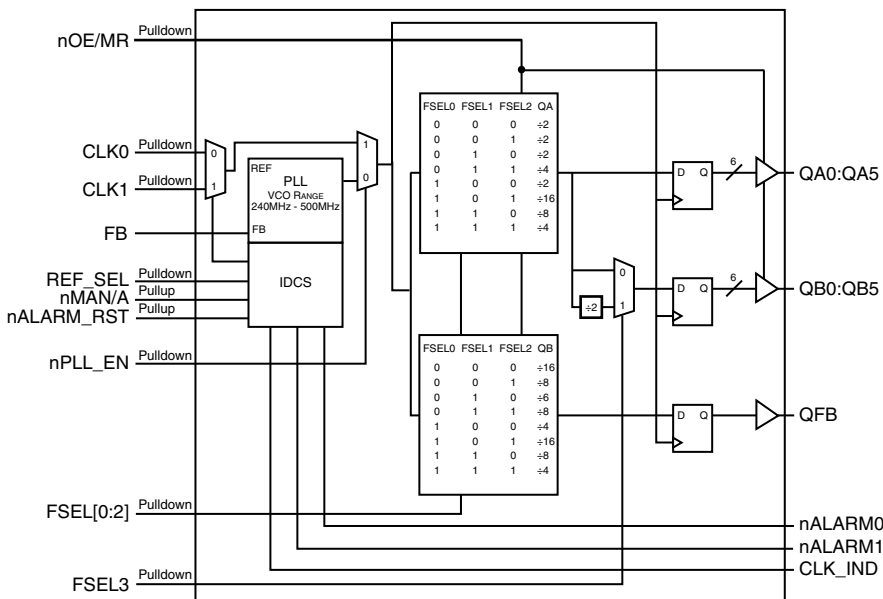
The 879893 is a PLL clock driver designed specifically for redundant clock tree designs. The device receives two LVCMOS/LVTTL clock signals from which it generates 12 new LVCMOS/LVTTL clock outputs. External PLL feedback is used to also provide zero delay buffer performance.

The 879893 Intelligent Dynamic Clock Switch (IDCS) circuit continuously monitors both input CLK signals. Upon detection of a failure (CLK stuck HIGH or LOW for at least 1 period), the nALARM for that CLK will be latched (LOW). If that CLK is the primary clock, the IDCS will switch to the good secondary clock and phase/frequency alignment will occur with minimal output phase disturbance.

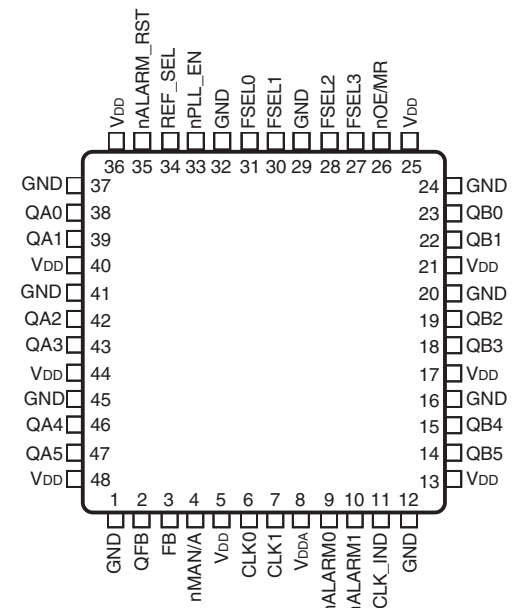
Features

- Twelve LVCMOS/LVTTL outputs (two banks of six outputs); One QFB feedback clock output
- Selectable CLK0 or CLK1 LVCMOS/LVTTL clock inputs
- CLK0, CLK1 supports the following input types: LVCMOS, LVTTL
- Automatically detects clock failure
- IDCS on-chip intelligent dynamic clock switch
- Maximum output frequency: 200MHz
- Output skew: 50ps (maximum), within bank
- Cycle-to-cycle (FSEL3=0, $V_{DD}=3.3V\pm5\%$): 150ps (maximum)
- Smooth output phase transition during clock fail-over switch
- Full 3.3V or 2.5V supply modes
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- **For functional replacement part use 87973i**

Simplified Block Diagram



Pin Assignment



879893

48-Lead LQFP

7mm x 7mm x 1.4mm package body

Y Package

Top View

Block Diagram

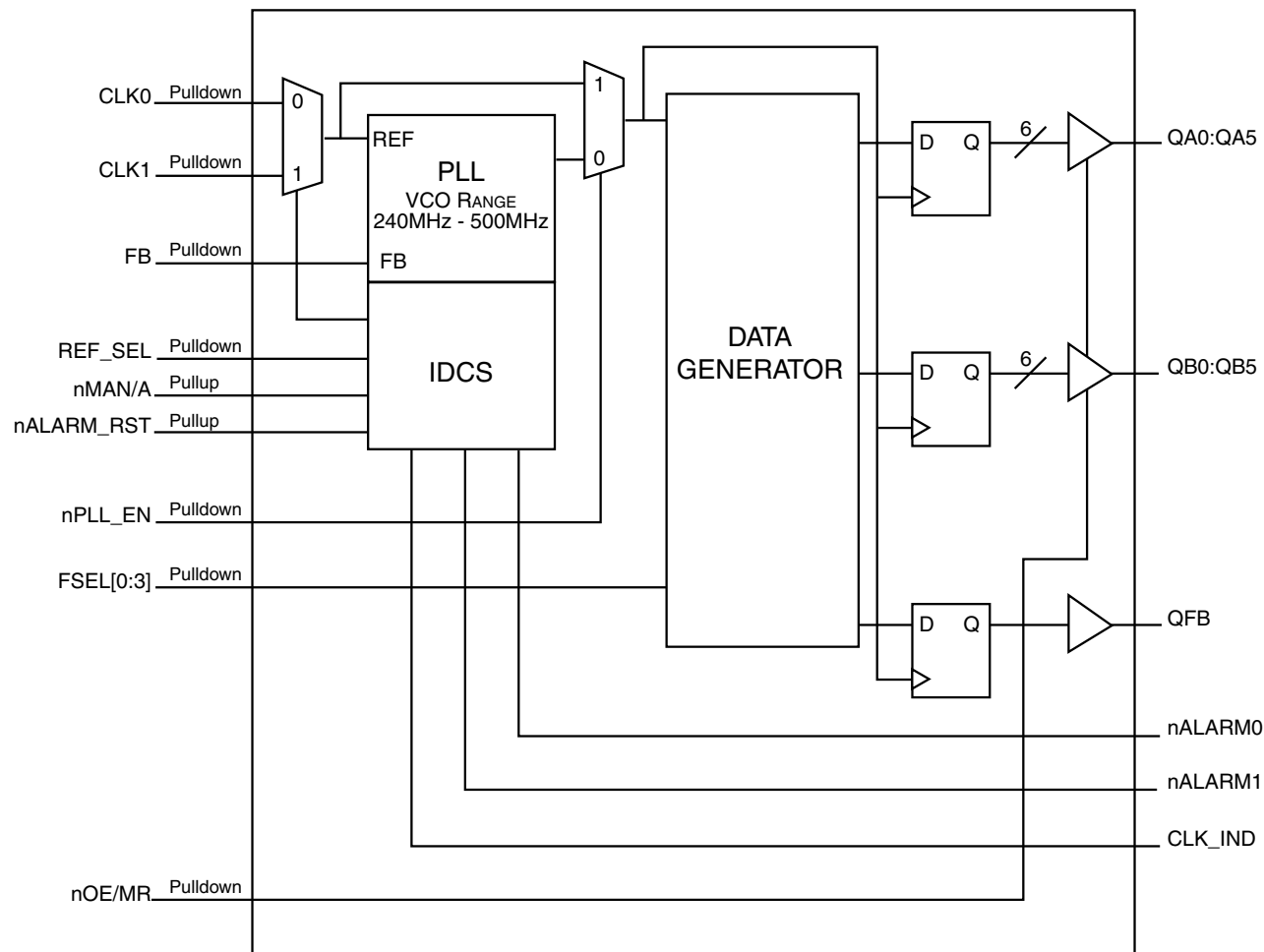


Table 1. Pin Descriptions

Number	Name	Type		Description
1, 12, 16, 20, 29, 32, 37, 41, 45	GND	Power		Power supply ground.
2	QFB	Output		Clock feedback output. LVCMOS / LVTTTL interface levels.
3	FB	Input	Pulldown	Feedback control input. LVCMOS / LVTTTL interface levels.
4	nMAN/A	Input	Pullup	Manual alarm input. Selects automatic switch mode or manual reference clock. Clock failure detection, and nALARM_RST and CLK_IND output flags are enabled. When LOW, IDCS is disabled. When HIGH, IDCS is enabled. IDCS overrides REF_SEL on a clock failure. IDCS operation requires nPLL_EN = 0. LVCMOS / LVTTTL interface levels.
5, 13, 17, 21, 25, 36, 40, 44, 48	V _{DD}	Power		Core supply pins.
6, 7	CLK0, CLK1	Input	Pulldown	Single-ended clock inputs. LVCMOS/LVTTTL interface levels.
8	V _{DDA}	Power		Analog supply pin.
9	nALARM0	Output		When LOW, indicates clock failure on CLK0. LVCMOS / LVTTTL interface levels.
10	nALARM1	Output		When LOW, indicates clock failure on CLK1. LVCMOS / LVTTTL interface levels.
11	CLK_IND	Output		Indicates currently selected input reference clock. When LOW, CLK0 is the reference clock. When HIGH, CLK1 is the reference clock. LVCMOS / LVTTTL interface levels.
14, 15, 18, 19, 22, 23	QB5, QB4, QB3, QB2, QB1, QB0	Output		Single-ended Bank B clock outputs. LVCMOS/LVTTTL interface levels.
26	nOE/MR	Input	Pulldown	Active High Master Reset. Active Low Output Enable. When logic LOW, the internal dividers and the outputs are enabled. When logic HIGH, the internal dividers are reset and the outputs are in a high-impedance state. LVCMOS / LVTTTL interface levels.
27, 28, 30, 31	FSEL3, FSEL2, FSEL1, FSEL0	Input	Pulldown	Clock frequency selection and configuration of clock divider modes. LVCMOS / LVTTTL interface levels.
33	nPLL_EN	Input	Pulldown	Selects PLL or static test mode. When LOW, PLL is enabled. When HIGH, PLL is bypassed and IDCS is disabled. The VCO output is replaced by the reference clock signal fREF. LVCMOS / LVTTTL interface levels.
34	REF_SEL	Input	Pulldown	Selects the primary reference clock. When LOW, selects CLK0 as the primary clock source. When HIGH, selects CLK1 as the primary clock source. LVCMOS / LVTTTL interface levels.
35	nALARM_RST	Input	Pullup	Resets the alarm flags and selected reference clock. LVCMOS / LVTTTL interface levels.
38, 39 42, 43, 46, 47	QA0, QA1, QA2, QA3, QA4, QA5	Output		Single-ended Bank A clock outputs. LVCMOS/LVTTTL interface levels.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance	$V_{DD} = 3.465V$		9		pF
		$V_{DD} = 2.625V$		9		pF
R_{PULLUP}	Input Pullup Resistor			51		k Ω
$R_{PULLDOWN}$	Input Pulldown Resistor			51		k Ω
R_{OUT}	Output Impedance			14		Ω

Function Tables**Table 3. Clock Frequency Function Table**

Inputs				f_{REF} Range (MHz)	Outputs				
FSEL0	FSEL1	FSEL2	FSEL3		Ratio	fQA _x (MHz)	Ratio	fQB _x (MHz)	QFB
0	0	0	0	15 – 25	$f_{REF} * 8$	120 – 200	$f_{REF} * 8$	120 – 200	f_{REF}
0	0	0	1				$f_{REF} * 4$	60 – 100	f_{REF}
0	0	1	0	30 – 50	$f_{REF} * 4$	120 – 200	$f_{REF} * 4$	120 – 200	f_{REF}
0	0	1	1				$f_{REF} * 2$	60 – 100	f_{REF}
0	1	0	0	40 – 66.66	$f_{REF} * 3$	120 – 200	$f_{REF} * 3$	120 – 200	f_{REF}
0	1	0	1				$f_{REF} * 3 \div 2$	60 – 100	f_{REF}
0	1	1	0	30 – 62.5	$f_{REF} * 2$	60 – 125	$f_{REF} * 2$	60 – 125	f_{REF}
0	1	1	1				$f_{REF} * 1$	30 – 75	f_{REF}
1	0	0	0	60 – 100	$f_{REF} * 2$	120 – 200	$f_{REF} * 2$	120 – 200	f_{REF}
1	0	0	1				f_{REF}	60 – 100	f_{REF}
1	0	1	0	15 – 31.25	f_{REF}	15 – 31.25	f_{REF}	15 – 31.25	f_{REF}
1	0	1	1				$f_{REF} \div 2$	7.5 – 15.62	f_{REF}
1	1	0	0	30 – 62.5	f_{REF}	30 – 62.5	f_{REF}	20 – 62.5	f_{REF}
1	1	0	1				$f_{REF} \div 2$	15 – 31.25	f_{REF}
1	1	1	0	60 – 100	f_{REF}	60 – 100	f_{REF}	60 – 100	f_{REF}
1	1	1	1				$f_{REF} \div 2$	30 – 50	f_{REF}

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, V_O	-0.5V to $V_{DD} + 0.5V$
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				195	mA
I_{DDA}	Analog Supply Current				13	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				173	mA
I_{DDA}	Analog Supply Current				13	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{DD} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		$V_{DD} = 3.465V$	2		$V_{DD} + 0.3$	V
			$V_{DD} = 2.625V$	1.7		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	FSEL[0:3], FB, nOE/MR, nMAN/A, nALARM_RST[0:1], nPLL_EN, REF_SEL	$V_{DD} = 3.465V$	-0.3		0.8	V
		FSEL[0:3], FB, nOE/MR, nMAN/A, nALARM_RST, nPLL_EN, REF_SEL	$V_{DD} = 2.625V$	-0.3		0.7	V
		CLK0, CLK1	$V_{DD} = 3.465V$ or $2.625V$	-0.3		1.3	V
I_{IH}	Input High Current	nMAN/A, nALARM_RST	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			5	μA
		CLK0, CLK1, FB, nOE/MR, FSEL[0:3], nPLL_EN, REF_SEL	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			200	μA
I_{IL}	Input Low Current	nMAN/A, nALARM_RST	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-200			μA
		CLK0, CLK1, FB, nOE/MR, FSEL[0:3], nPLL_EN, REF_SEL	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5			μA
V_{OH}	Output High Voltage		$V_{DD} = 3.465V$, $I_{OH} = -24mA$	2.4			V
			$V_{DD} = 2.625V$, $I_{OH} = -15mA$	1.8			V
V_{OL}	Output Low Voltage		$V_{DD} = 3.465V$, $I_{OL} = 24mA$			0.55	V
			$V_{DD} = 3.465V$, $I_{OL} = 12mA$			0.30	V
			$V_{DD} = 2.625V$, $I_{OL} = 15mA$			0.6	V

Unless otherwise noted, outputs terminated with 50Ω to $V_{DD}/2$.

See Parameter Measurement Information section. *Load Test Circuit diagrams.*

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		7.5		200	MHz
f_{REF}	Input Frequency		15		100	MHz
BW	PLL Closed Loop Bandwidth			0.8 to 4		MHz
$t(\emptyset)$	Propagation Delay, (Static Phase Offset, CLKx to FB); NOTE 1, 2, 3	$V_{DD} = 3.3V \pm 5\%$; FSEL = 111x	-35		120	ps
		$V_{DD} = 3.3V \pm 5\%$	-35		130	ps
$t_{sk(o)}$	Output Skew; NOTE 1, 2, 3, 4	within bank			50	ps
		bank-to-bank			135	ps
		any output to QFB			315	ps
Δt	Rate of Period Change; NOTE 2	$f_{REF} = 62.5MHz$, FSEL = 1000			160	ps/cycle
		FSEL = XXX0		100	280	ps/cycle
		FSEL = XXX1		200	425	ps/cycle
jit(cc)	Cycle-to-Cycle Jitter; NOTE 2, 3	FSEL3 = 0			150	ps
		FSEL3 = 1			190	ps
Δt_{CYCLE}	Output Clock Period Deviation when switching from primary input to secondary; NOTE 2	$f_{REF} = 62.5MHz$, FSEL = 1000	-600		700	ps
			-800		800	ps
jit(per)	Period Jitter; NOTE 2, 3	FSEL3 = 0			150	ps
		FSEL3 = 1, measured on QBx			150	ps
$\text{jit}(\emptyset)$	I/O Phase Jitter, (1 σ); NOTE 2, 3	FB = 4; FSEL [0:2] = 100 or 111 (1 σ)			25	ps
		FB = 6; FSEL [0:2] = 010 (1 σ)			25	ps
		FB = 8; FSEL [0:2] = 001, 011 or 110 (1 σ)			35	ps
		FB = 16; FSEL [0:2] = 000 or 101 (1 σ)			25	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		600	ps
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 2				10	ns
t_{PLZ}, t_{PHZ}	Output Disable Time; NOTE 2				10	ns
t_L	PLL Lock Time; NOTE 2				10	ms
odc	Output Duty Cycle		45	50	55	%

All parameters measured at f_{MAX} unless noted otherwise.

NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal, when the PLL is locked and the input reference frequency is stable.

NOTE 2: These parameters are guaranteed by characterization. Not tested in production.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DD}/2$.

Table 5B. AC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		7.5		200	MHz
f_{REF}	Input Frequency		15		100	MHz
BW	PLL Closed Loop Bandwidth			0.8 to 4		MHz
$t(\phi)$	Propagation Delay, (Static Phase Offset, CLKx to FB); NOTE 1, 2, 3	$V_{DD} = 3.3V \pm 5\%$; FSEL = 111x	-55		120	ps
		$V_{DD} = 3.3V \pm 5\%$	-55		130	ps
$t_{sk(o)}$	Output Skew; NOTE 1, 2, 3, 4	within bank			50	ps
		bank-to-bank			135	ps
		any output to QFB			280	ps
Δt	Rate of Period Change; NOTE 2	$f_{REF} = 62.5MHz$, FSEL = 1000			175	ps/cycle
		FSEL = XXX0			260	ps/cycle
		FSEL = XXX1			350	ps/cycle
$f_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 2, 3	FSEL3 = 0			180	ps
		FSEL3 = 1			245	ps
Δt_{CYCLE}	Output Clock Period Deviation when switching from primary input to secondary; NOTE 2	$f_{REF} = 62.5MHz$, FSEL = 1000	-600		700	ps
			-800		850	ps
$f_{jit(per)}$	Period Jitter; NOTE 2, 3	FSEL3 = 0			150	ps
		FSEL3 = 1, measured on QBx			150	ps
$f_{jit(\phi)}$	I/O Phase Jitter, (1σ) ; NOTE 2, 3	FB = 4; FSEL [0:2] = 100 or 111 (1σ)			30	ps
		FB = 6; FSEL [0:2] = 010 (1σ)			40	ps
		FB = 8; FSEL [0:2] = 001, 011 or 110 (1σ)			25	ps
		FB = 16; FSEL [0:2] = 000 or 101 (1σ)			30	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		600	ps
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 2				10	ns
t_{PLZ}, t_{PHZ}	Output Disable Time; NOTE 2				10	ns
t_L	PLL Lock Time; NOTE 2				10	ms
odc	Output Duty Cycle		45	50	55	%

All parameters measured at f_{MAX} unless noted otherwise.

NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal, when the PLL is locked and the input reference frequency is stable.

NOTE 2: These parameters are guaranteed by characterization. Not tested in production.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DD}/2$.

The diagram shows a differential signal source represented by a triangle. The top input is labeled $1.65V \pm 5\%$ and the bottom input is labeled $-1.65V \pm 5\%$. The top input is also labeled V_{DD}, V_{DDA} and the bottom input is labeled GND . The output of the source is connected to a transmission line, represented by a thick black cylinder, which is labeled $Z = 50\Omega$. The output of the transmission line is labeled Qx and is connected to a scope, represented by a rectangle labeled $SCOPE$. The scope input is connected to a 50Ω resistor, which is connected to ground.

The diagram shows a differential signal source represented by a triangle. The top input is labeled $1.25V \pm 5\%$ and the bottom input is labeled $-1.25V \pm 5\%$. The top input is also labeled V_{DD}, V_{DDA} and the bottom input is labeled GND . The output of the source is connected to a transmission line, represented by a thick black bar, which is labeled $Z = 50\Omega$. The transmission line is connected to a box labeled **SCOPE**. The connection point on the transmission line is labeled Qx . A 50Ω resistor is connected between the Qx point and ground.

The diagram shows two digital signals, Qx and Qy, plotted against time. Both signals follow the same logic sequence: a low-to-high transition, a high-to-low transition, and a low-to-high transition. The signal Qx is the reference, and Qy is delayed relative to it. A vertical dashed line marks the rising edge of Qx. A horizontal double-headed arrow between this line and the rising edge of Qy is labeled $tsk(0)$, representing the setup time delay. A horizontal tick mark on the Qy signal indicates the voltage level $\frac{V_{DD}}{2}$.

The diagram shows two digital signals, QA[0:5] and QB[0:5], over time. The signals are represented by a single line that transitions between high and low states. Vertical lines mark the start and end of two consecutive clock cycles, labeled $tcycle\ n$ and $tcycle\ n+1$. The jitter $fjit(cc)$ is defined as the absolute difference between the durations of these two cycles, normalized by 1000 Cycles.

$$fjit(cc) = \frac{|tcycle\ n - tcycle\ n+1|}{1000\ Cycles}$$

The diagram shows three signals: CLK0, CLK1, and FB. CLK0 and CLK1 are square waves with voltage levels V_{OH} and V_{OL} . FB is a signal that transitions from V_{OL} to V_{OH} at a specific time $t(O)$. The diagram illustrates the phase jitter and static phase offset.

$$jit(\varnothing) = |t(\varnothing) - t(\varnothing) \text{ mean}| = \text{Phase Jitter}$$

$$t(\varnothing) \text{ mean} = \text{Static Phase Offset and I/O Phase Jitter}$$

Where $t(\varnothing)$ is any random sample, and $t(\varnothing) \text{ mean}$ is the average of the sampled cycles measured on the controlled edges

The diagram illustrates a signal transition from a low state to a high state. A dashed horizontal line represents the reference voltage V_{REF} . The signal starts at a low level, rises to a high level V_{OH} , and then falls back to the low level. A vertical dashed line marks the "Reference Point (Trigger Edge)" at the start of the rising edge. A histogram is shown for the "Mean Period (First edge after trigger)", which is the time interval from the reference point to the first falling edge. The histogram is a bell-shaped curve with a peak at the mean period. The signal levels are labeled V_{OH} and V_{REF} .

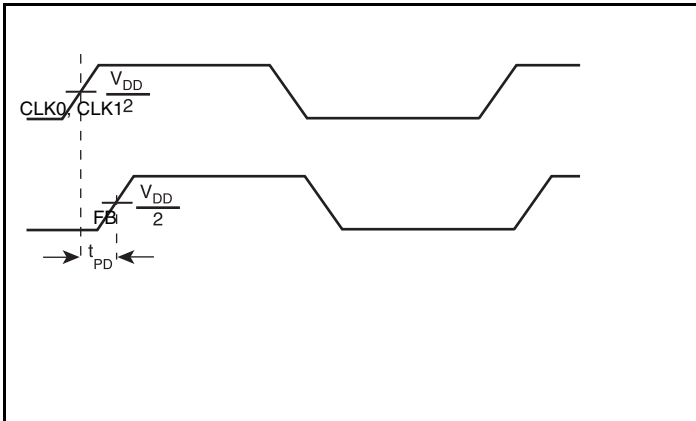
1 σ contains 68.26% of all measurements
 2 σ contains 95.4% of all measurements
 3 σ contains 99.73% of all measurements
 4 σ contains 99.99366% of all measurements
 6 σ contains (100-1.973x10⁻⁷)% of all measurements

Reference Point
 (Trigger Edge)

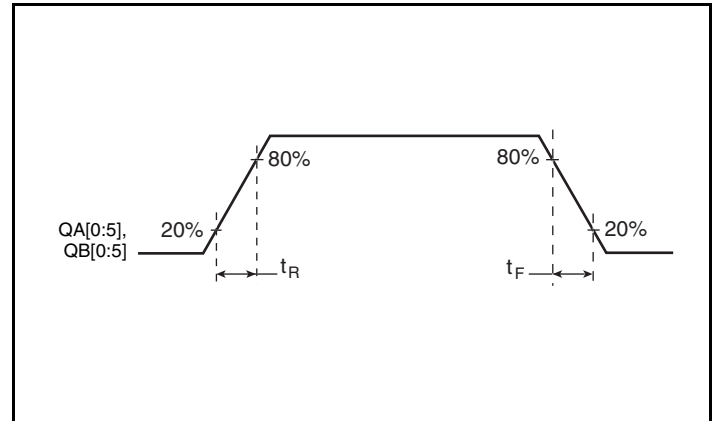
Histogram
 Mean Period
 (First edge after trigger)

LOW SKEW, 1-TO-12 (IDCS) LVCMOS/LVTTL CLOCK GENERATOR

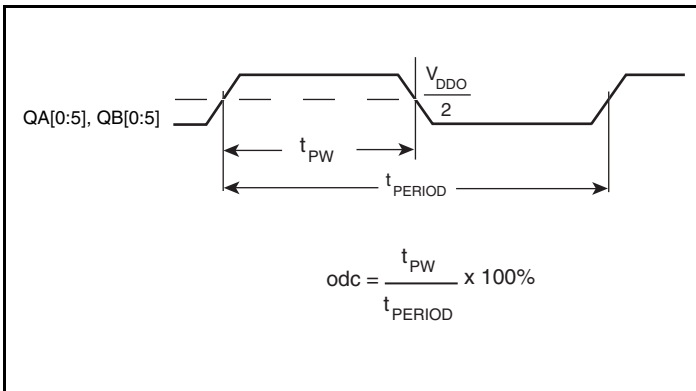
Parameter Measurement Information, continued



Propagation Delay



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Application Information

CLOCK REDUNDANCY AND REFERENCE SELECTION

The 879893 accepts two LVCMOS/LVTTL single ended input clocks, CLK0 and CLK1, for the purpose of redundancy. Only one of these clocks can be selected at any given time for use as the reference. The clock that is used by default as the reference is referred to as the primary clock, while the remaining clock is the redundant or secondary clock. Input signal REF_SEL determines which input is to be used as the primary and which is to be used as the secondary. When REF_SEL is driven HIGH, the primary clock input is CLK1, otherwise an internal pull down pulls this input LOW so that the primary clock input is CLK0. The output signal CLK_IND indicates which clock input is being used as the reference (LOW = CLK0, HIGH = CLK1), and will initially be at the same level as REF_SEL.

FAILURE DETECTION AND ALARM SIGNALING

Within the 879893 device, CLK0 and CLK are continuously monitored for failures. A failure on either of these clocks is detected when one of the clock signals is stuck HIGH or LOW for at least 1 period. Upon detection of a failure, the corresponding alarm signal, nALARM0 or nALARM1, is latched LOW. A HIGH-to-LOW transition on input signal nALARM_RST causes the alarm outputs to be reset HIGH, and the primary clock input is selected as the reference clock. Otherwise, an internal pull-up holds nALARM_RST HIGH, and the IDCS flags remain unchanged. If n_ALARM_RST is asserted when both of the alarm flag outputs are LOW, CLK0 is selected as the reference input. The device's internal PLL is able to maintain phase/frequency alignment, and lock with the input as long as the input used as the reference clock does not fail.

MANUAL CLOCK SWITCHING

When input signal nMAN/A is driven LOW, the primary clock, as selected by REF_SEL, is always used as the reference, even when a clock failure is detected at the reference. In order switch between CLK0 and CLK1 as the primary clock, the level on REF_SEL must be driven to the appropriate level. When the level on REF_SEL is changed, the selection of the new primary clock will take place, and CLK_IND will be updated to indicate which clock is now supplying reference. This process serves as a manual safety mechanism to protect the stability of the PLL when a failure occurs on the reference.

DYNAMIC CLOCK SWITCHING

When input signal nMAN/A is not driven LOW, an internal pull-up pulls it HIGH so that Intelligent Dynamic Clock Switching (IDCS) is enabled. If IDCS is enabled, once a failure occurs on the primary clock, the 879893 device will automatically deselect the primary clock as the reference and multiplex in the secondary clock, but only if it is valid and has no failures. When a successful switch from primary to secondary has been accomplished, CLK_IND will be updated to indicate the new reference. This process serves as an automatic safety mechanism to protect the stability of the PLL when a failure occurs on the reference.

OUTPUT TRANSITIONING

After a successful manual or IDCS initiated clock switch, the 879893's internal PLL will begin slewing to phase/frequency alignment, and will eventually achieve lock with the new input with minimal phase disturbance at the outputs.

MASTER RESET OPERATION

Applying logic HIGH to the nOE/MR input resets the internal dividers of the 879893 and disables the outputs QA0:QA5 and QB0:QB5 in high-impedance state. Logic LOW state at the nOE/MR input enables the outputs and internal dividers.

RECOMMENDED POWER-UP SEQUENCE

1. Hold nOE/MR HIGH, drive nMAN/A LOW, and drive REF_SEL to the desired value during power up in order to reset internal dividers, disable the outputs in high-impedance state (nOE/MR = HIGH), select manual switching mode, and select the primary input clock.
2. Once powered up, assuming a stable clock free of failures is present at the primary input, the PLL will begin phase/frequency slewing as it attempts to achieve lock with the input reference clock.
3. Transition nALARM_RST HIGH-to-LOW to reset nALARM0 and nALARM1 alarm flag outputs.
4. (Optional) Drive nMAN/A HIGH to enable IDCS mode.

ALTERNATE POWER-UP SEQUENCE

If both input clocks are valid before power up, the device may be powered up in IDCS mode.

1. During power up, select the desired primary clock input by REF_SEL and hold nOE/MR at logic HIGH level to reset the internal dividers and to disable the outputs QA0:QA5 and QB0:QB5 in high-impedance state. Logic high level at the nMAN/A input enables the IDCS mode. An internal bias resistor will pull the nMAN/A input to logic high level if nMAN/A is left open.
2. Once powered up, the PLL will begin phase/frequency slewing as it attempts to achieve lock with the input reference clock.
3. Transition nALARM_RST HIGH-to-LOW to reset nALARM0 and nALARM1 alarm flag outputs.

Recommendations for Unused Input and Output Pins

Inputs:

CLK Inputs

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a $1\text{k}\Omega$ resistor can be tied from the CLK input to ground.

LVC MOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A $1\text{k}\Omega$ resistor can be used.

Outputs:

LVC MOS Outputs

All unused LVC MOS output can be left floating. There should be no trace attached.

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 879893 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and $0.01\mu\text{F}$ bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a $10\mu\text{F}$ bypass capacitor be connected to the V_{DDA} pin.

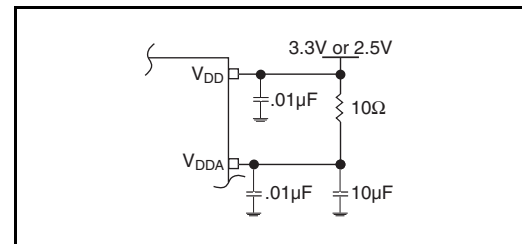


Figure 1. Power Supply Filtering

Schematic Example

Figure 2 shows a schematic example of the 879893. In this example, the CLK1 input is selected as primary. Both CLK0 and CLK1 inputs are driven by LVCMOS drivers. For the LVCMOS outputs, series termination is shown in this example. Additional LVCMOS termination approaches are shown in the LVCMOS Termination Application Note. In this example, feedback trace is assumed to be a long trace. The series termination near the QFB

pin is required. If the feedback trace is short, series termination is not required. If this device is also used as a zero delay buffer, the application note ZDB Delay Affected by Feedback Trace provides additional information. For the power pins, it is recommended to have at least one decoupling capacitor per power pin. The decoupling capacitors should be physically located near the power pins.

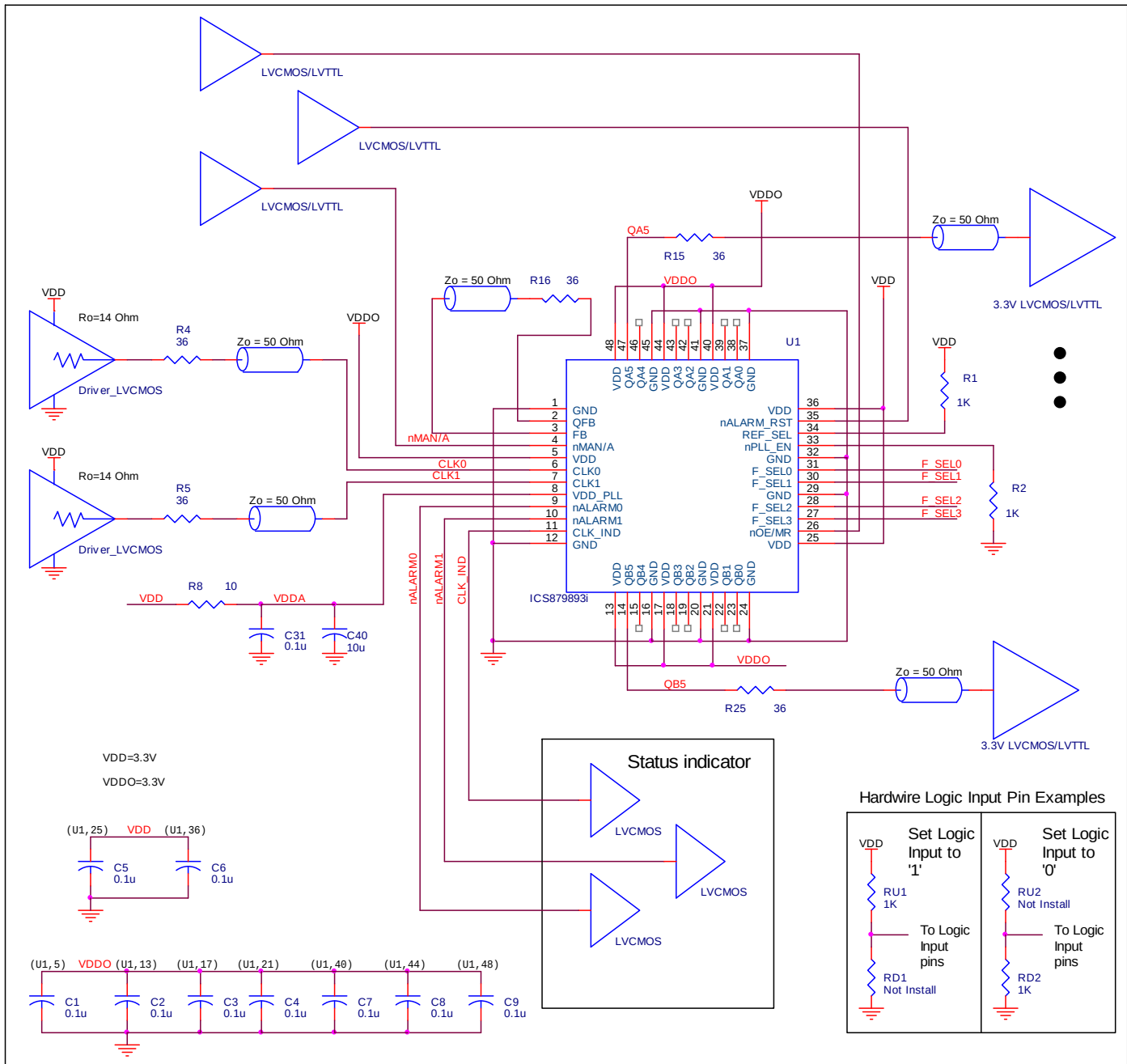


Figure 2. 879893 Schematic Example

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 48 Lead LQFP

θ_{JA} vs. Air Flow			
Linear Feet per Minute	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB design use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for 879893 is: 4615

Pin compatible with MPC9893

Package Outline and Package Dimensions

Package Outline - Y Suffix for 48 Lead LQFP

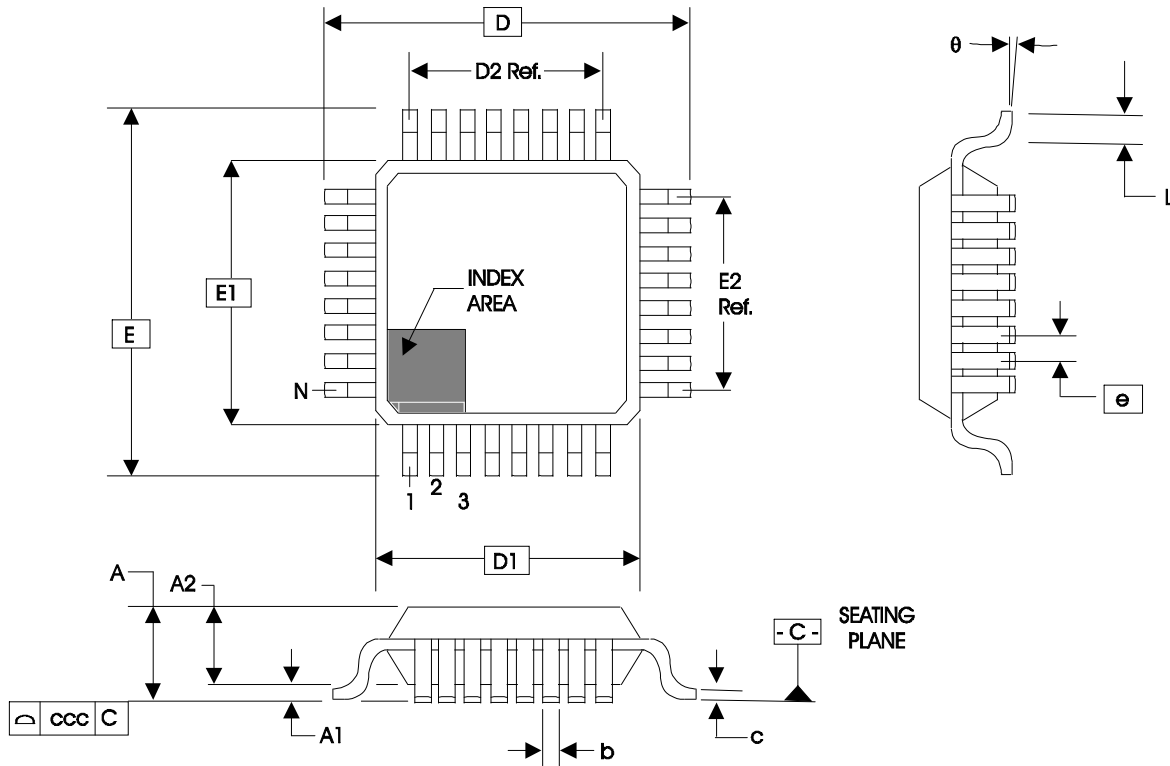


Table 7. Package Dimensions for 48 Lead LQFP

JEDEC Variation: ABC - HD			
All Dimensions in Millimeters			
Symbol	Minimum	Nominal	Maximum
N	48		
A			1.60
A1	0.05	0.10	0.15
A2	1.35	1.4	1.45
b	0.17	0.22	0.27
c	0.09	0.15	0.20
D & E	9.00 Basic		
D1 & E1	7.00 Basic		
D2 & E2	5.50 Ref.		
e	0.50 Basic		
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.08

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
879893AYILF	ICS879893AIL	"Lead-Free" 48 Lead LQFP	Tray	-40°C to 85°C
879893AYILFT	ICS879893AIL	"Lead-Free" 48 Lead LQFP	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		12	Updated Schematic Example text and diagram.	2/10/05
A	T8	1 11 15	Features Section - added lead-free bullet. Added <i>Recommendations for Unused Input and Output Pins</i> and <i>Power Supply Filtering Techniques</i> Sections. Ordering Information Table - added lead-free Part/Order Number, Marking and Note. Updated datasheet format.	7/8/08
A	T8	16	Ordering Information - removed leaded devices. Updated data sheet format.	7/21/15
A		1	Product Discontinuation Notice - Last time buy expires November 2, 2016. PDN# CQ-15-05.	11/6/15



Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com

Tech Support
email: clocks@idt.com

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its subsidiaries reserve the right to modify the products and/or specifications described herein at any time and at IDT's sole discretion. All information in this document, including descriptions of product features and performance, is subject to change without notice. Performance specifications and the operating parameters of the described products are determined in the independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications, such as those requiring extended temperature ranges, high reliability or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Integrated Device Technology, IDT and the IDT logo are registered trademarks of IDT. Product specification subject to change without notice. Other trademarks and service marks used herein, including protected names, logos and designs, are the property of IDT or their respective third party owners.

Copyright ©2015 Integrated Device Technology, Inc.. All rights reserved.