FemtoClock® NG Octal Universal Frequency Translator

IDT8T49N283I

PRELIMINARY SHORT FORM DATA SHEET

This Short Form Data Sheet is intended to provide an overview only. A full-version data sheet is available under NDA. Please contact IDT Sales as indicated on the last page of this document

General Description

The IDT8T49N283I has two independent, fractional-feedback PLLs that can be used as jitter attenuators and frequency translators. It is equipped with six integer and two fractional output dividers, allowing the generation of up to 8 different output frequencies, ranging from 8kHz to 1GHz. Four of these frequencies are completely independent of each other and the inputs. The other four are related frequencies. The eight outputs may select among LVPECL, LVDS, HCSL or LVCMOS output levels.

This makes it ideal to be used in any frequency translation application, including 1G, 10G, 40G and 100G Synchronous Ethernet, OTN, and SONET/SDH, including ITU-T G.709 (2009) FEC rates. The device may also behave as a frequency synthesizer.

The IDT8T49N283I accepts up to two differential or single-ended input clocks and a crystal input. Each of the two internal PLLs can lock to different input clocks which may be of independent frequencies. Each PLL can use the other input for redundant backup of the primary clock, but in this case, both input clocks must be related in frequency.

The device supports hitless reference switching between input clocks. The device monitors all input clocks for Loss of Signal (LOS), and generates an alarm when an input clock failure is detected. Automatic and manual hitless reference switching options are supported. LOS behavior can be set to support gapped or un-gapped clocks.

The IDT8T49N283I supports holdover for each PLL. The holdover has an initial accuracy of ±50ppB from the point where the loss of all applicable input reference(s) has been detected. It maintains a historical average operating point for each PLL that may be returned to in holdover at a limited phase slope.

The device places no constraints on input to output frequency conversion, supporting all FEC rates, including the new revision of ITU-T Recommendation G.709 (2009), most with 0ppm conversion error.

Each PLL has a register-selectable loop bandwidth from 0.5Hz to 512Hz.

Input to output delay can be programmable. External feedback is supported by looping any output back to allow dynamic input to output delay compensation. Each output also supports individual phase delay settings to allow output-output alignment.

The device supports Output Enable inputs and Lock, Holdover and LOS status outputs.

The device is programmable through an I^2C interface. It also supports I^2C master capability to allow the register configuration to be read from an external EEPROM.

Applications

- OTN or SONET / SDH equipment
- Gigabit and Terabit IP switches / routers including Synchronous Ethernet

Features

- Supports SDH/SONET and Synchronous Ethernet clocks including all FEC rate conversions
- Two differential outputs meet jitter limits for 100G Ethernet and STM-256/OC-768
  - <0.3ps RMS (including spurs): 12kHz to 20MHz
  - All outputs <1ps RMS (including spurs) 12kHz to 20MHz
- Operating modes: locked to input signal, holdover and free-run
  - Initial holdover accuracy of ±50ppb
- Accepts up to two LVPECL, LVDS, LVHSTL, HCSL or LVCMOS input clocks
  - Accepts frequencies ranging from 8kHz up to 875MHz
  - Auto and manual input clock selection with hitless switching
  - Clock input monitoring, including support for gapped clocks
- Phase-Slope Limiting and Fully Hitless Switching options to control output phase transients
- Operates from a 10MHz to 40MHz fundamental-mode crystal
- Generates eight LVPECL / LVDS or sixteen LVCMOS output clocks
  - Output frequencies ranging from 8kHz up to 1.0GHz (diff)
  - Output frequencies ranging from 8kHz to 250MHz (LVCMOS)
- Four General Purpose I/O pins with optional support for status & control:
  - Four Output Enable control inputs may be mapped to any of the eight outputs
  - Lock, Holdover & Loss-of-Signal status outputs
- Open-drain Interrupt pin
- Programmable PLL bandwidth settings for each PLL:
  - 0.5Hz, 1Hz, 2Hz, 4Hz, 8Hz, 16Hz, 32Hz, 64Hz, 128Hz, 256Hz or 512Hz
  - Optional Fast Lock function
- Programmable output phase delays in steps as small as 16ps
- Register programmable through I^2C or via external I^2C EEPROM
- Bypass clock paths for system tests
- Full 2.5V or 3.3V supply modes
  V_{CC} / V_{CCA} / V_{CCO}
  3.3V / 3.3V / 3.3V
  3.3V / 3.3V / 2.5V
  2.5V / 2.5V / 3.3V
  2.5V / 2.5V / 2.5V
- Maximum power consumption of 1.8W
- -40°C to 85°C ambient operating temperature
- Package: 56QFN, lead-free (RoHS 6)

Compliance

Supports the requirements of the following standards:

- GR-253-CORE jitter specification for OC-768
- ITU-T G.825 jitter specification for STM-256
- ITU-T G.825 jitter specification for STM-64
- ITU-T G.783

IDT8T49N283i Block Diagram

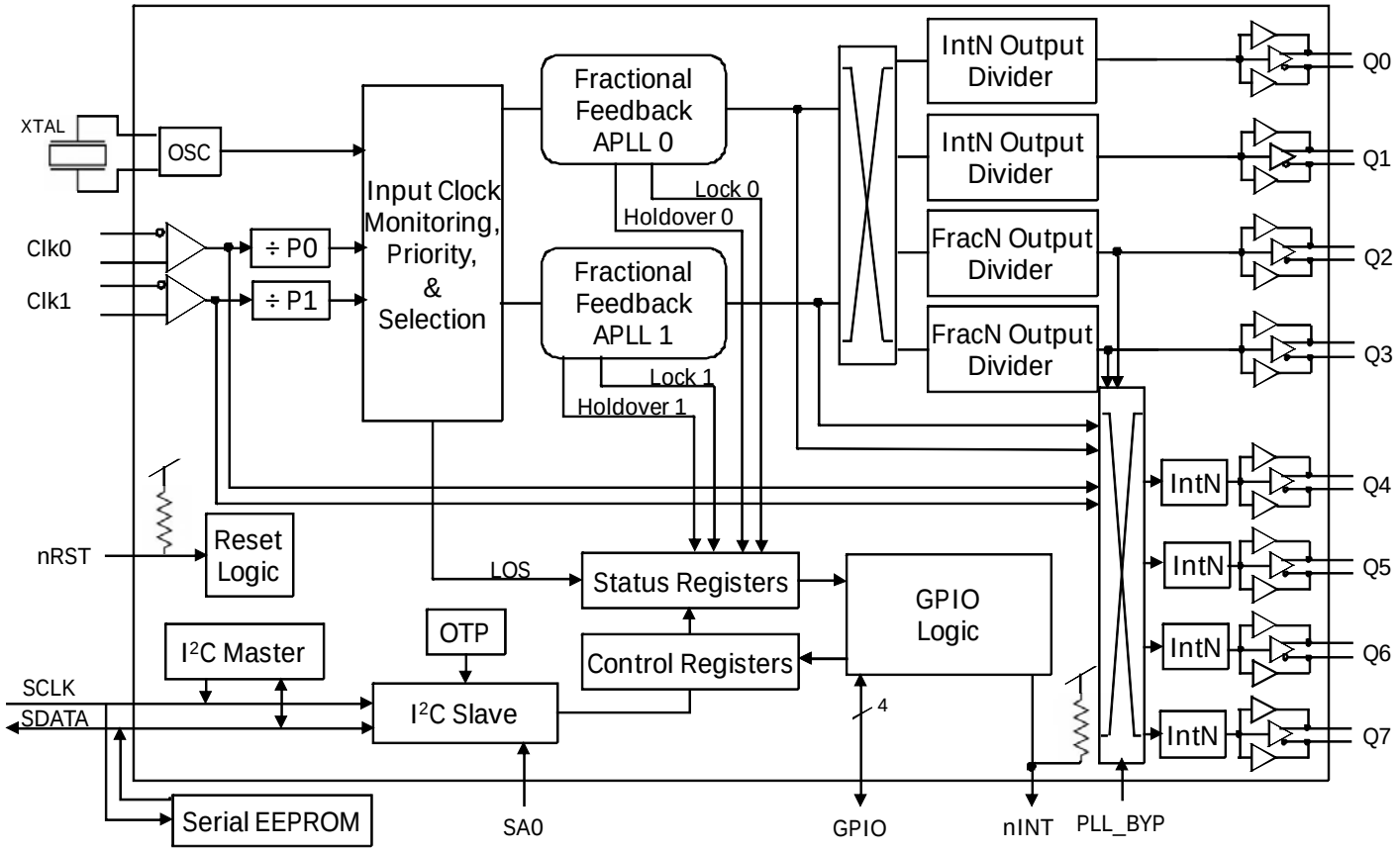


Figure 1: IDT8T49N283i Functional Block Diagram

Principles of Operation

The IDT8T49N283I has two PLLs that can each independently be locked to any of the input clocks and generate a wide range of synchronized output clocks.

It incorporates two completely independent PLLs. These could be used for example in the transmit and receive path of Synchronous Ethernet equipment. Either of the input clocks can be selected as the reference for either PLL. From the output of the two PLLs a wide range of output frequencies can be simultaneously generated.

The IDT8T49N283I accepts up to two differential input clocks ranging from 8kHz up to 875MHz. It generates up to eight output clocks ranging from 8kHz up to 1.0GHz.

Each PLL path within the IDT8T49N283I supports three states: Lock, Holdover and Free-run. Lock & holdover status may be monitored on register bits and pins. Each PLL also supports automatic and manual hitless reference switching. In the locked state, the PLL locks to a valid clock input and its output clocks have a frequency accuracy equal to the frequency accuracy of the input clock. In the Holdover state, the PLL will output a clock which is based on the selected holdover behavior. Each of the PLL paths within the IDT8T49N283I has an initial holdover frequency offset of ±50ppb. In the Free-run state, the PLL outputs a clock with the same frequency accuracy as the external crystal.

Upon power up, each PLL will enter Free-run state, in this state it generates output clocks with the same frequency accuracy as the external crystal. The IDT8T49N283I continuously monitors each input for activity (signal transitions).

In automatic reference switching, when an input clock has been validated the PLL will transition to the locked state. If the selected input clock fails and there are no other valid input clocks, the PLL will quickly detect that and go into holdover. In the Holdover state, the PLL will output a clock which is based on the selected holdover behavior. If the selected input clock fails and another input clock is available then the IDT8T49N283I will hitlessly switch to that input clock. The reference switch can be either revertive or non-revertive.

The device supports conversion of any input frequency to four different, independent output frequencies on the Q[0:3]outputs. Additionally, a further four output frequencies may be generated that are integer-related to the four independent frequencies. These additional four frequencies are on the Q[4:7] outputs.

The IDT8T49N283I has a programmable loop bandwidth from 0.5Hz to 512Hz.

The device monitors all input clocks and generates an alarm when an input clock failure is detected.

The device supports programmable individual output phase adjustments in order to allow control of input to output phase adjustments and output to output phase alignment.

The device is programmable through an I^2C and may also autonomously read its register settings from an internal One-Time Programmable (OTP) memory or an external serial I^2C EEPROM.

Crystal Input

The crystal input on the IDT8T49N283I is capable of being driven by a parallel-resonant, fundamental mode crystal with a frequency range of 10MHz - 40MHz.

The oscillator input also supports being driven by a single-ended crystal oscillator or reference clock.

The initial holdover frequency offset is set by the device, but the long term drift depends on the quality of the crystal or oscillator attached to this port.

Bypass Path

For system test purposes, each of PLL0 and PLL1 may be bypassed. When PLL_BYP is asserted the CLK0 input reference will be presented directly on the Q4 output. The CLK1 input reference will be presented directly on the Q5 output.

Additionally, CLK0 or CLK1 may be used as a clock source for the output dividers of Q4-Q7. This may only be done for input frequencies of 250MHz or less.

Input Clock Selection

The IDT8T49N283I accepts up to two input clocks with frequencies ranging from 8kHz up to 875MHz. Each input can accept LVPECL, LVDS, LVHSTL, HCSL or LVCMOS inputs using 1.8V, 2.5V or 3.3V logic levels.

The device has independent input clock selection control for each PLL. In Manual mode, only one of these inputs may be chosen per PLL and if that input fails that PLL will enter holdover.

Manual mode may be operated by directly selecting the desired input reference in the REFSEL register field. It may also operate via pin-selection of the desired input clock by selecting that mode in the REFSEL register field. In that case, GPIOs must be used as Clock Select inputs (CSELn). CSEL0 = 0 will select the CLK0 input and CSEL0 = 1 will select the CLK1 input for PLL0. CSEL1 will perform the same function for PLL1.

In addition, the crystal frequency may be passed directly to the output dividers for Q[4:7] for use as a reference.

Inputs do not support transmission of spread-spectrum clocking sources. Since this family is intended for high-performance applications, it will assume input reference sources to have stabilities of $\pm$100ppm or better, except where gapped clock inputs are used.

If the PLL is working in automatic mode, then each of the input reference sources is assigned a priority of 1-2. At power-up or if the currently selected input reference fails, the PLL will switch to the highest priority input reference that is valid at that time (see Input Clock Monitor section for details).

Automatic mode has two sub-options: revertive or non-revertive. In revertive mode, the PLL will switch to a reference with a higher priority setting whenever one becomes valid. In non-revertive mode the PLL remains with the currently selected source as long as it remains valid.

The clock input selection is based on the input clock priority set by the Clock Input Priority control registers. If two clocks have the same priority then the lowest clock number will be selected, for instance if CLK0 and CLK1 have the same priority then CLK0 will be selected.

Input Clock Monitor

Each clock input is monitored for Loss of Signal (LOS). If no activity has been detected on the clock input within a user-selectable time period then the clock input is considered to be failed and an internal Loss-of-Signal status flag is set, which may cause an input switchover depending on other settings. The user-selectable time period has sufficient range to allow a gapped clock missing many consecutive edges to be considered a valid input.

User-selection of the clock monitor time-period is based on a counter driven by a monitor clock. The monitor clock is fixed at the frequency of PLL0's VCO divided by 8. With a VCO range of 3GHz - 4GHz, the monitor clock has a frequency range of 375MHz to 500MHz.

The monitor logic for each input reference will count the number of monitor clock edges indicated in the appropriate Monitor Control register. If an edge is received on the input reference being monitored, then the count resets and begins again. If the target edge count is reached before an input reference edge is received, then an internal soft alarm is raised and the count re-starts. During the soft alarm period, the PLL(s) tracking this input will not be adjusted. If an input reference edge is received before the count expires for the second time, then the soft alarm status is cleared and the PLL(s) will resume adjustments. If the count expires again without any input reference edge being received, then a Loss-of-Signal alarm is declared.

It is expected that for normal (non-gapped) clock operation, users will set the monitor clock count for each input reference to be slightly longer than the nominal period of that input reference. A margin of 2-3 monitor clock periods should give a reasonably quick reaction time and yet prevent false alarms.

For gapped clock operation, the user will set the monitor clock count to a few monitor clock periods longer than the longest expected clock gap period. The monitor count registers support 17-bit count values, which will support at least a gap length of two clock periods for any supported input reference frequency, with longer gaps being supported for faster input reference frequencies. Since gapped clocks usually occur on input reference frequencies above 100MHz, gap lengths of thousands of periods can be supported.

Using this configuration for a gapped clock, the PLL will continue to adjust while the normally expected gap is present, but will freeze once the expected gap length has been exceeded. and alarm after twice the normal gap length has passed.

Once a LOS on any of the input clocks is detected, the appropriate internal LOS alarm will be asserted and it will remain asserted until that input clock returns and is validated over a fixed time period (TBD). If another error condition on the same input clock is detected during the validation time then the alarm remains asserted and the validation time starts over.

Each LOS flag may also be reflected on one of the GPIO[3:0] outputs. Changes in status of any reference can also generate an interrupt if not masked.

Holdover

IDT8T49N283I supports a small initial holdover frequency offset for each PLL path in non-gapped clock mode. When the input clock monitor is set to support gapped clock operation, this initial holdover frequency offset is indeterminate since the desired behavior with gapped clocks is for the PLL to continue to adjust itself even if clock edges are missing. In gapped clock mode, the PLL will not enter holdover until the input is missing for two LOS monitor periods.

The holdover performance characteristics of a clock are referred as its accuracy and stability, and are characterized in terms of the fractional frequency offset. The IDT8T49N283I can only control the initial frequency accuracy. Longer-term accuracy and stability are determined by the accuracy and stability of the external oscillator.

When a PLL loses all valid input references, it will enter the holdover state. In non-gapped clock mode, the PLL will initially maintain its most recent frequency offset setting and then transition at a rate dictated by its selected phase-slope limit setting to a frequency offset setting that is based on historical settings.

This behavior is intended to compensate for any frequency drift that may have occurred on the input reference before it was detected to be lost.

The historical holdover value will have three options:

- Return to center of tuning range within the VCO band.
- Instantaneous mode - the holdover frequency will use the DPLL current frequency 100msec before it entered holdover. The accuracy is shown in the AC Table.
- Fast average mode - an internal IIR (Infinite Impulse Response) filter is employed to get the frequency offset. The IIR filter gives a 3 dB attenuation point corresponding to a nominal period of 20 minutes. The accuracy is shown in the AC Table.

When entering holdover, each PLL will set a separate internal HOLD alarm internally. This alarm may be read from internal status register, appear on the appropriate GPIO pin and/or assert the nINT output.

While a PLL is in holdover, its frequency offset is now relative to the crystal input and so the output clocks derived from that PLL will be tracing their accuracy to the local oscillator or crystal. At some point in time, depending on the stability & accuracy of that source, the clock(s) derived from that PLL will have drifted outside of the limits of the holdover state and be considered to be in a free-run state. Since this borderline is defined outside the PLL and dictated by the accuracy and stability of the external local crystal or oscillator, the IDT8T49N283I cannot know or influence when that transition occurs.

Input to Output Clock Frequency

The IDT8T49N283I is designed to accept any frequency in its input range and generate eight different output frequencies that are independent from each other and from the input frequencies. The internal architecture of the device ensures that most such translations will result in the exact output frequency specified. Where exact frequency translation is not possible, the frequency translation error will be minimized.Please contact IDT for configuration software or other assistance in determining if a desired configuration will be supported exactly.

Synthesizer Mode Operation

The device may also act as a frequency synthesizer with either or both PLL's generating their operating frequency from just the crystal input. By setting the SYN_MODEn register bit and setting the STATEn[1:0] field to Freerun, no input clock references are required to generate the desired output frequencies.

Loop Filter and Bandwidth

The IDT8T49N283I uses no external components to support a range of loop bandwidths: 0.5Hz, 1Hz, 2Hz, 4Hz, 8Hz, 16Hz, 32Hz, 64Hz, 128Hz, 256Hz or 512Hz. Each PLL shall support separate loop filter settings.

The device supports three different loop bandwidth settings for each PLL: acquisition, locked and tight-locked. These loop bandwidths are selected from the list of options described above. If enabled, the acquisition bandwidth is used while lock is being acquired to allow the PLL to `fast-lock'. Once locked the PLL will use the locked bandwidth setting. If the acquisition bandwidth setting is not used, the PLL will use the locked bandwidth setting at all times. The tight-locked setting may be used to lower phase noise in situations where the input reference only varies within a very narrow, register-programmed range.

Output Dividers and Mapping to PLLs

The IDT8T49N283I will support eight output dividers that may be mapped to either PLL. Six of the output dividers will have IntN capability only (see Table 1) and the other two will support FracN division.

Integer Output Divider Programming (Q0, Q1, Q[4:7] only)

Each integer output divider block consists of two divider stages in a series to achieve the desired total output divider ratio. The first stage divider may be set to divide by 4, 5 or 6. The second stage of the divider may be bypassed (i.e. divide-by-1) or programmed to any even divider ratio from 2 to 131,070. The total divide ratios, settings and possible output frequencies are shown in Table 3.

In addition, the first divider stage for the Q4-Q7 outputs supports a bypass (i.e. divide-by-1) operation for some clock sources.

Table 1. Q0-Q1, Q4-Q7 Output Divide Ratios

1st-Stage Divide	2nd-Stage Divide	Total Divide	Minimum F_{OUT} MHz	Maximum F_{OUT} MHz
4	1	4	750	1000
5	1	5	600	800
6	1	6	500	666.7
4	2	8	375	500
5	2	10	300	400
6	2	12	250	333.3
4	4	16	187.5	250
5	4	20	150	200
6	4	24	125	166.7
...				
4	131,070	524,280	0.0057	0.0076
5	131,070	655,350	0.0046	0.0061
6	131,070	786,420	0.0038	0.0051

Note: Above ranges for Q[4:7] apply when driven directly from PLL0 or PLL1.

Fractional Output Divider Programming (Q2, Q3 only)

For the FracN output dividers Q2-Q3, the output divide ratio is given by:

Output Divide Ratio = (N.F)x2

N = Integer Part: 4, 5, ...$(2^{18}-1)$

F = Fractional Part: [0, 1, 2, ...$(2^{28}-1)$]/(2^{28})

For integer operation of these outputs dividers, N = 3 is also supported.

Output Divider Frequency Sources

Output dividers associated with the Q[0:3] outputs can take their input frequencies from either PLL0 or PLL1.

Output dividers associated with the Q[4:7] outputs can take their input frequencies from PLL0, PLL1, Q2 or Q3 output dividers, CLK0 or CLK1 input frequencies or the crystal frequency.

Output Banks

Outputs of the IDT8T49N283I are divided into three banks for purposes of output skew measurement:

- Q0, nQ0, Q1, nQ1
- Q4, nQ4, Q5, nQ5
- Q6, nQ6, Q7, nQ7

Output Phase Control on Switchover

When the IDT8T49N283I switches between input references, enters or leaves the holdover state for either PLL, there are two options on how the output phase can be controlled in these events: phase-slope limiting or fully hitless switching (sometimes called phase build-out) may be selected. The SWMODEn bit selects which behavior is to be followed for PLLn.

If fully hitless switching is selected, then the output phase will remain unchanged under any of these conditions. Note that fully hitless switching is not supported when external loopback is being used.

If phase-slope limiting is selected, then the output phase will adjust from its previous value until it is tracking the new condition at a rate dictated by the SLEWn[1:0] bits.

Output Phase Alignment

The device has a programmable output to output phase alignment for each of the eight output dividers. After power-up and the PLLs have achieved lock, the device will be in a state where the outputs are synchronized with a deterministic offset relative to each other.After synchronization, the output alignment will depend on the particular configuration of each output according to the following rules. The step size is defined as the period of the clock to that divider:

1) Only outputs derived from the same source will be aligned with each other. 'Source' means the reference selected to drive the output divider (as controlled by the CLK_SELn bit for each output.

2) For integer dividers (Q0, Q1, Q4-7) when both divider stages are active, edges are aligned. This case is used as a baseline to compare the other cases here.

3) For integer dividers where the 1st-stage divider is bypassed (only Q4-Q7 support this), the output phase will be one step earlier than in Case 2.

4) Fractional output dividers (Q2 or Q3) do not guarantee any specific phase on power-up or after a synchronization event.

5) Integer dividers using Q2 or Q3 as a source (Q4-7 support this option) will be aligned to their source divider's output (Q2 or Q3). Note that the output skews described above are not included in any of the phase adjustments described here.

Once the device is in operation, the outputs associated with each PLL may have their phase adjustments re-synced in one of two ways:

1) If the PLL becomes unlocked, the coarse phase adjustments will be reset and the fine phase adjustments will be re-loaded once it becomes locked again.

2) Toggling of a register bit for either PLL may also be used to force a re-sync / re-load for outputs associated with that PLL.

The user may apply adjustments that are proportional to the period of the clock source each output divider is operating from. For example, if the divider associated with Output Q3 is running off PLL0, which has a VCO frequency of 4GHz, then the appropriate period would be 250ps. The output phase may be adjusted in these steps across the full period of the output.

- Coarse Adjustment: all Output Dividers may have their phase adjusted in steps of the VCO period (T_{VCO}). For example a 4GHz VCO gives a step size of 250ps. The user may request an adjustment of phase of up to 31 steps using a single register write. The phase will be adjusted by lengthening the period of the output by 1 x T_{VCO} at a time. This process will be repeated every four output clock periods until the full requested adjustment has been achieved. A busy signal will remain asserted in the phase delay register until the requested adjustment is complete. Then a further adjustment may be setup and triggered by toggling the trigger bit.
- Fine Adjustment: For the Fractional Output Dividers associated with the Q2 and Q3 outputs, the phase of those outputs may be further adjusted with a granularity of 1/16th of the VCO period. For example a 4GHz VCO frequency gives a granularity of 16ps. This is performed by directly writing the required offset (from the nominal rising edge position) in units of 1/16th of the output period into a register. Then the appropriate PLLn_SYN bit must be toggled to load the new value. Note that toggling this bit will clear all Coarse Delays for all outputs associated with that PLL, so Fine Delays should be set first, before Coarse Delays. The output will then jump directly to that new offset value. For this reason, this adjustment should be made as the input is initially programmed or in Hi-Z.

In addition to the above, any of the output clock signals may be looped back to any input to serve as an external loopback connection. Any input reference used as an external feedback signal must not be used as an input reference for the same PLL. The REF_DISn_x register bit must be asserted for that input & PLL. Fractional output divide ratios and FEC rate outputs may not be used for external feedback.

Each output has the capability of being inverted (180 degree phase shift).

Jitter and Wander Tolerance

The IDT8T49N283I can be used as a line card device and therefore is expected to tolerate the jitter and wander output of a timing card PLL (e.g IDT82V3390).

Output Drivers

The Q0 to Q7 clock outputs are provided with register-controlled output drivers. By selecting the output drive type in the appropriate register, any of these outputs can support LVCMOS, LVPECL or LVDS logic levels.

The operating voltage ranges of each output is determined by its independent output power pin (V_{CCO}) and thus each can have different output voltage levels. Output voltage levels of 2.5V or 3.3V are supported for differential operation and LVCMOS operation. In addition, LVCMOS output operation supports 1.8V V_{CCO}.

Each output may be enabled or disabled by register bits and/or GPIO pins configured as Output Enables. The outputs will be enabled if the register bit and the associated OE pin are both asserted (high). When disabled an output will be in a high impedance state.

LVCMOS Operation

When a given output is configured to provide LVCMOS levels, then both the Q and nQ outputs will toggle at the selected output frequency. All the previously described configuration and control apply equally to both outputs. Frequency, phase alignment, voltage

levels and enable / disable status apply to both the Q and nQ pins. When configured as LVCMOS, the Q & nQ outputs can be selected to be phase-aligned with each other or inverted relative to one another. Selection of phase-alignment may have negative effects on the phase noise performance of any part of the device due to increased simultaneous switching noise within the device.

Power-Saving Modes

To allow the device to consume the least power possible for a given application, the following functions are included under register control:

- PLL1 may be shut down.
- Any unused output, including all output divider and phase adjustment logic, can be individually powered-off.
- Clock gating on logic that is not being used.

Status / Control Signals and Interrupts

General-Purpose I/Os & Interrupts

The IDT8T49N283I provides 4 General Purpose Input / Output (GPIO) pins for miscellaneous status & control functions. Each GPIO may be configured as an input or an output. Each GPIO may be directly controlled from register bits or be used as a predefined function as shown in Table 2. Note that the default state prior to configuration being loaded from internal OTP or external EEPROM will be to set each GPIO to function as an Output Enable.

Table 2. GPIO Configuration

	Configured as Input				Configured as Output		
	Fixed Function				Fixed Function		
GPIO Pin	Output Enable (default)		Clock Select	General Purpose			General Purpose
3	OE[3]	OE[7]	CSEL1	GPI[3]	-	-	GPO[3]
2	OE[2]	OE[6]	CSEL0	GPI[2]	LOS[0]	LOS[1]	GPO[2]
1	OE[1]	OE[5]	-	GPI[1]	HOLD[0]	HOLD[1]	GPO[1]
0	OE[0]	OE[4]	-	GPI[0]	LOL[0]	LOL[1]	GPO[0]

If used in the Fixed Function mode of operation, the GPIO bits will reflect the real-time status of their respective status bits as shown in Table 2.

Interrupt Functionality

Interrupt functionality includes an interrupt status flag for each of PLL Loss-of-Lock Status (LOL[1:0]), PLL Holdover Status (HOLD[1:0]) and Input Reference Status (LOS[1:0]) that is set whenever there is an alarm on any of those signals. The Status Flag will remain set until the alarm has been cleared and a '1' has been written to the Status Flag's register location or if a reset occurs. Each Status Flag will also have an Interrupt Enable bit that will determine if that Status Flag is allowed to cause the Interrupt Status to be affected (enabled) or not (disabled). All Interrupt Enable bits will be in the disabled state after reset. The Device Interrupt Status flag and nINT output pin are asserted if any of the enabled Interrupt Status flags are set.

Device Hardware Configuration

The IDT8T49N283I supports an internal One-Time Programmable (OTP) memory that can be pre-programmed at the factory with 1 complete device configuration. If the device is set to read a configuration from an external, serial EEPROM, then the values read will overwrite the OTP-defined values.

This configuration can be over-written using the serial interface once reset is complete. Any configuration written via the programming interface needs to be re-written after any power cycle or reset. Please contact IDT if a specific factory-programmed configuration is desired.

Device Start-up & Reset Behavior

The IDT8T49N283I has an internal power-up reset (POR) circuit and a Master Reset input pin nRST. If either is asserted, the device will be in the Reset State.

While in the reset state (nRST input asserted or POR active), the device will operate as follows:

- All registers will return to & be held in their default states as indicated in the applicable register description.
- All internal state machines will be in their reset conditions.
- The serial interface will not respond to read or write cycles.
- The GPIO signals will be configured as General-Purpose inputs.
- All clock outputs will be disabled.
- All interrupt status and Interrupt Enable bits will be cleared, negating the nINT signal.

Upon the later of the internal POR circuit expiring or the nRST input negating, the device will exit reset and begin self-configuration.

The device will load an initial block of its internal registers using the configuration stored in the internal One-Time Programmable (OTP) memory. Once this step is complete, the IDT8T49N283I will check the register settings to see if it should load the remainder of its configuration from an external I^2C EEPROM at a defined address or continue loading from OTP. See the section on I^2C Boot Initialization for details on how this is performed.

Once the full configuration has been loaded, the device will respond to accesses on the serial port and will attempt to lock both PLLs to the selected sources and begin operation. Once the PLLs are locked, all the outputs derived from a given PLL will be synchronized and output phase adjustments can then be applied if desired.Serial Control Port Description

Serial Control Port Configuration Description

The device has a serial control port capable of responding as a slave in an I^2C compatible configuration, to allow access any of the internal registers for device programming or examination of internal status. All registers are configured to have default values. See the specifics for each register for details.

The device has the additional capability of becoming a master on the I^2C bus only for the purpose of reading its initial register configurations from a serial EEPROM on the I^2C bus. Writing of the configuration to the serial EEPROM must be performed by another device on the same I^2C bus or pre-programmed into the device prior to assembly.

I²C Mode Operation

The I²C interface is designed to fully support v1.2 of the I²C Specification for Normal and Fast mode operation. The device acts as a slave device on the I²C bus at 100kHz or 400kHz using the address defined in the Status Control register, as modified by the S_A0 input pin setting. The interface accepts byte-oriented block write and block read operations. Two address bytes specify the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

For full electrical I²C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 51kΩ typical.

I²C Master Mode

When operating in I²C mode, the IDT8T49N283I has the capability to become a bus master on the I²C bus for the purposes of reading its configuration from an external I²C EEPROM. Only a block read cycle will be supported.

As an I²C bus master, the IDT8T49N283I will support the following functions:

- 7-bit addressing mode
- Base address register for EEPROM
- Validation of the read block via CCITT-8 CRC check against value stored in last byte of EEPROM
- Support for 100kHz and 400kHz operation with speed negotiation.
- Support for 1 or 2-byte addressing mode
- Master arbitration with programmable number of retries
- Fixed-period cycle response timer to prevent permanently hanging the I²C bus.
- Read will abort with an alarm (BOOTFAIL) if any of the following conditions occur: Slave NACK, Arbitration Fail, Collision during Address Phase, CRC failure, Slave Response time-out

The IDT8T49N283I will not support the following functions:

- I²C General Call
- Slave clock stretching
- I²C Start Byte protocol
- EEPROM Chaining
- CBUS compatibility
- Responding to its own slave address when acting as a master
- Writing to external I²C devices including the external EEPROM used for booting

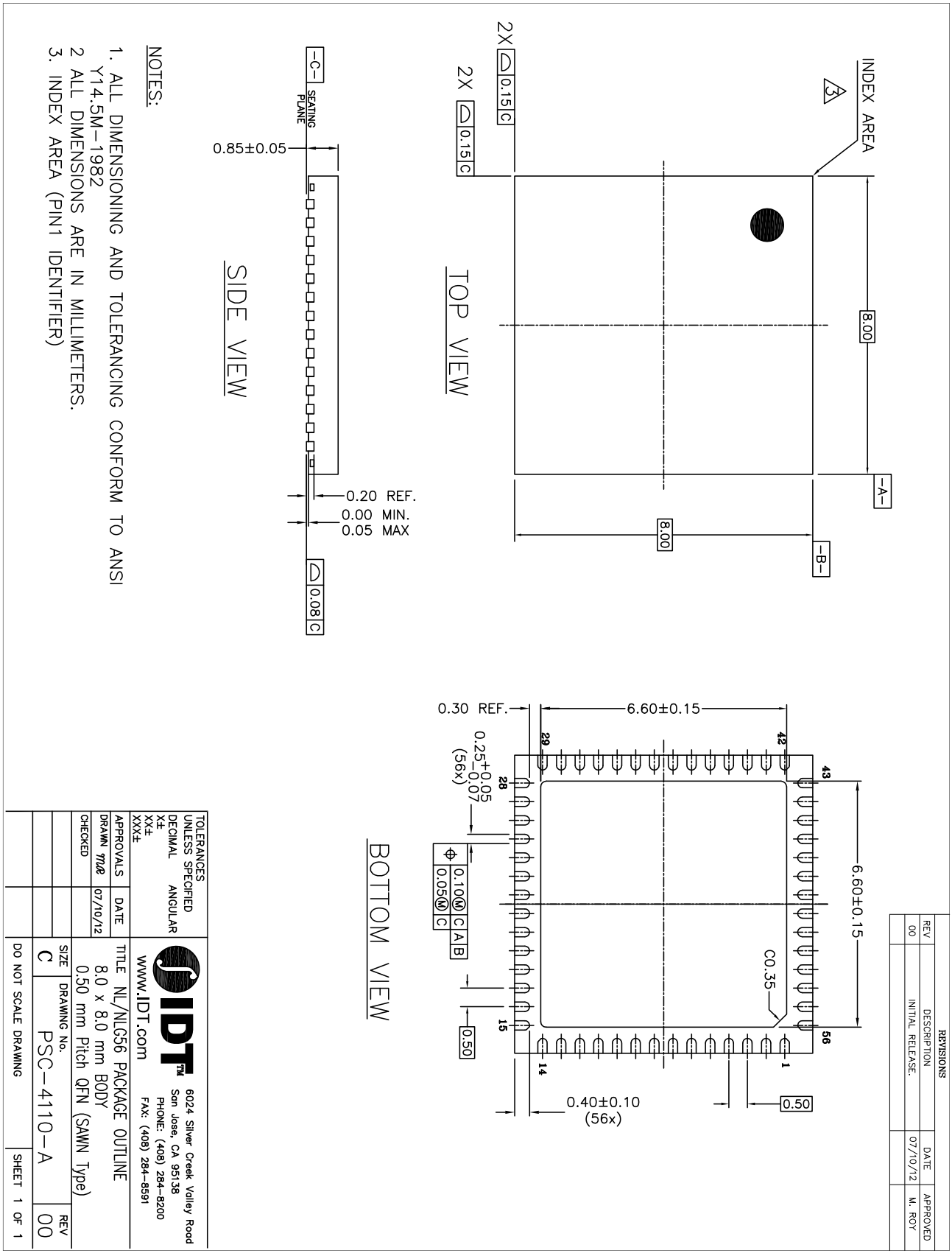
I²C Boot-up Initialization Mode

If enabled, once the nRST input has been deasserted (high) and its internal power-up reset sequence has completed, the device will contend for ownership of the I²C bus to read its initial register settings from a memory location on the I²C bus. The address of that memory location is kept in non-volatile memory in the Startup register. During the boot-up process, the device will not respond to serial control port accesses. Once the initialization process is complete, the contents of any of the device's registers can be altered. It is the responsibility of the user to make any desired adjustments in initial values directly in the serial bus memory.

If a NACK is received to any of the read cycles performed by the device during the initialization process, or if the CRC does not match the one stored in address 0xE0 of the EEPROM the process will be aborted and any uninitialized registers will remain with their default values. The BOOTFAIL bit in the Status Control register will also be set in this event.

If the BOOTFAIL bit is set, then both LOL[n] indicators will be set.

56 Lead VFQFN NL Package Outline



Ordering Information

Table 1:Table 14. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T49N283B-dddNLGI	8T49N283BNLGI	“Lead-Free” 56 Lead VFQFN	Tray	-40°C to +85°C
8T49N283B-dddNLGI8	8T49N283BNLGI	“Lead-Free” 56 Lead VFQFN	Tape & Reel	-40°C to +85°C

NOTE: For the specific -ddd order codes, refer to *FemtoClock NG Universal Frequency Translator Ordering Product Information guide*.

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