

## Programmable Timing Control Hub™ for Desktop P4™ Systems

### Recommended Application:

CK410 clock, Intel Yellow Cover part

### Output Features:

- 2 - 0.7V current-mode differential CPU pairs
- 6 - 0.7V current-mode differential SRC pair for SATA and PCI-E
- 1 - 0.7V current-mode differential CPU/SRC selectable pair
- 6 - PCI (33MHz)
- 3 - PCICLK\_F, (33MHz) free-running
- 1 - USB, 48MHz
- 1 - DOT, 96MHz, 0.7V current differential pair
- 1 - REF, 14.318MHz

### Key Specifications:

- CPU outputs cycle-cycle jitter < 85ps
- SRC output cycle-cycle jitter < 125ps
- PCI outputs cycle-cycle jitter < 500ps
- +/- 300ppm frequency accuracy on CPU & SRC clocks

### Features/Benefits:

- Supports tight ppm accuracy clocks for Serial-ATA and PCI-Express
- Supports spread spectrum modulation, 0 to -0.5% down spread
- Supports CPU clks up to 400MHz
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning
- Supports undriven differential CPU, SRC pair in PD# for power management.

### Functionality

| FS_C <sup>1</sup> | FS_B <sup>2</sup> | FS_A <sup>2</sup> | CPU MHz  | SRC MHz | PCI MHz | REF MHz | USB MHz | DOT MHz |
|-------------------|-------------------|-------------------|----------|---------|---------|---------|---------|---------|
| 0                 | 0                 | 0                 | 266.66   | 100.00  | 33.33   | 14.318  | 48.00   | 96.00   |
| 0                 | 0                 | 1                 | 133.33   | 100.00  | 33.33   | 14.318  | 48.00   | 96.00   |
| 0                 | 1                 | 0                 | 200.00   | 100.00  | 33.33   | 14.318  | 48.00   | 96.00   |
| 0                 | 1                 | 1                 | 166.66   | 100.00  | 33.33   | 14.318  | 48.00   | 96.00   |
| 1                 | 0                 | 0                 | 333.33   | 100.00  | 33.33   | 14.318  | 48.00   | 96.00   |
| 1                 | 0                 | 1                 | 100.00   | 100.00  | 33.33   | 14.318  | 48.00   | 96.00   |
| 1                 | 1                 | 0                 | 400.00   | 100.00  | 33.33   | 14.318  | 48.00   | 96.00   |
| 1                 | 1                 | 1                 | RESERVED |         |         | 14.318  | 48.00   | 96.00   |

1. FS\_C is a three-level input. Please see V<sub>IL,FS</sub> and V<sub>IH,FS</sub> specifications in the Input/Supply/Common Output Parameters Table for correct values. Also refer to the Test Clarification Table.
2. FS\_B and FS\_A are low-threshold inputs. Please see the V<sub>IL,FS</sub> and V<sub>IH,FS</sub> specifications in the Input/Supply/Common Output Parameters Table for correct values.

### Pin Configuration

|                  |    |    |                        |
|------------------|----|----|------------------------|
| VDDPCI           | 1  | 56 | PCICLK2                |
| GND              | 2  | 55 | PCICLK1                |
| PCICLK3          | 3  | 54 | PCICLK0                |
| PCICLK4          | 4  | 53 | FS_C/TEST_SEL          |
| PCICLK5          | 5  | 52 | REFOUT                 |
| GND              | 6  | 51 | GND                    |
| VDDPCI           | 7  | 50 | X1                     |
| ITP_EN/PCICLK_F0 | 8  | 49 | X2                     |
| PCICLK_F1        | 9  | 48 | VDDREF                 |
| PCICLK_F2        | 10 | 47 | SDATA                  |
| VDD48            | 11 | 46 | SCLK                   |
| USB_48MHz        | 12 | 45 | GND                    |
| GND              | 13 | 44 | CPUCLKT0               |
| DOTT_96MHz       | 14 | 43 | CPUCLKC0               |
| DOTC_96MHz       | 15 | 42 | VDDCPU                 |
| FS_B/TEST_MODE   | 16 | 41 | CPUCLKT1               |
| Vtt_PwrGd#/PD    | 17 | 40 | CPUCLKC1               |
| FS_A_410         | 18 | 39 | IREF                   |
| SRCCLKT1         | 19 | 38 | GNDA                   |
| SRCCLKC1         | 20 | 37 | VDDA                   |
| VDDSRC           | 21 | 36 | CPUCLKT2_ITP/SRCCLKT_7 |
| SRCCLKT2         | 22 | 35 | CPUCLKC2_ITP/SRCCLKC_7 |
| SRCCLKC2         | 23 | 34 | VDDSRC                 |
| SRCCLKT3         | 24 | 33 | SRCCLKT6               |
| SRCCLKC3         | 25 | 32 | SRCCLKC6               |
| SRCCLKT4_SATA    | 26 | 31 | SRCCLKT5               |
| SRCCLKC4_SATA    | 27 | 30 | SRCCLKC5               |
| VDDSRC           | 28 | 29 | GND                    |

### 56-pin SSOP & TSSOP



## Pin Description

| Pin # | PIN NAME         | PIN TYPE | DESCRIPTION                                                                                                                                                                                                                                                   |
|-------|------------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | VDDPCI           | PWR      | Power supply for PCI clocks, nominal 3.3V                                                                                                                                                                                                                     |
| 2     | GND              | PWR      | Ground pin.                                                                                                                                                                                                                                                   |
| 3     | PCICLK3          | OUT      | PCI clock output.                                                                                                                                                                                                                                             |
| 4     | PCICLK4          | OUT      | PCI clock output.                                                                                                                                                                                                                                             |
| 5     | PCICLK5          | OUT      | PCI clock output.                                                                                                                                                                                                                                             |
| 6     | GND              | PWR      | Ground pin.                                                                                                                                                                                                                                                   |
| 7     | VDDPCI           | PWR      | Power supply for PCI clocks, nominal 3.3V                                                                                                                                                                                                                     |
| 8     | ITP_EN/PCICLK_F0 | I/O      | Free running PCI clock not affected by PCI_STOP#.<br>ITP_EN: latched input to select pin functionality<br>1 = CPU_ITP pair<br>0 = SRC pair                                                                                                                    |
| 9     | PCICLK_F1        | OUT      | Free running PCI clock not affected by PCI_STOP# .                                                                                                                                                                                                            |
| 10    | PCICLK_F2        | OUT      | Free running PCI clock not affected by PCI_STOP# .                                                                                                                                                                                                            |
| 11    | VDD48            | PWR      | Power pin for the 48MHz output.3.3V                                                                                                                                                                                                                           |
| 12    | USB_48MHz        | OUT      | 48.00MHz USB clock                                                                                                                                                                                                                                            |
| 13    | GND              | PWR      | Ground pin.                                                                                                                                                                                                                                                   |
| 14    | DOTT_96MHz       | OUT      | True clock of differential pair for 96.00MHz DOT clock.                                                                                                                                                                                                       |
| 15    | DOTC_96MHz       | OUT      | Complement clock of differential pair for 96.00MHz DOT clock.                                                                                                                                                                                                 |
| 16    | FS_B/TEST_MODE   | IN       | 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table.  |
| 17    | Vtt_PwrGd#/PD    | IN       | Vtt_PwrGd# is an active low input used to determine when latched inputs are ready to be sampled. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks, PLLs and the crystal oscillator are stopped. |
| 18    | FS_A_410         | IN       | 3.3V tolerant low threshold input for CPU frequency selection. This pin requires CK410 FSA. Refer to input electrical characteristics for Vil_FS and Vih_FS threshold values.                                                                                 |
| 19    | SRCCLKT1         | OUT      | True clock of differential SRC clock pair.                                                                                                                                                                                                                    |
| 20    | SRCCLKC1         | OUT      | Complement clock of differential SRC clock pair.                                                                                                                                                                                                              |
| 21    | VDDSRC           | PWR      | Supply for SRC clocks, 3.3V nominal                                                                                                                                                                                                                           |
| 22    | SRCCLKT2         | OUT      | True clock of differential SRC clock pair.                                                                                                                                                                                                                    |
| 23    | SRCCLKC2         | OUT      | Complement clock of differential SRC clock pair.                                                                                                                                                                                                              |
| 24    | SRCCLKT3         | OUT      | True clock of differential SRC clock pair.                                                                                                                                                                                                                    |
| 25    | SRCCLKC3         | OUT      | Complement clock of differential SRC clock pair.                                                                                                                                                                                                              |
| 26    | SRCCLKT4_SATA    | OUT      | True clock of differential SRC/SATA pair.                                                                                                                                                                                                                     |
| 27    | SRCCLKC4_SATA    | OUT      | Complement clock of differential SRC/SATA pair.                                                                                                                                                                                                               |
| 28    | VDDSRC           | PWR      | Supply for SRC clocks, 3.3V nominal                                                                                                                                                                                                                           |



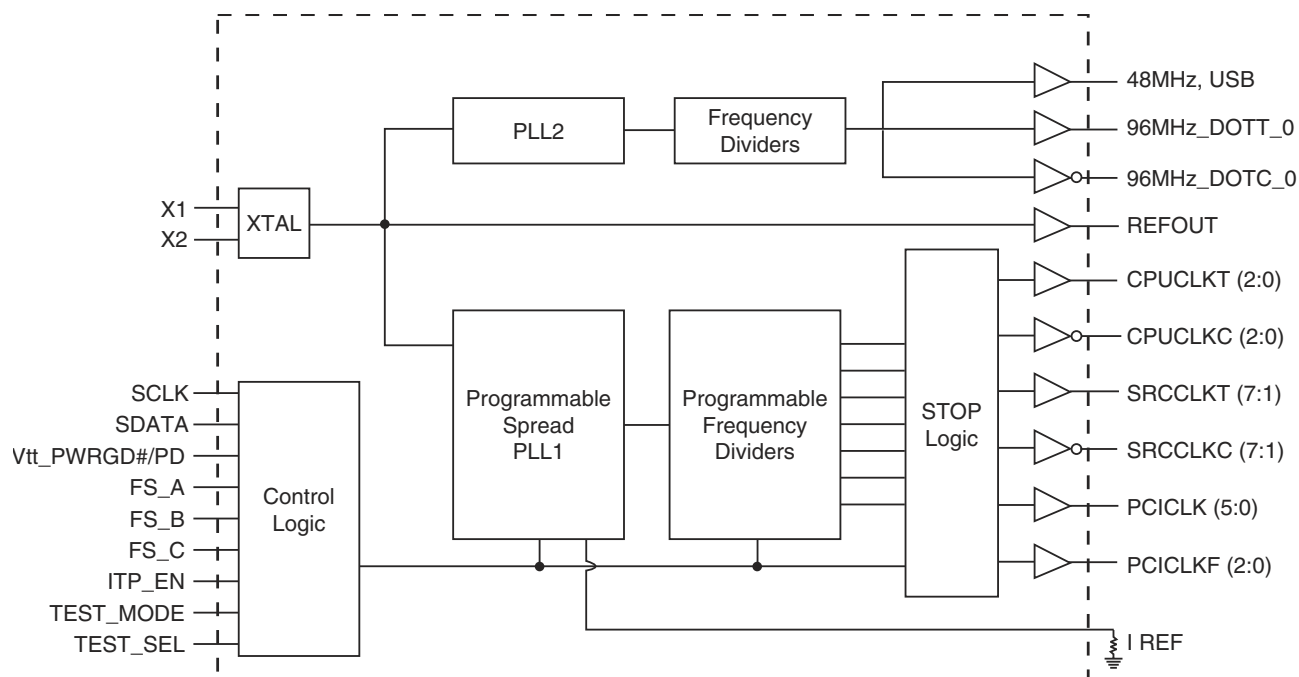
## Pin Description (Continued)

| Pin # | PIN NAME               | TYPE | DESCRIPTION                                                                                                                                                                                                                              |
|-------|------------------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29    | GND                    | PWR  | Ground pin.                                                                                                                                                                                                                              |
| 30    | SRCCLK5                | OUT  | Complement clock of differential SRC clock pair.                                                                                                                                                                                         |
| 31    | SRCCLKT5               | OUT  | True clock of differential SRC clock pair.                                                                                                                                                                                               |
| 32    | SRCCLK6                | OUT  | Complement clock of differential SRC clock pair.                                                                                                                                                                                         |
| 33    | SRCCLKT6               | OUT  | True clock of differential SRC clock pair.                                                                                                                                                                                               |
| 34    | VDDSRC                 | PWR  | Supply for SRC clocks, 3.3V nominal                                                                                                                                                                                                      |
| 35    | CPUCLKC2_ITP/SRCCLKC_7 | OUT  | Complimentary clock of CPU_ITP/SRC differential pair CPU_ITP/SRC output. These are current mode outputs. External resistors are required for voltage bias. Selected by ITP_EN input.                                                     |
| 36    | CPUCLKT2_ITP/SRCCLKT_7 | OUT  | True clock of CPU_ITP/SRC differential pair CPU_ITP/SRC output. These are current mode outputs. External resistors are required for voltage bias. Selected by ITP_EN input.                                                              |
| 37    | VDDA                   | PWR  | 3.3V power for the PLL core.                                                                                                                                                                                                             |
| 38    | GNDA                   | PWR  | Ground pin for the PLL core.                                                                                                                                                                                                             |
| 39    | IREF                   | OUT  | This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.    |
| 40    | CPUCLKC1               | OUT  | Complimentary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.                                                                                                  |
| 41    | CPUCLKT1               | OUT  | True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.                                                                                                           |
| 42    | VDDCPU                 | PWR  | Supply for CPU clocks, 3.3V nominal                                                                                                                                                                                                      |
| 43    | CPUCLKC0               | OUT  | Complimentary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.                                                                                                  |
| 44    | CPUCLKT0               | OUT  | True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.                                                                                                           |
| 45    | GND                    | PWR  | Ground pin.                                                                                                                                                                                                                              |
| 46    | SCLK                   | IN   | Clock pin of SMBus circuitry, 5V tolerant.                                                                                                                                                                                               |
| 47    | SDATA                  | I/O  | Data pin for SMBus circuitry, 5V tolerant.                                                                                                                                                                                               |
| 48    | VDDREF                 | PWR  | Ref, XTAL power supply, nominal 3.3V                                                                                                                                                                                                     |
| 49    | X2                     | OUT  | Crystal output, Nominally 14.318MHz                                                                                                                                                                                                      |
| 50    | X1                     | IN   | Crystal input, Nominally 14.318MHz.                                                                                                                                                                                                      |
| 51    | GND                    | PWR  | Ground pin.                                                                                                                                                                                                                              |
| 52    | REFOUT                 | OUT  | Reference Clock output                                                                                                                                                                                                                   |
| 53    | FS_C/TEST_SEL          | IN   | 3.3V tolerant input for CPU frequency selection. Low voltage threshold inputs, see input electrical characteristics for Vil_FS and Vih_FS values. TEST_Sel: 3-level latched input to enable test mode. Refer to Test Clarification Table |
| 54    | PCICLK0                | OUT  | PCI clock output.                                                                                                                                                                                                                        |
| 55    | PCICLK1                | OUT  | PCI clock output.                                                                                                                                                                                                                        |
| 56    | PCICLK2                | OUT  | PCI clock output.                                                                                                                                                                                                                        |

## General Description

**ICS954101** follows Intel CK410 Yellow Cover specification. This clock synthesizer provides a single chip solution for next generation P4 Intel processors and Intel chipsets. **ICS954101** is driven with a 14.318MHz crystal. It generates CPU outputs up to 400MHz. It also provides a tight ppm accuracy output for Serial ATA and PCI-Express support.

## Block Diagram



## Power Groups

| Pin Number |     | Description              |
|------------|-----|--------------------------|
| VDD        | GND |                          |
| 48         | 51  | Xtal, Ref                |
| 1,7        | 2,6 | PCICLK outputs           |
| 21,28,34   | 29  | SRCCLK outputs           |
| 37         | 38  | Master clock, CPU Analog |
| 11         | 13  | DOT, USB, PLL_48         |
| 42         | 45  | CPUCCLK clocks           |

## General I<sup>2</sup>C serial interface information for the ICS954101

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2<sub>(H)</sub>
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**  
(see Note 2)
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation     |           |                      |
|---------------------------------|-----------|----------------------|
| Controller (Host)               |           | ICS (Slave/Receiver) |
| T                               | starT bit |                      |
| Slave Address D2 <sub>(H)</sub> |           |                      |
| WR                              | WRite     |                      |
|                                 |           | ACK                  |
| Beginning Byte = N              |           |                      |
|                                 |           | ACK                  |
| Data Byte Count = X             |           |                      |
|                                 |           | ACK                  |
| Beginning Byte N                |           |                      |
|                                 |           | ACK                  |
| ○                               |           | ○                    |
| ○                               |           | ○                    |
| ○                               |           | ○                    |
| Byte N + X - 1                  |           |                      |
|                                 |           | ACK                  |
| P                               | stoP bit  |                      |

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2<sub>(H)</sub>
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3<sub>(H)</sub>
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if X<sub>(H)</sub> was written to byte 8)**.
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation      |                 |                      |
|---------------------------------|-----------------|----------------------|
| Controller (Host)               |                 | ICS (Slave/Receiver) |
| T                               | starT bit       |                      |
| Slave Address D2 <sub>(H)</sub> |                 |                      |
| WR                              | WRite           |                      |
|                                 |                 | ACK                  |
| Beginning Byte = N              |                 |                      |
|                                 |                 | ACK                  |
| RT                              | Repeat starT    |                      |
| Slave Address D3 <sub>(H)</sub> |                 |                      |
| RD                              | ReaD            |                      |
|                                 |                 | ACK                  |
|                                 |                 | Data Byte Count = X  |
| ACK                             |                 |                      |
| ACK                             |                 | Beginning Byte N     |
| ○                               |                 | ○                    |
| ○                               |                 | ○                    |
| ○                               |                 | ○                    |
|                                 |                 | Byte N + X - 1       |
| N                               | Not acknowledge |                      |
| P                               | stoP bit        |                      |

## Absolute Max

| Symbol   | Parameter                                | Min       | Max             | Units |
|----------|------------------------------------------|-----------|-----------------|-------|
| VDD_A    | 3.3V Core Supply Voltage                 |           | $V_{DD} + 0.5V$ | V     |
| VDD_In   | 3.3V Logic Input Supply Voltage          | GND - 0.5 | $V_{DD} + 0.5V$ | V     |
| Ts       | Storage Temperature                      | -65       | 150             | °C    |
| Tambient | Ambient Operating Temp                   | 0         | 70              | °C    |
| Tcase    | Case Temperature                         |           | 115             | °C    |
| ESD prot | Input ESD protection<br>human body model | 2000      |                 | V     |

## Electrical Characteristics - Input/Supply/Common Output Parameters

T<sub>A</sub> = 0 - 70°C; Supply Voltage V<sub>DD</sub> = 3.3 V +/-5%

| PARAMETER                                  | SYMBOL                | CONDITIONS                                                        | MIN            | TYP      | MAX            | UNITS | NOTES |
|--------------------------------------------|-----------------------|-------------------------------------------------------------------|----------------|----------|----------------|-------|-------|
| Input High Voltage                         | V <sub>IH</sub>       | 3.3 V +/-5%                                                       | 2              |          | $V_{DD} + 0.3$ | V     |       |
| Input Low Voltage                          | V <sub>IL</sub>       | 3.3 V +/-5%                                                       | $V_{SS} - 0.3$ |          | 0.8            | V     |       |
| Input High Current                         | I <sub>IH</sub>       | V <sub>IN</sub> = V <sub>DD</sub>                                 | -5             |          | 5              | uA    |       |
| Input Low Current                          | I <sub>IL1</sub>      | V <sub>IN</sub> = 0 V; Inputs with no pull-up resistors           | -5             |          |                | uA    |       |
|                                            | I <sub>IL2</sub>      | V <sub>IN</sub> = 0 V; Inputs with pull-up resistors              | -200           |          |                | uA    |       |
| Low Threshold Input High Voltage           | V <sub>IH_FS</sub>    | 3.3 V +/-5%                                                       | 0.7            |          | $V_{DD} + 0.3$ | V     |       |
| Low Threshold Input Low Voltage            | V <sub>IL_FS</sub>    | 3.3 V +/-5%                                                       | $V_{SS} - 0.3$ |          | 0.35           | V     |       |
| Operating Supply Current                   | I <sub>DD3.3OP</sub>  | 3.3 V +/-5%, Full Load                                            |                | 350      | 500            | mA    |       |
| Powerdown Current                          | I <sub>DD3.3PD</sub>  | all diff pairs driven                                             |                |          | 70             | mA    |       |
|                                            |                       | all differential pairs tri-stated                                 |                |          | 12             | mA    |       |
| Input Frequency <sup>3</sup>               | F <sub>i</sub>        | V <sub>DD</sub> = 3.3 V                                           |                | 14.31818 |                | MHz   | 3     |
| Pin Inductance <sup>1</sup>                | L <sub>pin</sub>      |                                                                   |                |          | 7              | nH    | 1     |
| Input Capacitance <sup>1</sup>             | C <sub>IN</sub>       | Logic Inputs                                                      |                |          | 5              | pF    | 1     |
|                                            | C <sub>OUT</sub>      | Output pin capacitance                                            |                |          | 6              | pF    | 1     |
|                                            | C <sub>INX</sub>      | X1 & X2 pins                                                      |                |          | 5              | pF    | 1     |
| Clk Stabilization <sup>1,2</sup>           | T <sub>STAB</sub>     | From V <sub>DD</sub> Power-Up or de-assertion of PD# to 1st clock |                |          | 1.8            | ms    | 1,2   |
| Modulation Frequency                       |                       | Triangular Modulation                                             | 30             |          | 33             | kHz   | 1     |
| Tdrive_PD#                                 |                       | CPU output enable after PD# de-assertion                          |                |          | 300            | us    | 1     |
| Tfall_Pd#                                  |                       | PD# fall time of                                                  |                |          | 5              | ns    | 1     |
| Trise_Pd#                                  |                       | PD# rise time of                                                  |                |          | 5              | ns    | 2     |
| SMBus Voltage                              | V <sub>DD</sub>       |                                                                   | 2.7            |          | 5.5            | V     | 1     |
| Low-level Output Voltage                   | V <sub>OL</sub> SMBUS | @ I <sub>PULLUP</sub>                                             |                |          | 0.4            | V     | 1     |
| Current sinking at V <sub>OL</sub> = 0.4 V | I <sub>PULLUP</sub>   |                                                                   | 4              |          |                | mA    | 1     |
| SCLK/SDATA<br>Clock/Data Rise Time         | T <sub>RI2C</sub>     | (Max V <sub>IL</sub> - 0.15) to (Min V <sub>IH</sub> + 0.15)      |                |          | 1000           | ns    | 1     |
| SCLK/SDATA<br>Clock/Data Fall Time         | T <sub>FI2C</sub>     | (Min V <sub>IH</sub> + 0.15) to (Max V <sub>IL</sub> - 0.15)      |                |          | 300            | ns    | 1     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>See timing diagrams for timing requirements.

<sup>3</sup>Input frequency should be measured at the REF output pin and tuned to ideal 14.31818MHz to meet ppm accuracy on PLL outputs.

### Electrical Characteristics - CPU 0.7V Current Mode Differential Pair

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ;  $C_L = 2\text{pF}$ ,  $R_S = 33.2\Omega$ ,  $R_P = 49.9\Omega$ ,  $I_{REF} = 475\Omega$

| PARAMETER                       | SYMBOL        | CONDITIONS                                                                       | MIN    | TYP | MAX     | UNITS    | NOTES |
|---------------------------------|---------------|----------------------------------------------------------------------------------|--------|-----|---------|----------|-------|
| Current Source Output Impedance | $Z_o$         | $V_O = V_x$                                                                      | 3000   |     |         | $\Omega$ | 1     |
| Voltage High                    | VHigh         | Statistical measurement on single ended signal using oscilloscope math function. | 660    |     | 850     | mV       | 1     |
| Voltage Low                     | VLow          |                                                                                  | -150   |     | 150     |          | 1     |
| Max Voltage                     | Vovs          | Measurement on single ended signal using absolute value.                         |        |     | 1150    | mV       | 1     |
| Min Voltage                     | Vuds          |                                                                                  | -300   |     |         |          | 1     |
| Crossing Voltage (abs)          | Vcross(abs)   |                                                                                  | 250    |     | 550     | mV       | 1     |
| Crossing Voltage (var)          | d-Vcross      | Variation of crossing over all edges                                             |        |     | 140     | mV       | 1     |
| Long Accuracy                   | ppm           | see Tperiod min-max values                                                       | -300   |     | 300     | ppm      | 1,2   |
| Average period                  | Tperiod       | 400MHz nominal                                                                   | 2.4993 |     | 2.5008  | ns       | 2     |
|                                 |               | 400MHz spread                                                                    | 2.4993 |     | 2.5133  | ns       | 2     |
|                                 |               | 333.33MHz nominal                                                                | 2.9991 |     | 3.0009  | ns       | 2     |
|                                 |               | 333.33MHz spread                                                                 | 2.9991 |     | 3.016   | ns       | 2     |
|                                 |               | 266.66MHz nominal                                                                | 3.7489 |     | 3.7511  | ns       | 2     |
|                                 |               | 266.66MHz spread                                                                 | 3.7489 |     | 3.77    | ns       | 2     |
|                                 |               | 200MHz nominal                                                                   | 4.9985 |     | 5.0015  | ns       | 2     |
|                                 |               | 200MHz spread                                                                    | 4.9985 |     | 5.0266  | ns       | 2     |
|                                 |               | 166.66MHz nominal                                                                | 5.9982 |     | 6.0018  | ns       | 2     |
|                                 |               | 166.66MHz spread                                                                 | 5.9982 |     | 6.0320  | ns       | 2     |
|                                 |               | 133.33MHz nominal                                                                | 7.4978 |     | 7.5023  | ns       | 2     |
|                                 |               | 133.33MHz spread                                                                 | 7.4978 |     | 5.4000  | ns       | 2     |
|                                 |               | 100.00MHz nominal                                                                | 9.9970 |     | 10.0030 | ns       | 2     |
|                                 |               | 100.00MHz spread                                                                 | 9.9970 |     | 10.0533 | ns       | 2     |
| Absolute min period             | $T_{absmin}$  | 400MHz nominal/spread                                                            | 2.4143 |     |         | ns       | 1,2   |
|                                 |               | 333.33MHz nominal/spread                                                         | 2.9141 |     |         | ns       | 1,2   |
|                                 |               | 266.66MHz nominal/spread                                                         | 3.6639 |     |         | ns       | 1,2   |
|                                 |               | 200MHz nominal/spread                                                            | 4.8735 |     |         | ns       | 1,2   |
|                                 |               | 166.66MHz nominal/spread                                                         | 5.8732 |     |         | ns       | 1,2   |
|                                 |               | 133.33MHz nominal/spread                                                         | 7.3728 |     |         | ns       | 1,2   |
|                                 |               | 100.00MHz nominal/spread                                                         | 9.8720 |     |         | ns       | 1,2   |
| Rise Time                       | $t_r$         | $V_{OL} = 0.175\text{V}$ , $V_{OH} = 0.525\text{V}$                              | 175    |     | 700     | ps       | 1     |
| Fall Time                       | $t_f$         | $V_{OH} = 0.525\text{V}$ $V_{OL} = 0.175\text{V}$                                | 175    |     | 700     | ps       | 1     |
| Rise Time Variation             | d- $t_r$      |                                                                                  |        |     | 125     | ps       | 1     |
| Fall Time Variation             | d- $t_f$      |                                                                                  |        |     | 125     | ps       | 1     |
| Duty Cycle                      | $d_{13}$      | Measurement from differential waveform                                           | 45     |     | 55      | %        | 1     |
| Skew                            | $t_{sk3}$     | CPU (1:0) $V_T = 50\%$                                                           |        |     | 100     | ps       | 1     |
| Skew                            | $t_{sk4}$     | CPU (1:0) to CPU_ITP, $V_T = 50\%$                                               |        |     | 150     | ps       | 1     |
| Jitter, Cycle to cycle          | $t_{jyc-cyc}$ | Measurement from differential waveform                                           |        |     | 85      | ps       | 1     |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFoutput is at 14.31818MHz

## Electrical Characteristics - SRC 0.7V Current Mode Differential Pair

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ;  $C_L = 2\text{pF}$ ,  $R_S = 33.2\Omega$ ,  $R_P = 49.9\Omega$ ,  $I_{REF} = 475\Omega$

| PARAMETER                       | SYMBOL        | CONDITIONS                                                        | MIN    | TYP | MAX     | UNITS    | NOTES |
|---------------------------------|---------------|-------------------------------------------------------------------|--------|-----|---------|----------|-------|
| Current Source Output Impedance | $Z_o$         | $V_O = V_x$                                                       | 3000   |     |         | $\Omega$ | 1     |
| Voltage High                    | VHigh         | Statistical measurement on single ended signal using oscilloscope | 660    |     | 850     | mV       | 1     |
| Voltage Low                     | VLow          |                                                                   | -150   |     | 150     |          | 1     |
| Max Voltage                     | Vovs          | Measurement on single ended signal using absolute value.          |        |     | 1150    | mV       | 1     |
| Min Voltage                     | Vuds          |                                                                   | -300   |     |         |          | 1     |
| Crossing Voltage (abs)          | Vcross(abs)   |                                                                   | 250    | 350 | 550     | mV       | 1     |
| Crossing Voltage (var)          | d-Vcross      | Variation of crossing over all edges                              |        | 12  | 140     | mV       | 1     |
| Long Accuracy                   | ppm           | see Tperiod min-max values                                        | -300   |     | 300     | ppm      | 1,2   |
| Average period                  | Tperiod       | 100.00MHz nominal                                                 | 9.9970 |     | 10.0030 | ns       | 2     |
|                                 |               | 100.00MHz spread                                                  | 9.9970 |     | 10.0533 | ns       | 2     |
| Absolute min period             | Tabsmin       | 100.00MHz nominal/spread                                          | 9.8720 |     |         | ns       | 1,2   |
| Rise Time                       | $t_r$         | $V_{OL} = 0.175\text{V}$ , $V_{OH} = 0.525\text{V}$               | 175    |     | 700     | ps       | 1     |
| Fall Time                       | $t_f$         | $V_{OH} = 0.525\text{V}$ $V_{OL} = 0.175\text{V}$                 | 175    |     | 700     | ps       | 1     |
| Rise Time Variation             | d- $t_r$      |                                                                   |        | 30  | 125     | ps       | 1     |
| Fall Time Variation             | d- $t_f$      |                                                                   |        | 30  | 125     | ps       | 1     |
| Duty Cycle                      | $d_{t3}$      | Measurement from differential waveform                            | 45     |     | 55      | %        | 1     |
| Skew                            | $t_{sk3}$     | SRC(7:0), $V_T = 50\%$                                            |        |     | 250     | ps       | 1     |
| Jitter, Cycle to cycle          | $t_{jyc-cyc}$ | Measurement from differential waveform                            |        |     | 125     | ps       | 1     |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

<sup>2</sup> All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOutput is at 14.31818MHz

**Electrical Characteristics - PCICLK/PCICLK\_F**
 $T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ;  $C_L = 30\text{ pF}$  (unless otherwise specified)

| PARAMETER                     | SYMBOL              | CONDITIONS                                        | MIN      | TYP | MAX      | UNITS | Notes |
|-------------------------------|---------------------|---------------------------------------------------|----------|-----|----------|-------|-------|
| Long Accuracy                 | ppm                 | see Tperiod min-max values                        | -300     |     | 300      | ppm   | 1,2   |
| Clock period                  | $T_{\text{period}}$ | 33.33MHz output nominal                           | 29.99100 |     | 30.00900 | ns    | 2     |
|                               |                     | 33.33MHz output spread                            | 29.99100 |     | 30.15980 | ns    | 2     |
| Absolute Min/Max Clock period | $T_{\text{abs}}$    | 33.33MHz output nominal                           | 29.49100 |     | 30.50900 | ns    | 2     |
|                               |                     | 33.33MHz output spread                            | 29.49100 |     | 30.65980 | ns    | 2     |
| Clk High Time                 | $t_{h1}$            |                                                   | 12       |     | N/A      | ns    | 1     |
| Clock Low Time                | $t_{l1}$            |                                                   | 12       |     | N/A      | ns    | 1     |
| Output High Voltage           | $V_{OH}$            | $I_{OH} = -1\text{ mA}$                           | 2.4      |     |          | V     |       |
| Output Low Voltage            | $V_{OL}$            | $I_{OL} = 1\text{ mA}$                            |          |     | 0.55     | V     |       |
| Output High Current           | $I_{OH}$            | $V_{OH} @ \text{MIN} = 1.0\text{ V}$              | -33      |     |          | mA    |       |
|                               |                     | $V_{OH} @ \text{MAX} = 3.135\text{ V}$            |          |     | -33      | mA    |       |
| Output Low Current            | $I_{OL}$            | $V_{OL} @ \text{MIN} = 1.95\text{ V}$             | 30       |     |          | mA    |       |
|                               |                     | $V_{OL} @ \text{MAX} = 0.4\text{ V}$              |          |     | 38       | mA    |       |
| Edge Rate                     |                     | Rising edge rate                                  | 1        |     | 4        | V/ns  | 1     |
| Edge Rate                     |                     | Falling edge rate                                 | 1        |     | 4        | V/ns  | 1     |
| Rise Time                     | $t_{r1}$            | $V_{OL} = 0.4\text{ V}$ , $V_{OH} = 2.4\text{ V}$ | 0.5      |     | 2        | ns    | 1     |
| Fall Time                     | $t_{f1}$            | $V_{OH} = 2.4\text{ V}$ , $V_{OL} = 0.4\text{ V}$ | 0.5      |     | 2        | ns    | 1     |
| Duty Cycle                    | $d_{t1}$            | $V_T = 1.5\text{ V}$                              | 45       |     | 55       | %     | 1     |
| Skew                          | $t_{sk1}$           | $V_T = 1.5\text{ V}$                              |          |     | 500      | ps    | 1     |
| Jitter                        | $t_{jvc-cyc}$       | $V_T = 1.5\text{ V}$                              |          |     | 500      | ps    | 1     |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFoutput is at 14.31818MHz

**Electrical Characteristics - USB\_48MHz**
 $T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ;  $C_L = 20\text{ pF}$  (unless otherwise specified)

| PARAMETER                     | SYMBOL              | CONDITIONS                                        | MIN      | TYP | MAX      | UNITS | Notes |
|-------------------------------|---------------------|---------------------------------------------------|----------|-----|----------|-------|-------|
| Long Accuracy                 | ppm                 | see Tperiod min-max values                        | -100     |     | 100      | ppm   | 1,2   |
| Clock period                  | $T_{\text{period}}$ | 48.0000MHz output nominal                         | 20.82570 |     | 20.83400 | ns    | 2     |
| Absolute Min/Max Clock period | $T_{\text{abs}}$    | Nominal                                           | 20.48125 |     | 21.18542 | ns    | 2     |
| Clk High Time                 | $t_{h1}$            |                                                   | 8.094    |     | 10.036   | ns    | 1     |
| Clock Low Time                | $t_{l1}$            |                                                   | 7.694    |     | 9.836    | ns    | 1     |
| Output High Current           | $I_{OH}$            | $V_{OH} @ \text{MIN} = 1.0\text{ V}$              | -33      |     |          | mA    |       |
|                               |                     | $V_{OH} @ \text{MAX} = 3.135\text{ V}$            |          |     | -33      | mA    |       |
| Output Low Current            | $I_{OL}$            | $V_{OL} @ \text{MIN} = 1.95\text{ V}$             | 30       |     |          | mA    |       |
|                               |                     | $V_{OL} @ \text{MAX} = 0.4\text{ V}$              |          |     | 38       | mA    |       |
| Edge Rate                     |                     | Rising edge rate                                  | 1        |     | 2        | V/ns  | 1     |
| Edge Rate                     |                     | Falling edge rate                                 | 1        |     | 2        | V/ns  | 1     |
| Rise Time                     | $t_{r1}$            | $V_{OL} = 0.4\text{ V}$ , $V_{OH} = 2.4\text{ V}$ | 1        | 1.4 | 2        | ns    | 1     |
| Fall Time                     | $t_{f1}$            | $V_{OH} = 2.4\text{ V}$ , $V_{OL} = 0.4\text{ V}$ | 1        | 1.3 | 2        | ns    | 1     |
| Duty Cycle                    | $d_{t1}$            | $V_T = 1.5\text{ V}$                              | 45       | 48  | 55       | %     | 1     |
| Jitter, Cycle to cycle        | $t_{jvc-cyc}$       | $V_T = 1.5\text{ V}$                              |          |     | 350      | ps    | 1     |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFoutput is at 14.31818MHz

## Electrical Characteristics - DOT, 96MHz 0.7V Current Mode Differential Pair

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ;  $C_L = 2\text{pF}$ ,  $R_S = 33.2\Omega$ ,  $R_P = 49.9\Omega$ ,  $I_{REF} = 475\mu\text{A}$

| PARAMETER                       | SYMBOL                | CONDITIONS                                                                                 | MIN     | TYP | MAX     | UNITS    | NOTES |
|---------------------------------|-----------------------|--------------------------------------------------------------------------------------------|---------|-----|---------|----------|-------|
| Current Source Output Impedance | $Z_o$                 | $V_o = V_x$                                                                                | 3000    |     |         | $\Omega$ | 1     |
| Voltage High                    | VHigh                 | Statistical measurement on single ended signal<br>Measurement on single ended signal using | 660     |     | 850     | mV       | 1     |
| Voltage Low                     | VLow                  |                                                                                            | -150    |     | 150     |          | 1     |
| Max Voltage                     | Vovs                  |                                                                                            |         |     | 1150    | mV       | 1     |
| Min Voltage                     | Vuds                  |                                                                                            | -300    |     |         |          | 1     |
| Crossing Voltage (abs)          | Vcross(abs)           |                                                                                            | 250     |     | 550     | mV       | 1     |
| Crossing Voltage (var)          | d-Vcross              | Variation of crossing over all edges                                                       |         |     | 140     | mV       | 1     |
| Long Accuracy                   | ppm                   | see Tperiod min-max values                                                                 | -100    |     | 100     | ppm      | 1,2   |
| Average period                  | Tperiod               | 96.00MHz nominal                                                                           | 10.4135 |     | 10.4198 | ns       | 2     |
| Absolute min period             | Tabmin                | 96.00MHz nominal                                                                           | 10.1635 |     |         | ns       | 1,2   |
| Rise Time                       | $t_r$                 | $V_{OL} = 0.175\text{V}$ , $V_{OH} = 0.525\text{V}$                                        | 175     |     | 700     | ps       | 1     |
| Fall Time                       | $t_f$                 | $V_{OH} = 0.525\text{V}$ , $V_{OL} = 0.175\text{V}$                                        | 175     |     | 700     | ps       | 1     |
| Rise Time Variation             | d- $t_r$              |                                                                                            |         |     | 125     | ps       | 1     |
| Fall Time Variation             | d- $t_f$              |                                                                                            |         |     | 125     | ps       | 1     |
| Duty Cycle                      | $d_{13}$              | Measurement from differential waveform                                                     | 45      |     | 55      | %        | 1     |
| Jitter, Cycle to cycle          | $t_{j\text{cyc-cyc}}$ | Measurement from differential waveform                                                     |         |     | 250     | ps       | 1     |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

<sup>2</sup> All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOutput is at 14.31818MHz



## Electrical Characteristics - REF-14.318MHz

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 20 \text{ pF}$  (unless otherwise specified)

| PARAMETER                     | SYMBOL                | CONDITIONS                                                                         | MIN      | TYP | MAX      | UNITS | NOTES |
|-------------------------------|-----------------------|------------------------------------------------------------------------------------|----------|-----|----------|-------|-------|
| Long Accuracy                 | ppm                   | see Tperiod min-max values                                                         | -300     |     | 300      | ppm   | 1     |
| Clock period                  | $T_{\text{period}}$   | 14.318MHz output nominal                                                           | 69.82700 |     | 69.85500 | ns    | 1     |
| Absolute Min/Max Clock period | $T_{\text{abs}}$      | Nominal                                                                            | 68.82033 |     | 70.86224 | ns    | 2     |
| Output High Voltage           | $V_{OH}$              | $I_{OH} = -1 \text{ mA}$                                                           | 2.4      |     |          | V     | 1     |
| Output Low Voltage            | $V_{OL}$              | $I_{OL} = 1 \text{ mA}$                                                            |          |     | 0.4      | V     | 1     |
| Output High Current           | $I_{OH}$              | $V_{OH} @ \text{MIN} = 1.0 \text{ V}$ ,<br>$V_{OH} @ \text{MAX} = 3.135 \text{ V}$ | -29      |     | -23      | mA    | 1     |
| Output Low Current            | $I_{OL}$              | $V_{OL} @ \text{MIN} = 1.95 \text{ V}$ ,<br>$V_{OL} @ \text{MAX} = 0.4 \text{ V}$  | 29       |     | 27       | mA    | 1     |
| Rise Time                     | $t_{r1}$              | $V_{OL} = 0.4 \text{ V}$ , $V_{OH} = 2.4 \text{ V}$                                | 1        |     | 2        | ns    | 1     |
| Fall Time                     | $t_{f1}$              | $V_{OH} = 2.4 \text{ V}$ , $V_{OL} = 0.4 \text{ V}$                                | 1        |     | 2        | ns    | 1     |
| Duty Cycle                    | $d_{t1}$              | $V_T = 1.5 \text{ V}$                                                              | 45       |     | 55       | %     | 1     |
| Jitter                        | $t_{j\text{cyc-cyc}}$ | $V_T = 1.5 \text{ V}$                                                              |          |     | 1000     | ps    | 1     |

<sup>1</sup>Guaranteed by design, not 100% tested in production.



I<sup>2</sup>C Table: Read-Back Register

| Byte 0 | Pin # | Name                  | Control Function | Type | 0       | 1      | PWD |
|--------|-------|-----------------------|------------------|------|---------|--------|-----|
| Bit 7  | 35,36 | CPUCLK2/RCCLK7 Enable | Output Enable    | RW   | DISABLE | ENABLE | 1   |
| Bit 6  | 32,33 | SRCLK6 Enable         | Output Enable    | RW   | DISABLE | ENABLE | 1   |
| Bit 5  | 30,31 | SRCLK5 Enable         | Output Enable    | RW   | DISABLE | ENABLE | 1   |
| Bit 4  | 26,27 | SRCLK4 Enable         | Output Enable    | RW   | DISABLE | ENABLE | 1   |
| Bit 3  | 24,25 | SRCLK3 Enable         | Output Enable    | RW   | DISABLE | ENABLE | 1   |
| Bit 2  | 22,23 | SRCLK2 Enable         | Output Enable    | RW   | DISABLE | ENABLE | 1   |
| Bit 1  | 19,20 | SRCLK1 Enable         | Output Enable    | RW   | DISABLE | ENABLE | 1   |
| Bit 0  | -     | RESERVED              |                  |      |         |        |     |

I<sup>2</sup>C Table: Spreading and Device Behavior Control Register

| Byte 1 | Pin # | Name                 | Control Function | Type | 0          | 1         | PWD |
|--------|-------|----------------------|------------------|------|------------|-----------|-----|
| Bit 7  | 54    | PCI_F0 Enable        | Output Enable    | RW   | Disable    | Enable    | 1   |
| Bit 6  | 14,15 | DOT_96MHz            | Output Enable    | RW   | Disable    | Enable    | 1   |
| Bit 5  | 12    | USB_48MHz Enable     | Output Enable    | RW   | Disable    | Enable    | 1   |
| Bit 4  | 52    | REFOUT Enable        | Output Enable    | RW   | Disable    | Enable    | 1   |
| Bit 3  | -     | RESERVED             |                  |      |            |           |     |
| Bit 2  | 40,41 | CPUT1/CPUC1          | Output Enable    | RW   | Disable    | Enable    | 1   |
| Bit 1  | 43,44 | CPUT0/CPUC0          | Output Enable    | RW   | Disable    | Enable    | 1   |
| Bit 0  | -     | Spread Spectrum Mode | Spread Off       | RW   | SPREAD OFF | SPREAD ON | 0   |

I<sup>2</sup>C Table: Output Control Register

| Byte 2 | Pin # | Name          | Control Function | Type | 0       | 1      | PWD |
|--------|-------|---------------|------------------|------|---------|--------|-----|
| Bit 7  | 5     | PCICLK5       | Output Enable    | RW   | Disable | Enable | 1   |
| Bit 6  | 4     | PCICLK4       | Output Enable    | RW   | Disable | Enable | 1   |
| Bit 5  | 3     | PCICLK3       | Output Enable    | RW   | Disable | Enable | 1   |
| Bit 4  | 56    | PCICLK2       | Output Enable    | RW   | Disable | Enable | 1   |
| Bit 3  | 55    | PCICLK1       | Output Enable    | RW   | Disable | Enable | 1   |
| Bit 2  | 54    | PCICLK0       | Output Enable    | RW   | Disable | Enable | 1   |
| Bit 1  | 10    | PCI_F2 Enable | Output Enable    | RW   | Disable | Enable | 1   |
| Bit 0  | 9     | PCI_F1 Enable | Output Enable    | RW   | Disable | Enable | 1   |

I<sup>2</sup>C Table: Output Control Register

| Table: Output Control Register |       |       |                 |                                                                                           |      |              |           |     |
|--------------------------------|-------|-------|-----------------|-------------------------------------------------------------------------------------------|------|--------------|-----------|-----|
| Byte 3                         |       | Pin # | Name            | Control Function                                                                          | Type | 0            | 1         | PWD |
| Bit 7                          | 35,35 |       | CPU_ITP/SRCCLK7 | Free-Running<br>Control<br>default:<br>not affected by<br>PCI/SRC_STOP<br>(Byte 6, bit 3) | RW   | Free-Running | Stoppable | 0   |
| Bit 6                          | 32,33 |       | SRCLK6          |                                                                                           | RW   | Free-Running | Stoppable | 0   |
| Bit 5                          | 30,31 |       | SRCLK5          |                                                                                           | RW   | Free-Running | Stoppable | 0   |
| Bit 4                          | 26,27 |       | SRCLK4          |                                                                                           | RW   | Free-Running | Stoppable | 0   |
| Bit 3                          | 24,25 |       | SRCLK3          |                                                                                           | RW   | Free-Running | Stoppable | 0   |
| Bit 2                          | 22,23 |       | SRCLK2          |                                                                                           | RW   | Free-Running | Stoppable | 0   |
| Bit 1                          | 19,20 |       | SRCLK1          |                                                                                           | RW   | Free-Running | Stoppable | 0   |
| Bit 0                          | -     |       | RESERVED        |                                                                                           |      |              |           |     |



I<sup>2</sup>C Table: Output Control Register

| Byte 4 | Pin # | Name      | Control Function                           | Type | 0            | 1         | PWD |
|--------|-------|-----------|--------------------------------------------|------|--------------|-----------|-----|
| Bit 7  |       | RESERVED  |                                            |      |              |           | 1   |
| Bit 6  | 14,15 | DOT_96MHz | Driven in PD                               | RW   | Driven       | Hi-Z      | 1   |
| Bit 5  | 10    | PCI_F2    | Free-Running<br>Control<br>not affected by | RW   | Free-Running | Stoppable | 1   |
| Bit 4  | 9     | PCI_F1    |                                            | RW   | Free-Running | Stoppable | 1   |
| Bit 3  | 8     | PCI_F0    |                                            | RW   | Free-Running | Stoppable | 1   |
| Bit 2  |       | RESERVED  |                                            |      |              |           | 1   |
| Bit 1  |       | RESERVED  |                                            |      |              |           | 1   |
| Bit 0  |       | RESERVED  |                                            |      |              |           | 1   |

I<sup>2</sup>C Table: Output Control Register

| Byte 5 | Pin #                                             | Name                | Control Function          | Type | 0      | 1    | PWD |
|--------|---------------------------------------------------|---------------------|---------------------------|------|--------|------|-----|
| Bit 7  | 19,20,22,23,<br>24,25,26,27,30,31,<br>32,33,35,36 | SRC Stop Drive Mode | Drive Mode in<br>PCI_Stop | RW   | Driven | Hi-Z | 0   |
| Bit 6  |                                                   | RESERVED            |                           |      |        |      | 0   |
| Bit 5  |                                                   | RESERVED            |                           |      |        |      | 0   |
| Bit 4  |                                                   | RESERVED            |                           |      |        |      | 0   |
| Bit 3  | 19,20,22,23,<br>24,25,26,27,30,31,<br>32,33,35,36 | SRC PD Drive Mode   | Drive Mode in PD          | RW   | Driven | Hi-Z | 0   |
| Bit 2  | 35,36                                             | CPUCLK_ITP          | Drive Mode in PD          | RW   | Driven | Hi-Z | 0   |
| Bit 1  | 40,41                                             | CPUCLK1             | Drive mode in PD          | RW   | Driven | Hi-Z | 0   |
| Bit 0  | 43,44                                             | CPUCLK0             | Drive mode in PD          | RW   | Driven | Hi-Z | 0   |

I<sup>2</sup>C Table: Output Control Register

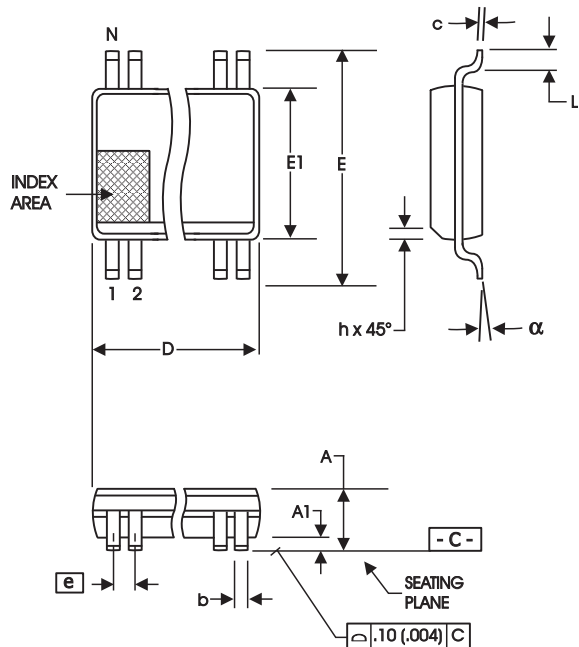
| Byte 6 | Pin #                                                                                | Name                  | Control Function               | Type | 0                                                                  | 1                                                               | PWD     |
|--------|--------------------------------------------------------------------------------------|-----------------------|--------------------------------|------|--------------------------------------------------------------------|-----------------------------------------------------------------|---------|
| Bit 7  | -                                                                                    | Test Mode Selection   | Test Mode<br>Selection         | RW   | Hi-Z                                                               | REF/N                                                           | 0       |
| Bit 6  | -                                                                                    | Test Clock Mode Entry | Test Mode                      | RW   | Disable                                                            | Enable                                                          | 0       |
| Bit 5  | -                                                                                    | RESERVED              |                                |      |                                                                    |                                                                 | 0       |
| Bit 4  | 52                                                                                   | REFOUT Strength       | Strength Prog                  | RW   | 1X                                                                 | 2X                                                              | 1       |
| Bit 3  | 17,18,19,20,22,23,<br>24,25,26,27,30,31,<br>32,33,35,36<br>54,55,56,3,4,5,8,9,<br>10 | PCI/SRC_STOP          | Stop all PCI and<br>SRC clocks | RW   | Enabled, all<br>stoppable PCI<br>and SRC<br>clocks are<br>stopped. | Disabled, all<br>stoppable PCI<br>and SRC clocks<br>are running | 1       |
| Bit 2  | -                                                                                    | FS_C                  | readback                       | R    | -                                                                  | -                                                               | LATCHED |
| Bit 1  | -                                                                                    | FS_B                  | readback                       | R    | -                                                                  | -                                                               | LATCHED |
| Bit 0  | -                                                                                    | FS_A                  | readback                       | R    | -                                                                  | -                                                               | LATCHED |

I<sup>2</sup>C Table: Vendor & Revision ID Register

| Byte 7 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------|------------------|------|---|---|-----|
| Bit 7  | -     | RID3 | REVISION ID      | R    | - | - | 0   |
| Bit 6  | -     | RID2 |                  | R    | - | - | 0   |
| Bit 5  | -     | RID1 |                  | R    | - | - | 0   |
| Bit 4  | -     | RID0 |                  | R    | - | - | 0   |
| Bit 3  | -     | VID3 | VENDOR ID        | R    | - | - | 0   |
| Bit 2  | -     | VID2 |                  | R    | - | - | 0   |
| Bit 1  | -     | VID1 |                  | R    | - | - | 0   |
| Bit 0  | -     | VID0 |                  | R    | - | - | 1   |

## Test Clarification Table

| Comments                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | HW                      |                          | SW                     |                       | OUTPUT |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|--------------------------|------------------------|-----------------------|--------|
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | FS_C/TEST_SEL<br>HW PIN | FS_B/TEST_MODE<br>HW PIN | TEST ENTRY BIT<br>B6b6 | REF/N or HI-Z<br>B6b7 |        |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 0                       | X                        | 0                      | X                     | NORMAL |
| <ul style="list-style-type: none"> <li>FS_C/TEST_SEL is a 3-level latched input. <ul style="list-style-type: none"> <li>Power-up w/ V &gt;= 2.0V to select TEST</li> <li>Power-up w/ V &lt; 2.0V to have pin function as FS_C.</li> </ul> </li> <li>When pin is FS_C, VIH_FS and VIL_FS levels apply.</li> <li>FS_B/TEST_MODE is a low-threshold input <ul style="list-style-type: none"> <li>VIH_FS and VIL_FS levels apply.</li> <li>TEST_MODE is a real time input</li> </ul> </li> <li>TEST_SEL can be invoked after power up through SMBus B6b6. <ul style="list-style-type: none"> <li>If TEST is selected by B6b6, only B6b7 controls TEST_MODE. The FS_B/TEST_Mode pin is not used.</li> </ul> </li> <li>Power must be cycled to exit TEST.</li> </ul> | 1                       | 0                        | X                      | 0                     | HI-Z   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 1                       | 0                        | X                      | 1                     | REF/N  |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 1                       | 1                        | X                      | 0                     | REF/N  |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 1                       | 1                        | X                      | 1                     | REF/N  |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 0                       | X                        | 1                      | 0                     | HI-Z   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 0                       | X                        | 1                      | 1                     | REF/N  |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                         |                          |                        |                       |        |
| B6b6: 1= ENTER TEST MODE, Default = 0 (NORMAL OPERATION)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                         |                          |                        |                       |        |
| B6b7: 1= REF/N, Default = 0 (HI-Z)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                         |                          |                        |                       |        |



**56-Lead, 300 mil Body, 25 mil, SSOP**

| SYMBOL | In Millimeters<br>COMMON DIMENSIONS |       | In Inches<br>COMMON DIMENSIONS |       |
|--------|-------------------------------------|-------|--------------------------------|-------|
|        | MIN                                 | MAX   | MIN                            | MAX   |
| A      | 2.41                                | 2.80  | .095                           | .110  |
| A1     | 0.20                                | 0.40  | .008                           | .016  |
| b      | 0.20                                | 0.34  | .008                           | .0135 |
| c      | 0.13                                | 0.25  | .005                           | .010  |
| D      | SEE VARIATIONS                      |       | SEE VARIATIONS                 |       |
| E      | 10.03                               | 10.68 | .395                           | .420  |
| E1     | 7.40                                | 7.60  | .291                           | .299  |
| e      | 0.635 BASIC                         |       | 0.025 BASIC                    |       |
| h      | 0.38                                | 0.64  | .015                           | .025  |
| L      | 0.50                                | 1.02  | .020                           | .040  |
| N      | SEE VARIATIONS                      |       | SEE VARIATIONS                 |       |
| a      | 0°                                  | 8°    | 0°                             | 8°    |

**VARIATIONS**

| N  | D mm. |       | D (inch) |      |
|----|-------|-------|----------|------|
|    | MIN   | MAX   | MIN      | MAX  |
| 56 | 18.31 | 18.55 | .720     | .730 |

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

## Ordering Information

**ICS954101yFLFT**

Example:

**ICS XXXX y F LFT**

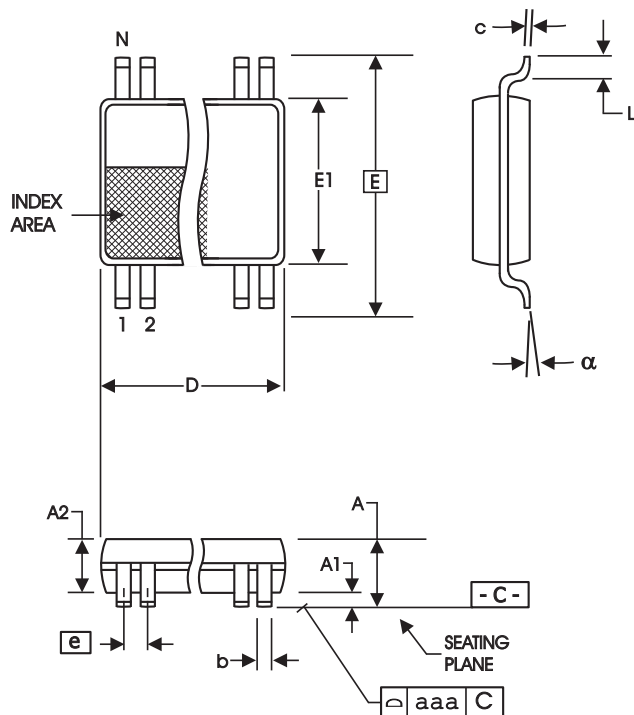
Designation for tape and reel packaging  
RoHS Compliant (Optional)

Package Type  
F = SSOP

Revision Designator (will not correlate with datasheet revision)

Device Type (consists of 3 to 7 digit numbers)

Prefix  
ICS, AV = Standard Device



**56-Lead 6.10 mm. Body, 0.50 mm. Pitch TSSOP**  
(240 mil) (20 mil)

| SYMBOL | In Millimeters    |      | In Inches         |      |
|--------|-------------------|------|-------------------|------|
|        | COMMON DIMENSIONS |      | COMMON DIMENSIONS |      |
|        | MIN               | MAX  | MIN               | MAX  |
| A      | --                | 1.20 | --                | .047 |
| A1     | 0.05              | 0.15 | .002              | .006 |
| A2     | 0.80              | 1.05 | .032              | .041 |
| b      | 0.17              | 0.27 | .007              | .011 |
| c      | 0.09              | 0.20 | .0035             | .008 |
| D      | SEE VARIATIONS    |      | SEE VARIATIONS    |      |
| E      | 8.10 BASIC        |      | 0.319 BASIC       |      |
| E1     | 6.00              | 6.20 | .236              | .244 |
| e      | 0.50 BASIC        |      | 0.020 BASIC       |      |
| L      | 0.45              | 0.75 | .018              | .030 |
| N      | SEE VARIATIONS    |      | SEE VARIATIONS    |      |
| a      | 0°                | 8°   | 0°                | 8°   |
| aaa    | --                | 0.10 | --                | .004 |

**VARIATIONS**

| N  | D mm. |       | D (inch) |      |
|----|-------|-------|----------|------|
|    | MIN   | MAX   | MIN      | MAX  |
| 56 | 13.90 | 14.10 | .547     | .555 |

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

## Ordering Information

**ICS954101yGLFT**

Example:

**ICS XXXX y G LFT**

Designation for tape and reel packaging  
RoHS Compliant (Optional)

Package Type  
G = TSSOP

Revision Designator (will not correlate with datasheet revision)

Device Type (consists of 3 to 7 digit numbers)

Prefix  
ICS, AV = Standard Device



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### Revision History

| Rev. | Issue Date | Description                                                                       | Page #  |
|------|------------|-----------------------------------------------------------------------------------|---------|
| E    | 6/1/2005   | 1. Updated Block Diagram.<br>2. Update LF Ordering Information to RoHS Compliant. | 4,15-16 |
| F    | 0815/05    | 1. Removed Skew from REF Electrical Characteristics Table - only 1 REF output.    | 11      |
|      |            |                                                                                   |         |
|      |            |                                                                                   |         |

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## 954101 (Desktop Chipsets)

### Description

GRANTSDALE - CK410 clock, Intel Yellow Cover part

### Market Group

PC CLOCK

### Additional Info

ICS954101 follows Intel CK410 Yellow Cover specification. This clock synthesizer provides a single chip solution for next generation P4 Intel processors and Intel chipsets. ICS954101 is driven with a 14.318MHz crystal. It generates CPU outputs up to 400MHz. It also provides a tight ppm accuracy output for Serial ATA and PCI-Express support • Supports tight ppm accuracy clocks for Serial-ATA and • PCI-Express • Supports spread spectrum modulation, 0 to -0.5% down spread • Supports CPU clks up to 400MHz • Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning • Supports undriven differential CPU, SRC pair in PD# er management.

**Time is money**

### Related Orderable Parts

| Attributes                     | 954101DFLF           | 954101DFLFT          | 954101DGLF           | 954101DGLFT          |
|--------------------------------|----------------------|----------------------|----------------------|----------------------|
| <b>Voltage</b>                 | <b>3.3 V (PVG56)</b> | <b>3.3 V (PVG56)</b> | <b>3.3 V (PAG56)</b> | <b>3.3 V (PAG56)</b> |
| <b>Package</b>                 | SSOP 56              | SSOP 56              | TSSOP 56             | TSSOP 56             |
| <b>Speed</b>                   | NA                   | NA                   | NA                   | NA                   |
| <b>Temperature</b>             | C                    | C                    | C                    | C                    |
| <b>Status</b>                  | Active               | Active               | Active               | Active               |
| <b>Sample</b>                  | Yes                  | No                   | Yes                  | No                   |
| <b>Minimum Order Quantity</b>  | 130                  | 1000                 | 102                  | 1000                 |
| <b>Factory Order Increment</b> | 26                   | 1000                 | 34                   | 1000                 |

### Related Documents

| Type         | Title                             | Size   | Revision Date |
|--------------|-----------------------------------|--------|---------------|
| Datasheet    | <a href="#">954101 Datasheet</a>  | 189 KB | 03/27/2006    |
| Model - IBIS | <a href="#">954101 IBIS Model</a> | 237 KB | 03/27/2006    |



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|--------------------------------|----------------------|----------------------|----------------------|----------------------|
| <b>Voltage</b>                 | <b>3.3 V (PVG56)</b> | <b>3.3 V (PVG56)</b> | <b>3.3 V (PAG56)</b> | <b>3.3 V (PAG56)</b> |
| <b>Package</b>                 | SSOP 56              | SSOP 56              | TSSOP 56             | TSSOP 56             |
| <b>Speed</b>                   | NA                   | NA                   | NA                   | NA                   |
| <b>Temperature</b>             | C                    | C                    | C                    | C                    |
| <b>Status</b>                  | Active               | Active               | Active               | Active               |
| <b>Sample</b>                  | Yes                  | No                   | Yes                  | No                   |
| <b>Minimum Order Quantity</b>  | 130                  | 1000                 | 102                  | 1000                 |
| <b>Factory Order Increment</b> | 26                   | 1000                 | 34                   | 1000                 |

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