



LOW SKEW, 1-TO-4 LVCMOS/LVTTL-TO-LVDS FANOUT BUFFER

ICS8545I

General Description



The ICS8545I is a low skew, high performance 1-to-4 LVCMOS/LVTTL-to-LVDS Clock Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT.

Utilizing Low Voltage Differential Signaling (LVDS)

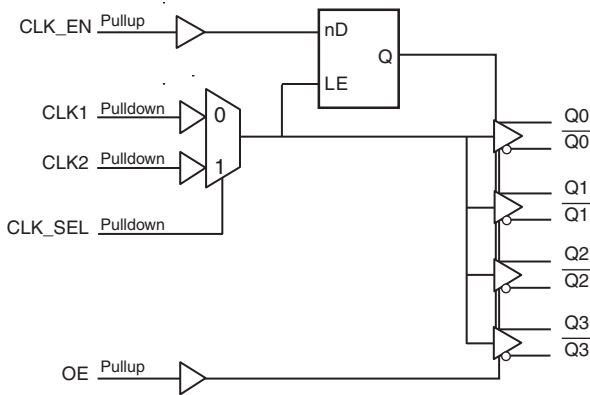
the ICS8545I provides a low power, low noise, solution for distributing clock signals over controlled impedances of 100Ω. The ICS8545I accepts a LVCMOS/LVTTL input level and translates it to 3.3V LVDS output levels.

Guaranteed output and part-to-part skew characteristics make the ICS8545I ideal for those applications demanding well defined performance and repeatability.

Features

- Four differential LVDS output pairs
- Two LVCMOS/LVTTL clock inputs to support redundant or selectable frequency fanout applications
- Maximum output frequency: 650MHz
- Translates LVCMOS/LVTTL input signals to LVDS levels
- Output skew: 40ps (maximum)
- Part-to-part skew: 500ps (maximum)
- Propagation delay: 3.6ns (maximum)
- Additive phase jitter, RMS: 0.13ps (typical)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment

| | | | |
|-----------------|----|----|-----------------|
| GND | 1 | 20 | Q0 |
| CLK_EN | 2 | 19 | Q0 |
| CLK_SEL | 3 | 18 | V _{DD} |
| CLK1 | 4 | 17 | Q1 |
| nc | 5 | 16 | Q1 |
| CLK2 | 6 | 15 | Q2 |
| nc | 7 | 14 | Q2 |
| OE | 8 | 13 | GND |
| GND | 9 | 12 | Q3 |
| V _{DD} | 10 | 11 | Q3 |

ICS8545I

20-Lead TSSOP

6.5mm x 4.4mm x 0.925mm

package body

G Package

Top View

Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|----------|----------------------|--------|----------|--|
| 1, 9, 13 | GND | Power | | Power supply ground. |
| 2 | CLK_EN | Input | Pullup | Synchronizing clock enable. When HIGH, clock outputs follows clock input. When LOW, Q outputs are forced low, \overline{Q} outputs are forced high. LVCMOS / LVTTL interface levels. |
| 3 | CLK_SEL | Input | Pulldown | Clock select input. When HIGH, selects CLK2 input. When LOW, selects CLK1 input. LVCMOS / LVTTL interface levels. |
| 4 | CLK1 | Input | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels. |
| 5, 7 | nc | Unused | | No connect. |
| 6 | CLK2 | Input | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels. |
| 8 | OE | Input | Pullup | Output enable. Controls enabling and disabling of outputs Q0/ $\overline{Q0}$ through Q3/ $\overline{Q3}$. LVCMOS/LVTTL interface levels. |
| 10, 18 | V _{DD} | Power | | Positive supply pins. |
| 11, 12 | $\overline{Q3}$, Q3 | Output | | Differential output pair. LVDS interface levels. |
| 14, 15 | $\overline{Q2}$, Q2 | Output | | Differential output pair. LVDS interface levels. |
| 16, 17 | $\overline{Q1}$, Q1 | Output | | Differential output pair. LVDS interface levels. |
| 19, 20 | $\overline{Q0}$, Q0 | Output | | Differential output pair. LVDS interface levels. |

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|------------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | k Ω |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | k Ω |

Function Tables

Table 3A. Control Input Function Table

| Inputs | | | | Outputs | |
|--------|--------|---------|-----------------|---------|--------------------|
| OE | CLK_EN | CLK_SEL | Selected Source | Q0:Q3 | $\overline{Q0:Q3}$ |
| 0 | X | X | | Hi-Z | Hi-Z |
| 1 | 0 | 0 | CLK1 | Low | High |
| 1 | 0 | 1 | CLK2 | Low | High |
| 1 | 1 | 0 | CLK1 | Active | Active |
| 1 | 1 | 1 | CLK2 | Active | Active |

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1. In the active mode, the state of the outputs are a function of the CLK1 and CLK2 inputs as described in Table 3B.

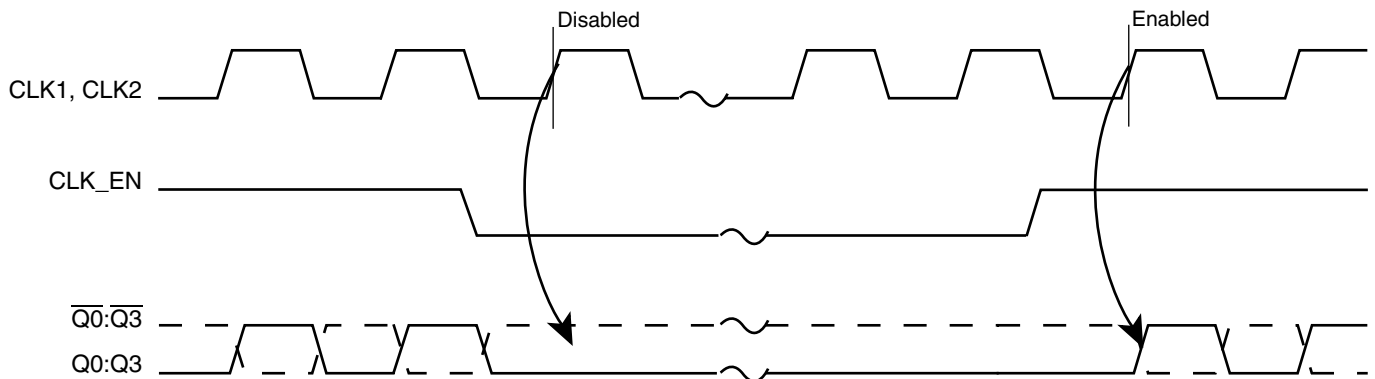


Figure 1. CLK_EN Timing Diagram

Table 3B. Clock Input Function Table

| Inputs | Outputs | |
|--------------|---------|--------------------|
| CLK1 or CLK2 | Q0:Q3 | $\overline{Q0:Q3}$ |
| 0 | LOW | HIGH |
| 1 | HIGH | LOW |

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|--------------------------|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_I | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, I_O Continuous Current Surge Current | 10mA 15mA |
| Package Thermal Impedance, θ_{JA} | 73.2°C/W (0 lfm) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-------------------------|-----------------|---------|---------|---------|-------|
| V_{DD} | Positive Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{DD} | Power Supply Current | | | | 52 | mA |

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|---------------------|--------------------------------|---------|----------------|---------|
| V_{IH} | Input High Voltage | | 2 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | CLK1, CLK2 | -0.3 | | 1.3 | V |
| | | OE, CLK_EN, CLK_SEL | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | CLK1, CLK2, CLK_SEL | $V_{DD} = V_{IN} = 3.465V$ | | 150 | μA |
| | | OE, CLK_EN | $V_{DD} = V_{IN} = 3.465V$ | | 5 | μA |
| I_{IL} | Input Low Current | CLK1, CLK2, CLK_SEL | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5 | | μA |
| | | OE, CLK_EN | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150 | | μA |

Table 4C. LVDS DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|---|-----------------|---------|---------|---------|---------------|
| V_{OD} | Differential Output Voltage | | 200 | 280 | 360 | mV |
| ΔV_{OD} | V_{OD} Magnitude Change | | | | 40 | mV |
| V_{OS} | Offset Voltage | | 1.125 | 1.25 | 1.375 | V |
| ΔV_{OS} | V_{OS} Magnitude Change | | | 5 | 25 | mV |
| I_{OZ} | High Impedance Leakage | | -10 | ± 1 | +10 | μA |
| I_{OFF} | Power Off Leakage | | -20 | ± 1 | +20 | μA |
| I_{OSD} | Differential Output Short Circuit Current | | | -3.5 | -5 | mA |
| I_{OS} | Output Short Circuit Current | | | -3.5 | -5 | mA |
| V_{OH} | Output Voltage High | | | 1.34 | 1.6 | V |
| V_{OL} | Output Voltage Low | | 0.9 | 1.06 | | V |

AC Electrical Characteristics

Table 5. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

| Parameter | Symbol | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|---|---|---------|---------|---------|-------|
| f_{MAX} | Output Frequency | | | | 650 | MHz |
| t_{PD} | Propagation Delay; NOTE 1 | $f \leq 650\text{MHz}$ | 1.4 | | 3.6 | ns |
| t_{jit} | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section | 156.25MHz, Integration Range: 12kHz – 20MHz | | 0.13 | | ps |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 4 | | | | 40 | ps |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 3, 4 | | | | 500 | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% @ 50MHz | 200 | 400 | 700 | ps |
| odc | Output Duty Cycle | $f \leq 266\text{MHz}$ | 45 | | 55 | % |
| | | $f > 266\text{MHz}$ | 40 | | 60 | % |

All parameters measured at $f \leq 650\text{MHz}$ unless noted otherwise.

NOTE 1: Measured from $V_{DD}/2$ of the input to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at $V_{DD}/2$ of the input to the differential output crossing point.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions.

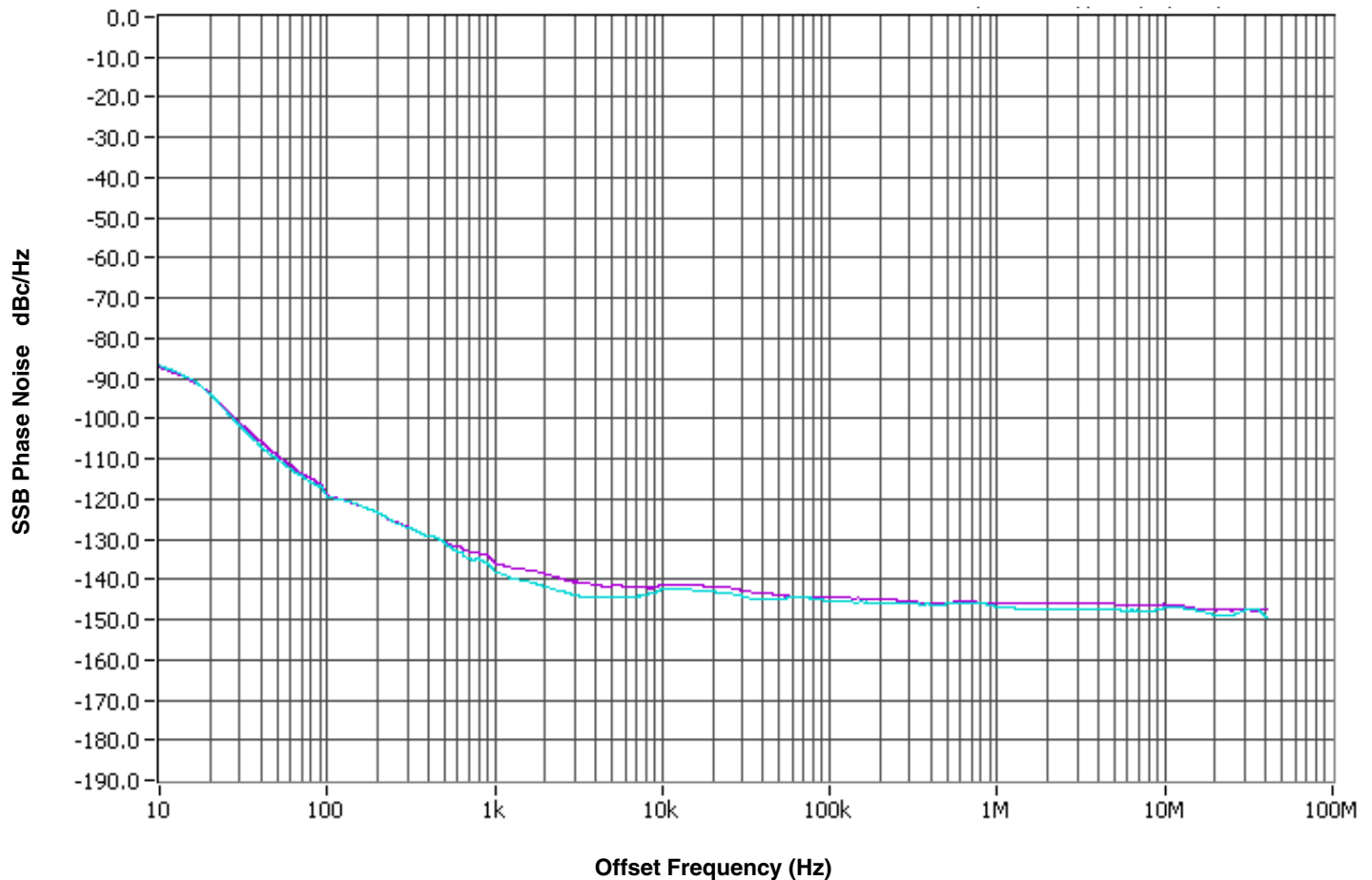
Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band

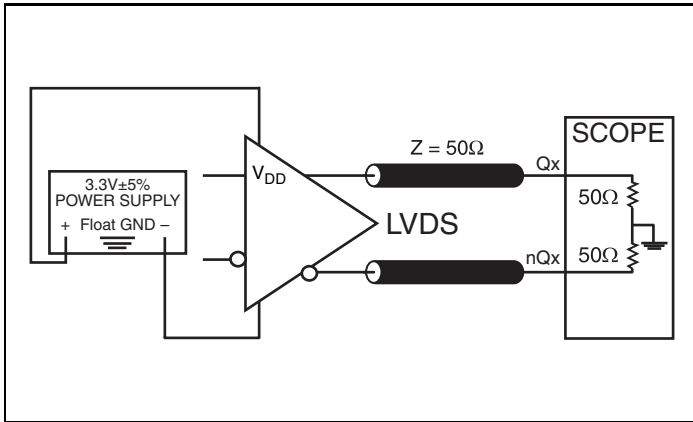
to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



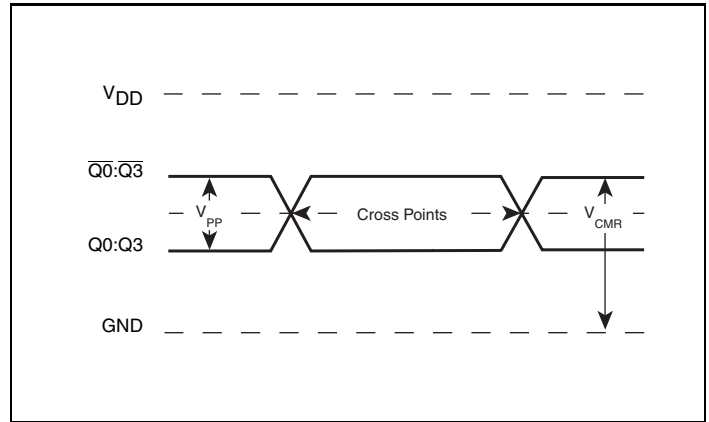
As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device

meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

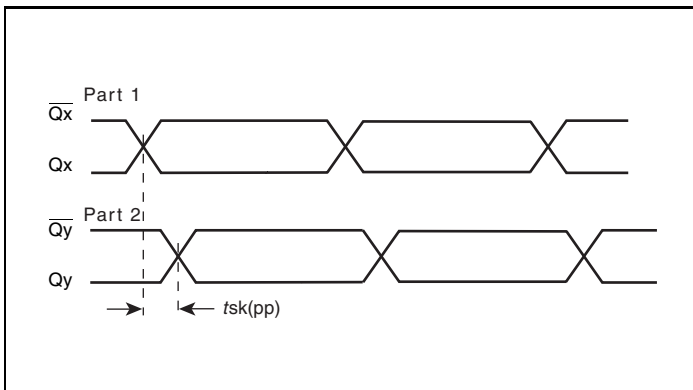
Parameter Measurement Information



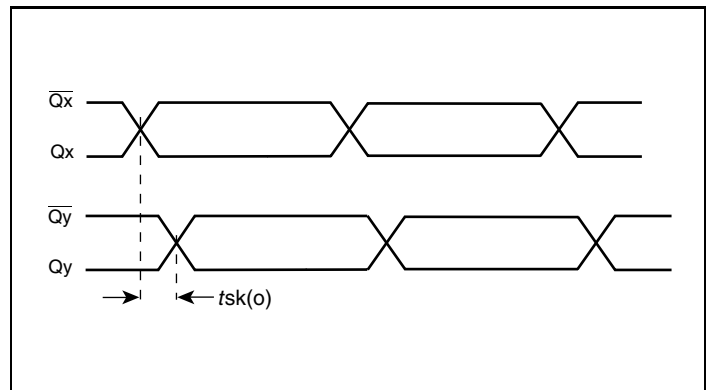
3.3V LVDS Output Load AC Test Circuit



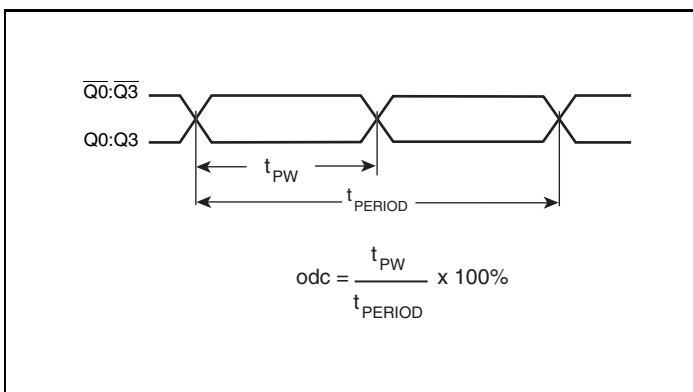
Differential Output Level



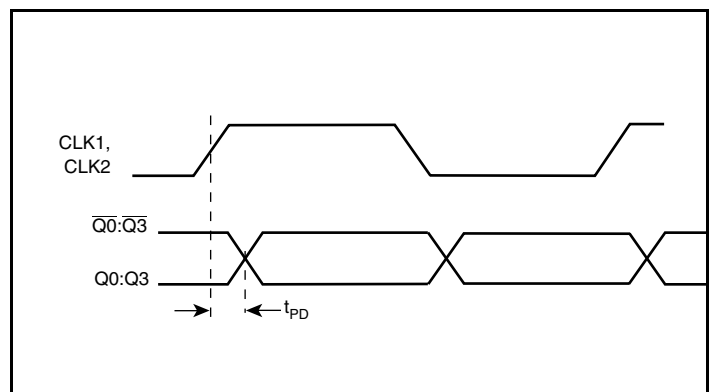
Part-to-Part Skew



Output Skew

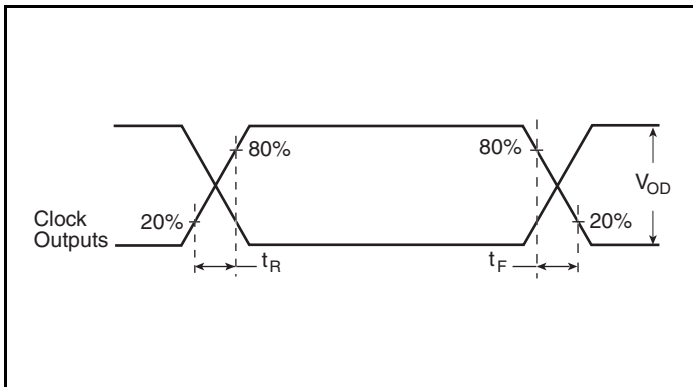


Output Duty Cycle/Pulse Width/Period

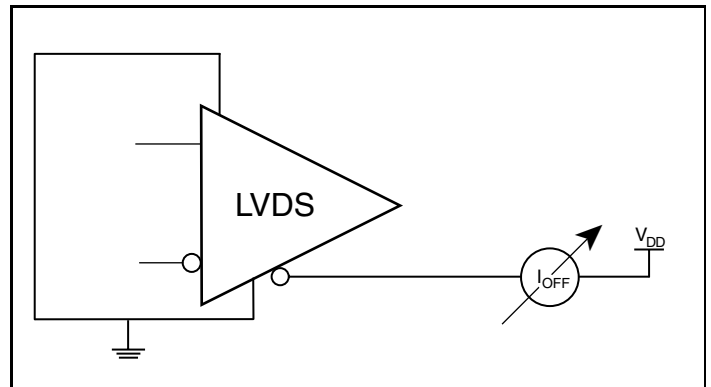


Propagation Delay

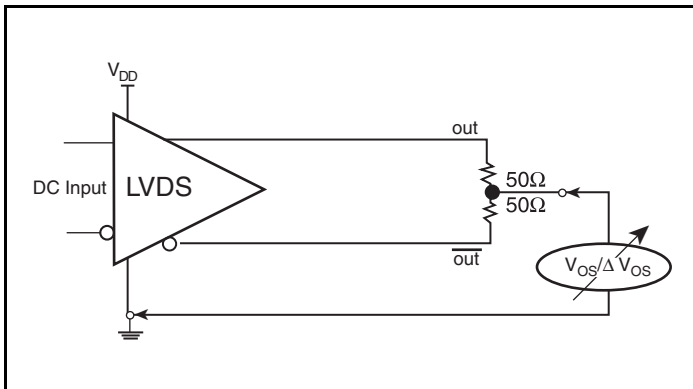
Parameter Measurement Information, continued



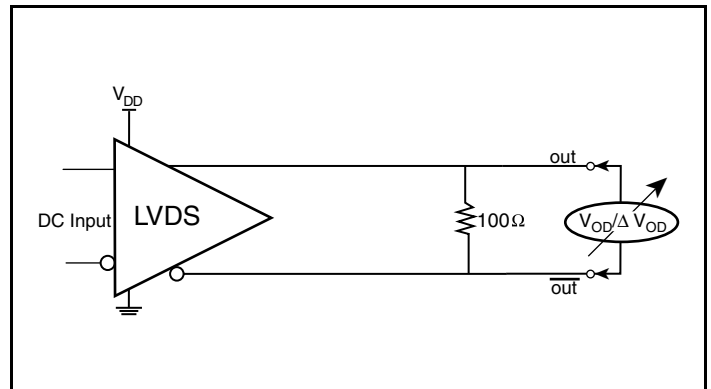
Output Rise/Fall Time



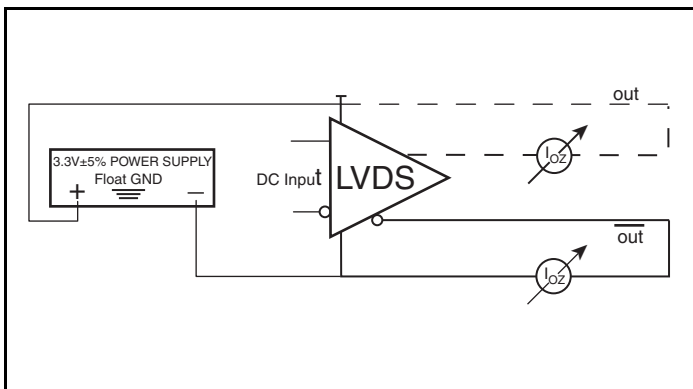
Power Off Leakage Setup



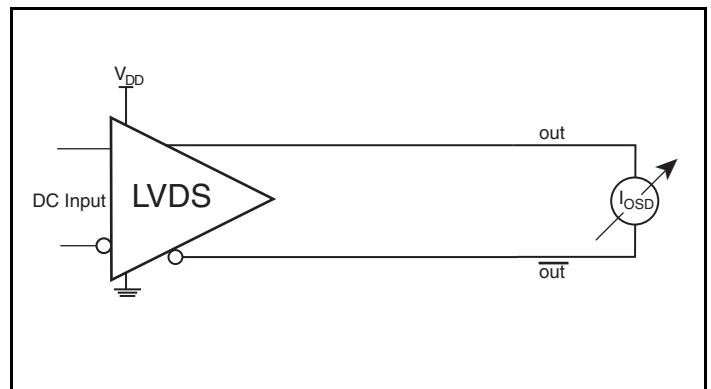
Offset Voltage Setup



Differential Output Voltage Setup

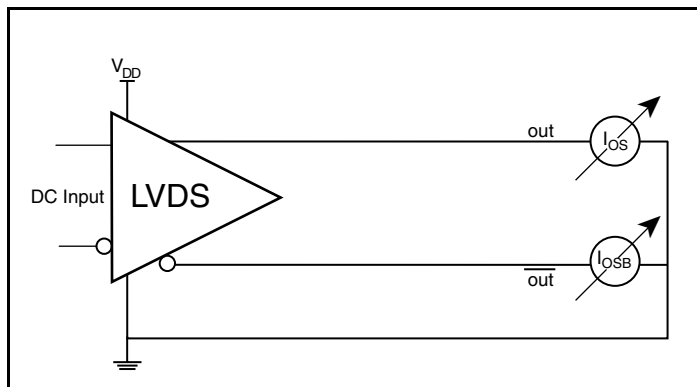


High Impedance Leakage Current Setup



Differential Output Short Circuit Setup

Parameter Measurement Information, continued



Output Short Circuit Current Setup

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK Inputs

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from the CLK input to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100 Ω across. If they are left floating, there should be no trace attached.

3.3V LVDS Driver Termination

A general LVDS interface is shown in Figure 2. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input.

For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

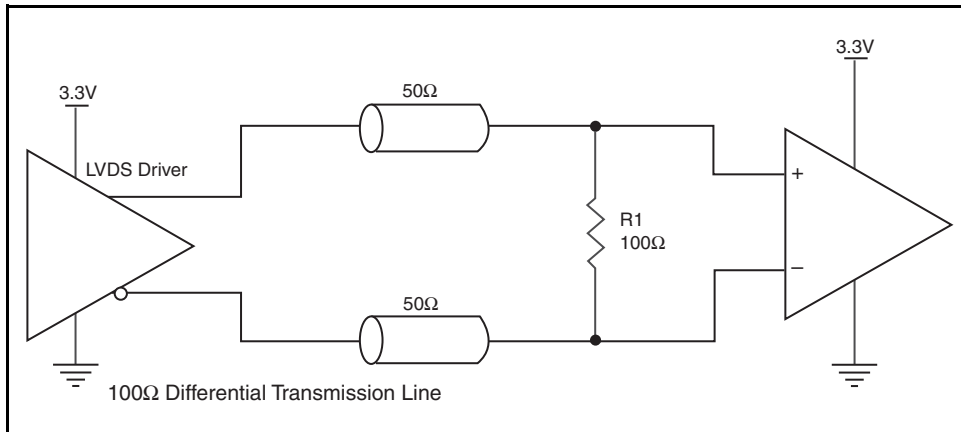


Figure 2. Typical LVDS Driver Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8545I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8545I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{DD_MAX} * I_{DD_MAX} = 3.465V * 52mA = \mathbf{180.18mW}$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.180\text{W} * 66.6^\circ\text{C/W} = 97^\circ\text{C}. \text{ This is well below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 20 Lead TSSOP, Forced Convection

| Linear Feet per Minute | θ_{JA} by Velocity | | |
|--|---------------------------|----------|----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP

| Linear Feet per Minute | θ_{JA} by Velocity | | |
|--|---------------------------|----------|----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |

Transistor Count

The transistor count for ICS8545I is: 644

Package Outline and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP

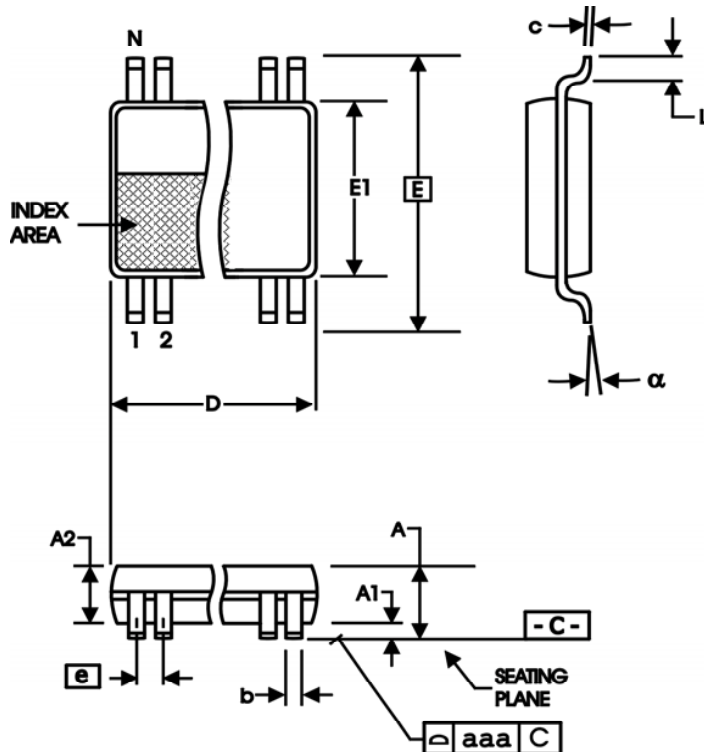


Table 8. Package Dimensions

| All Dimensions in Millimeters | | |
|-------------------------------|------------|---------|
| Symbol | Minimum | Maximum |
| N | 20 | |
| A | | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 6.40 | 6.60 |
| E | 6.40 Basic | |
| E1 | 4.30 | 4.50 |
| e | 0.65 Basic | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|--------------|---------------------------|--------------------|---------------|
| 8545BGI | ICS8545BGI | 20 Lead TSSOP | Tube | -40°C to 85°C |
| 8545BGIT | ICS8545BGI | 20 Lead TSSOP | 2500 Tape & Reel | -40°C to 85°C |
| 8545BGILF | ICS8545BGILF | "Lead-Free" 20 Lead TSSOP | Tube | -40°C to 85°C |
| 8545BGILFT | ICS8545BGILF | "Lead-Free" 20 Lead TSSOP | 2500 Tape & Reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|-----|-------|------|--|---------|
| B | T5 | 1 | Features Section - added Additive Phase Jitter bullet. | 5/31/07 |
| | | 5 | AC Characteristics Table - added Additive Phase Jitter spec. | |
| | | 6 | Added <i>Additive Phase Jitter Plot</i> . | |
| | | 11 | Added <i>Power Considerations</i> section. | |
| B | T9 | 13 | Ordering Information Table - added lead-free marking. | 2/15/08 |

ICS8545I

LOW SKEW, 1-TO-4, LVCMOS/LVTTL-TO-LVDS FANOUT BUFFER

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