16 OUTPUT LOW SKEW CLOCK GENERATOR

MK74CG117B

Description

The MK74CG117B is a monolithic CMOS high speed, low-skew clock driver that includes an on-chip PLL. Ideal for communications and other systems that require a large number of high-speed clocks, the unique combination of PLL and 16 low-skew outputs can eliminate oscillators and low skew buffers from systems.

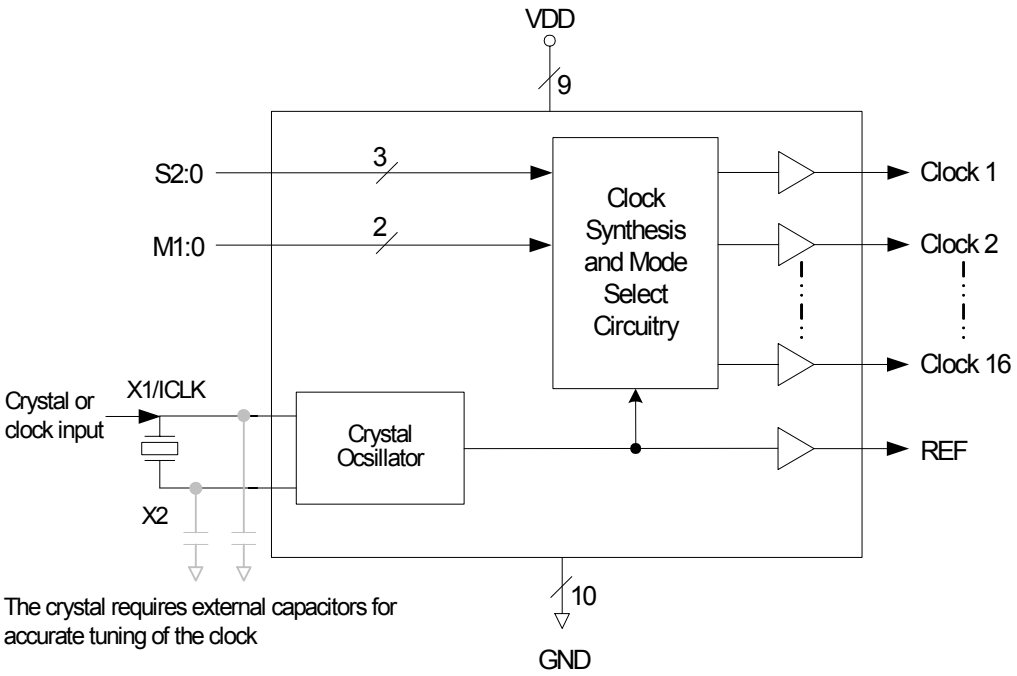
The device has a number of built in multipliers, making it possible to run from one inexpensive, low frequency crystal, and produce high frequency clock outputs. Another selection allows the chip to run as a divider, dividing the input clock by two (or 4 using the mode select).

The device also has a buffered reference output, allowing multiple devices to be easily driven from one clock source.

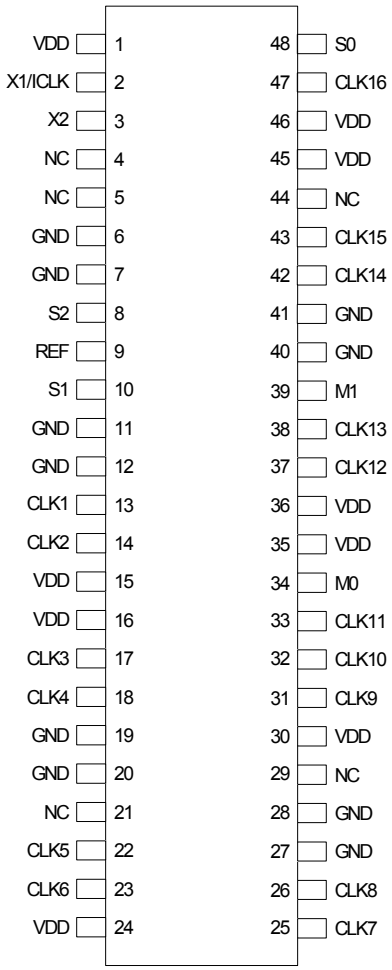
Features

- 48-pin SSOP (300 mil) package, Pb free
- On-chip PLL generates output clocks up to 100 MHz from a simple crystal or clock input
- 16 low-skew outputs
- Output skew less than 250 ps on rising edges
- Ability to configure as:
  - 16 clocks at full frequency
  - 12 at full and 4 at half frequency
  - 8 at full and 8 at half frequency
- Tri-state mode for Output Enable function
- 3.3 V ±5% supply voltage
- Industrial temperature version available

Block Diagram



Pin Assignment



48-pin (300 mil) SSOP

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1, 15, 16, 24, 30, 35, 36, 45, 46	VDD	Power	Connect to VDD.
2	X1/ICLK	XI	Connect to a crystal input or clock.
3	X2	XO	Connect to a crystal, or leave unconnected for clock input.
4, 5, 21, 29, 44	NC	—	No connect. Nothing is connected to these pins.
6, 7, 11, 12, 19, 20, 27, 28, 40, 41	GND	Power	Connect to ground.
8, 10, 48	S2, S1, S0	Input	Multiplier select pins. See table 2.
9	REF	Output	Crystal oscillator buffered reference clock output.
13, 14, 17, 18	CLK1 - 4	Output	Clock 1 - 4. Can be either full or half speed per Table 1.
22, 23, 25, 26, 31, 32, 33, 37	CLK5 - 12	Output	Clock outputs 5 - 12. At full (1x) speed unless tristated per Table 1.
34, 39	M0, M1	Input	Mode Select pins. Selects tri-state or speed of outputs per Table 1.
38, 42, 43, 47	CLK13 - 16	Output	Clock 13 - 16. Can be either full or half speed per Table 1.

External Components

The MK74CG117B requires a minimum number of external components for proper operation.

Decoupling Capacitor

A decoupling capacitor of 0.1µF must be connected between each VDD and GND. Connect the capacitor as close to these pins as possible. For optimum device performance, mount the decoupling capacitor on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, observe the following guidelines:

1) Mount the 0.01µF decoupling capacitor on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to the VDD pin and the PCB trace to the ground via should be kept as short as possible.

2) To minimize EMI, place the 33Ω series-termination resistor (if needed) close to the clock output.

3) An optimum layout is one with all components on the same side of the board, thus minimizing vias through other signal layers. Other signal traces should be routed away from the MK74CG117B device. This includes signal traces located underneath the device, or on layers adjacent to the ground plane layer used by the device.

Crystal Information

The crystal used should be a fundamental mode (do not use third overtone), parallel resonant crystal. The oscillator has internal caps that provide the proper load for a crystal with C_L = 18 pF. The value of these capacitors is given by the following equation:

$$\text{Crystal caps (pF)} = (C_L - 18) \times 2$$

Power Dissipation, Termination, and Operating Frequency

As with all clock drivers, the power dissipated by the MK74CG117B is affected by the external loading on the output pins. This consists of the capacitance of the load that is being driven, as well as the PC board trace itself. Since this capacitance must be charged and discharged with each cycle of the output clock, as the frequency goes up. so does the power required. Operating below the specified maximum output clock frequency shown in Table 2 will keep the MK74CG117B power dissipation within acceptable limits.

External series termination resistors must be used in series with each output. These resistors serve two purposes: The first is to match the source impedance to the line (PC board trace) that is being driven. This will minimize reflections that cause non-linear transitions on the output clock waveform. The output impedance of the MK74CG117B is approximately 20Ω; assuming a 50Ω line, then a 33Ω resistor should be used at each output as shown in Figure 1.

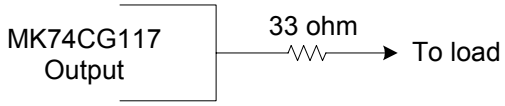
Table 1. Tri-state and Mode Select

M1	M0	Mode	at CLK(1x)	at CLK/2(0.5x)	Max Output Freq.
0	0	All outputs, including REF, tri-stated	Z	Z	
0	1	12 @ 1x, 4 @ 0.5x	CLK1–12	CLK13–16	83.3 MHz 0.8
1	0	8 @ 1x, 8 @ 0.5x	CLK5–12	CLK1–4, 13–16	83.3 MHz 1.25
1	1	16 outputs @ 1x	CLK1–16	None	100 MHz

Table 2. Multiplier Selections (Input and CLK Frequencies in MHz)

S2	S1	S0	Input	Multiplier	CLK Out	Comments
0	0	0	33–50	0.5	16.5–25	Divider only; no PLL
0	0	1	20–50	1	20–50	PLL
0	1	0	16–40	1.25	20–50	PLL
0	1	1	10–50	2	20–100	PLL
1	0	0	8–40	2.5	20–100	PLL
1	0	1	8–30	3.333	26.7–100	PLL
1	1	0	8–25	4	32–100	PLL
1	1	1	8–20	5	40–90	PLL

Figure 1. External Termination



As speeds rise, the limiting factor in device operation becomes the power generated by having a large number of drivers in one package. Using the external termination resistors reduces the power dissipated within the device, allowing output frequencies up to 100 MHz.

Note that the maximum operating frequency of the MK74CG117A is determined by the Mode selected from Table 1 and the Multiplier selected from Table 2. For output frequencies above 83.3 MHz, all 16 outputs must be at the same frequency (M1=M0=1).

When operating with a combination of 1X and 0.5X outputs, the output frequency cannot exceed 83.3 MHz.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK74CG117B. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device, at these or any other conditions, above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD (referenced to GND)	7 V
All Inputs and Outputs (referenced to GND)	0.5 V to VDD+0.5 V
Ambient Operating Temperature	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	° C
Power Supply Voltage (measured in respect to GND)	+3.0		3.63	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.14	3.3	3.47	V
Supply Current (at 50 MHz)	IDD	No load		63		mA
Input High Voltage, ICLK	V_{IH}	pin 2	VDD-1	VDD/2		V
Input Low Voltage, ICLK	V_{IL}	pin 2		VDD/2	1	V
Output High Voltage	V_{OH}	I_{OH} = -8 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.0			V
Output Low Voltage, 3.3 V	V_{OL}	I_{OL} = 12 mA			0.4	V
Short Circuit Current		Each output		±35		mA
Input Capacitance	C_{IN}	S0, S1, FRSEL pins		7	6	pF

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature 0 to +85° C, C_L = 15 pF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Clock Frequency		See table 2				
Input Crystal Frequency		Except when S2=S1=1	8		20	MHz
Output Clock Frequency (see tables 1, 2)		M1=M0=1			100	MHz
Output Clock Duty Cycle		At VDD/2	45	50	55	%
Output Clock Rising Edge Skew		VDD=3.3 V, Note 2		150	250	ps
Absolute Clock Period Jitter, except REF		VDD=3.3 V		±300		ps
Absolute Clock Period Jitter, REF		VDD=3.3 V		±500		ps
Output Clock Rise Time	t_R	0.8 to 2.0 V, Note 1		1.5	2	ns
Output Clock Fall Time	t_F	2.0 V to 0.8 V, Note 1		1.5	2	ns
Maximum Load per Total of 16 Outputs, with 33 Ω termination, Note 3		100 MHz output clock			240	pF
		83.3 MHz output clock			320	pF

Note 1: Based upon characterization data with a 33 Ω series termination resistor and 15 pF capacitor to ground.

Note 2: Between any two outputs with equal loading.

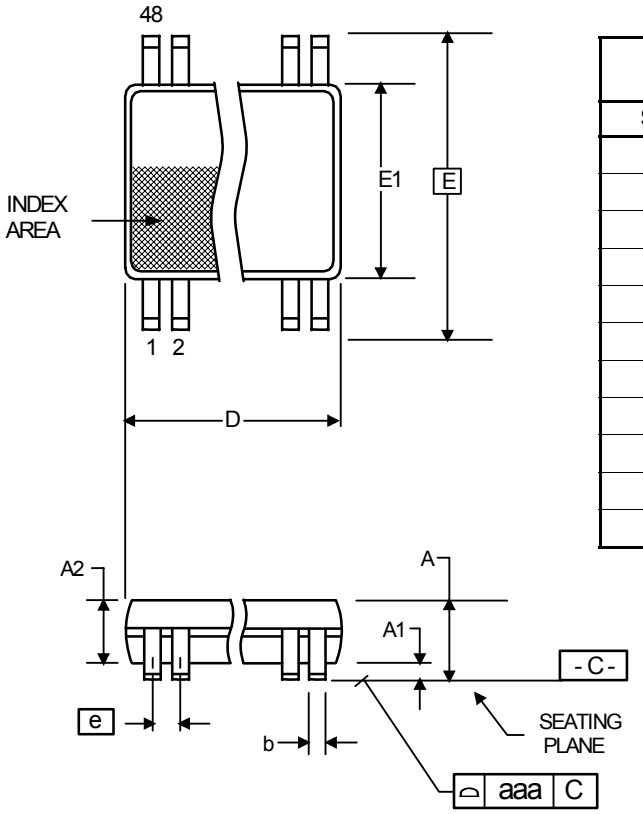
Note 3: Additional load may be driven with the addition of an external heat sink. Contact IDT for details.

Thermal Characteristics for 48-pin SSOP

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		80		°C/W
	θ_{JA}	1 m/s air flow		67		°C/W
	θ_{JA}	3 m/s air flow		54		°C/W
Thermal Resistance Junction to Case	θ_{JC}			45		°C/W

Package Outline and Package Dimensions (48-pin SSOP, 300 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	15.75	16.00	.620	.630
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK74CG117BFLF	74CG117BFLF	Tubes	48-pin SSOP	0 to +70° C
MK74CG117BFLFT	74CG117BFLF	Tape and Reel	48-pin SSOP	0 to +70° C
MK74CG117BFILF	74CG117BFILF	Tubes	48-pin SSOP	-40 to +85° C
MK74CG117BFILFT	74CG117BFILF	Tape and Reel	48-pin SSOP	-40 to +85° C

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